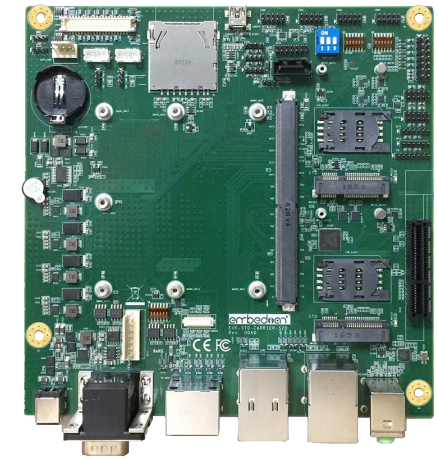
User's Manual

EVK-STD-CARRIER-S20



Development Board for SMARC V2.0 compliant modules

Revision History

Revision	Date	Changes from Previous Revision
1.0	2017/04/25	Initial Release

USER INFORMATION

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Table of Contents

Using this Manual

This guide provides information about the *SMARC Evaluation Carrier* for embedded *SMARC* core module family. All *SMARC* v 2.0 compliant modules should be able to work under *EVK-STD-CARRIER-S20*.

Conventions used in this guide

This table describes the typographic conventions used in this guide:

This Convention	Is used for
Italic type	Emphasis, new terms, variables, and document titles.
`monospaced type`	Filenames, pathnames, and code examples.

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To contact Embedian by	Use
Mail	Embedian, Inc. 4F-7. 432 Keelung Rd. Sec. 1, Taipei 11051, Taiwan
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FCC Class B

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the *FCC* Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Packing List

Before installation, please ensure the following items have been shipped.

Items	
EVK-STD-CARRIER-S20	*1*
12V/3A Power Adapter	*1*
LDVS Cable (*)	*1*
LVDS Backlight Cable (*)	*1*
Pre-Installed Bring Up SD Card (**)	*1*
2x5 Box Header to DB9 Cable	*1*
SATA Power Cable	*1*

Note 1:

LVDS cables and *LVDS* backlight cables support the following panels.

1. *AUO G240HW01 V0* 24 inch-wide 1920 (H) x 1080 (V) TFT color LCD or
2. *AUO G185XW01 V2* 18.5 inch-wide WXGA 1366 (H) x 768 (V) TFT color LCD or
3. *AUO G070VW01 V0* 7 inch WVGA 800 (H) x 480 (V) TFT color LCD

If not specified, the default shipping will be cables for 7-inch G070VW01.

Note 2:

Pre-installed SD card only come with the case when users also purchase *Embedian's SMARC* module at the same time.

Part Number	Description
SMARC-T3354-600	TI AM3352 600MHz, 3.3V VDDIO (0°C~60°C)
SMARC-T3354-01G	TI AM3354 1GHz, 3.3V VDDIO (0°C~60°C)
SMARC-T3354-800-I	TI AM3352 800MHz, 3.3V VDDIO (-40°C~85°C)
SMARC-T4378-800	TI AM4378 Cortex-A9 800MHz, 3.3V and 1.8V VDDIO (0°C~60°C)
SMARC-T4378-01G	TI AM4378 Cortex-A9 1GHz, 3.3V and 1.8V VDDIO (0°C~60°C)
SMARC-T4378-800-I	TI AM4378 Cortex-A9 1GHz, 3.3V and 1.8V VDDIO (-40°C~85°C)
SMARC-T4378-01G-I	TI AM4378 Cortex-A9 1GHz, 3.3V and 1.8V VDDIO (-40°C~85°C)
SMARC-FiMX6-S	Freescale i.MX6 Solo Core 1GHz with 512MB memory, 1.8V and 3.3V VDDIO (0°C~60°C)
SMARC-FiMX6-U-1G	Freescale i.MX6 Dual Lite Core 1GHz with 1GB memory, 1.8V and 3.3V VDDIO (0°C~60°C)
SMARC-FiMX6-D-1G	Freescale i.MX6 Dual Core 1GHz with 1GB memory, 1.8V and 3.3V VDDIO (0°C~60°C)
SMARC-FiMX6-D-2G	Freescale i.MX6 Dual Core 1GHz with 2GB memory, 1.8V and 3.3V VDDIO (0°C~60°C)
SMARC-FiMX6-Q-1G	Freescale i.MX6 Quad Core 1GHz with 1GB memory, 1.8V and 3.3V VDDIO (0°C~60°C)
SMARC-FiMX6-Q-2G	Freescale i.MX6 Quad Core 1GHz with 2GB memory, 1.8V and 3.3V VDDIO (0°C~60°C)
SMARC-FiMX6-S-I	Freescale i.MX6 Solo Core 800MHz with 512MB memory, 1.8V and 3.3V VDDIO (-40°C~85°C)
SMARC-FiMX6-Q-1G-I	Freescale i.MX6 Quad Core 800MHz with 1GB memory, 1.8V and 3.3V VDDIO (-40°C~85°C)
SMARC-FiMX7-S	Freescale i.MX7 Solo Core 800MHz with 512MB memory, 1.8V VDDIO (-20°C~85°C)
SMARC-FiMX7-D	Freescale i.MX7 Dual Core1.2GHz with 1GB memory, 1.8V VDDIO (-20°C~85°C)

Introduction

This Chapter gives background information on the *EVK-STD-CARRIER-S20* Evaluation Carrier
Section include：

- *EVK-STD-CARRIER-S20* Evaluation Carrier Goals
- Feature Set Overview
- Block Diagram
- Peripheral Overview
- Layout Diagram
- Document and Standard References

Chapter 1 Introduction

This document serves as a user manual and technical reference for the *EMBEDIAN EVK-STD-CARRIER-S20* Evaluation Baseboard. The manual is intended for use by engineering personnel working with *SMARC 2.0* modules. It will be very helpful if developers can refer together with the carrier board schematics. *EVK-STD-CARRIER-S20* accepts *SMARC* 2.0 compliant modules.

1.1 EVK-STD-CARRIER-S20 Evaluation Carrier Goals

EMBEDIAN EVK-STD-CARRIER-S20 evaluation carrier is equipped with all mechanical and electrical components necessary for the rapid start-up of the SMARC compliant computer on module. The *EVK-STD-CARRIER-S20* is designed for evaluation, testing and prototyping of the *SMARC* modules in development environments prior to use in customer designed applications. It can also be used together with *SMARC* module as an “application ready” *mini-ITX* single board computer.

The *EVK-STD-CARRIER-S20* Evaluation Carrier is intended to serve multiple needs and summarized as followed:

- *SMARC 2.0* Module bring-up platform for hardware and software development.
- Module validation platform.
- Customer evaluation platform.
- Customer design reference.
- Manufacturing test platform.
- Flexible prototyping vehicle (facilitated by multiple mezzanines).
- An “application ready” single board computer. (together with *SMARC 2.0* module)

1.2 Feature Set Overview

The *EVK-STD-CARRIER-S20* has the following features for supporting the *SMARC* 2.0 modules:

Computer on Module	SMARC 2.0 Compliant Module	
Graphic	HDMI	1 x HDMI Type A
	LVDS	1 dual-channel 24-bit LVDS
	Display Port	1 Display Port Connector
Ethernet	10/100/1000Mbps	2 RJ45 with GBE transformer
Storage	EEPROM	Onboard AT24C32 EEPROM
	SD	1 SD card slot
	SATA	1 SATAII Connector (with SATA-DOM support)
IO	USB	2 USB 3.0 Type A, 2 USB 2.0 Type A, 2 USB 2.0 to mini PCIeB and mini PCIeC, 1 USB OTG mini Type AB
	UART	4 RS232 Ports (two of them can be configured as RS422/4845)
	Audio	3.5mm Audio Jack (Headphone and Microphone, SGTL5000 Audio Codec)
	Camera input	2 MIPI Connectors (2 LANEs and 4 LANEs)
	CAN	2 CAN 2.0B ports, Differential mode +5V
	GPIO	12 GPIO Ports
	I2C	I2C_GP, I2C_CAM0 and I2C_CAM1 pin header
	SPI	2 SPI0 pin header with 2 chip selects for each port
	ESPI	2 ESPI1 pin header with 2 chip selects for each port
Expansion	PCIe	1 PCIe x4 and 2 mini PCIe Slots
Communication	SIM Card Holder	2 for 2.5G/3G mini-PCIe Card

Computer on Module	SMARC v1.0 and v1.1 Compliant Module	
Power Input	Power	Power Inputs (+12V~+24V DC-Jack, Lithium-ion battery socket)
Physical Characters	Dimensions	170mm x 170mm (mini-ITX form factor)

1.3 Block Diagram

An overall system block diagram for the *EVK-STD-CARRIER-S20* Evaluation Carrier is shown on the following page. The following color coding is used on the block diagram:

- Industry standard wired I/O connectors are shown in orange.
- Embedian defined wired I/O connectors and headers are shown in red.
- Industry standard mezzanine and slot format connectors are shown in blue.
- ICs on the board are shown in pale yellow.
- Miscellaneous features (jumpers, switches) are shown in drab green.

Much may be gleaned from this diagram:

- How SMARC resources are used on the Evaluation Carrier.
- What the major Evaluation Carrier Features are.
- An indication of the power supply architecture.

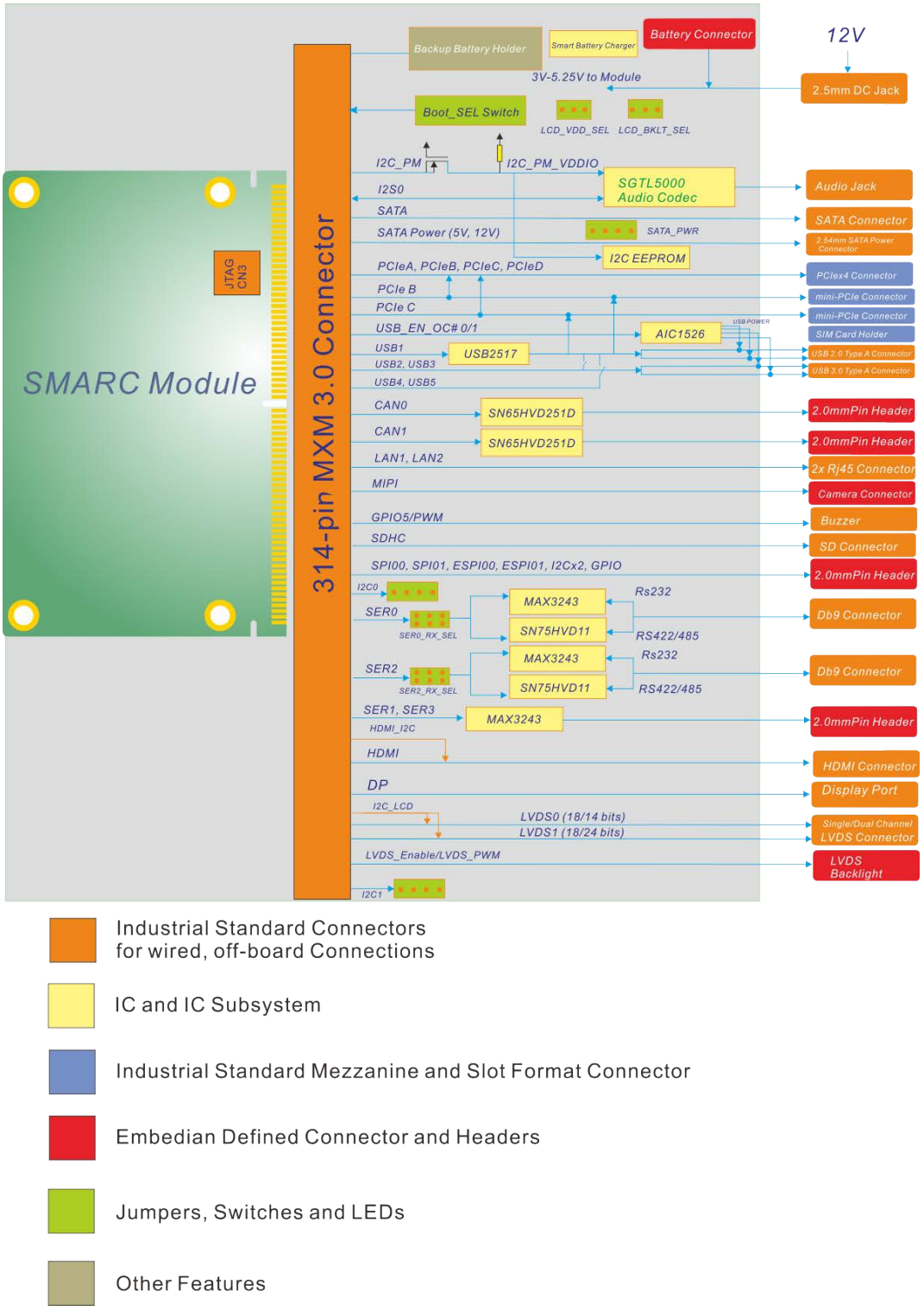


Figure 1: EVK-STD-CARRIER-S20 Evaluation Carrier Block Diagram

Details for this diagram will be explained in the following chapters.

1.4 Peripheral Overview

The following diagram shows the function of all peripherals including of connectors, headers, configuration jumpers and other important features on the *EVK-STD-CARRIER-S20* Evaluation Carrier.

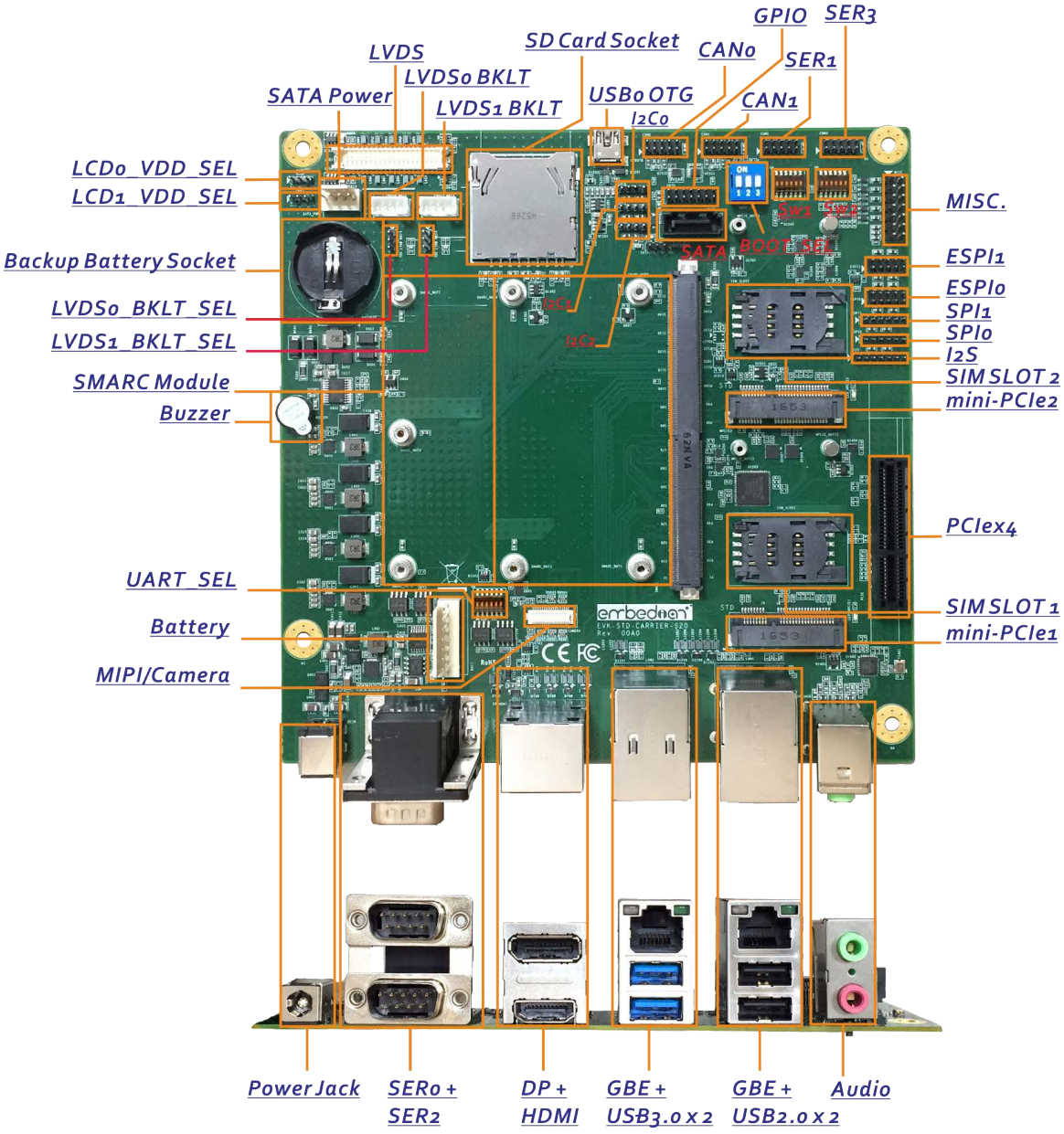


Figure 2: EVK-STD-CARRIER-S20 Peripheral Diagram

1.5 Layout Diagram

The following section shows the physical location and reference designator of connectors, configuration jumpers and other important features on the *EVK-STD-CARRIER-S20* Evaluation Carrier.

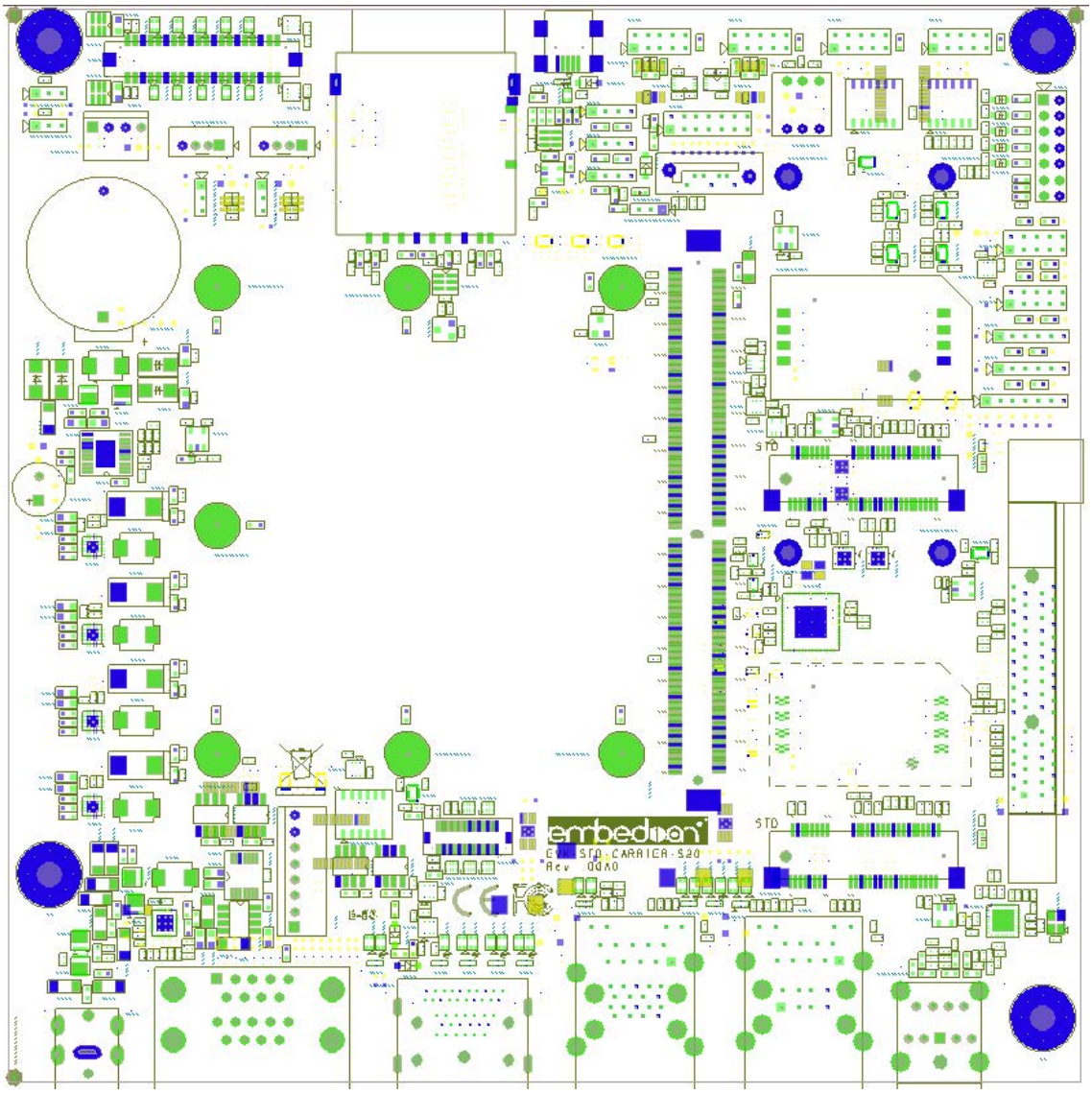


Figure 3: EVK-STD-CARRIER-S20 Connectors, Headers and Jumpers

1.6 Mounting Holes Mechanical Drawing

Figure 4 shows the mounting holes information of *EVK-STD-CARRIER-S20*. The diameter of mounting hole is 3.96mm and the diameter of the ring is 6mm.

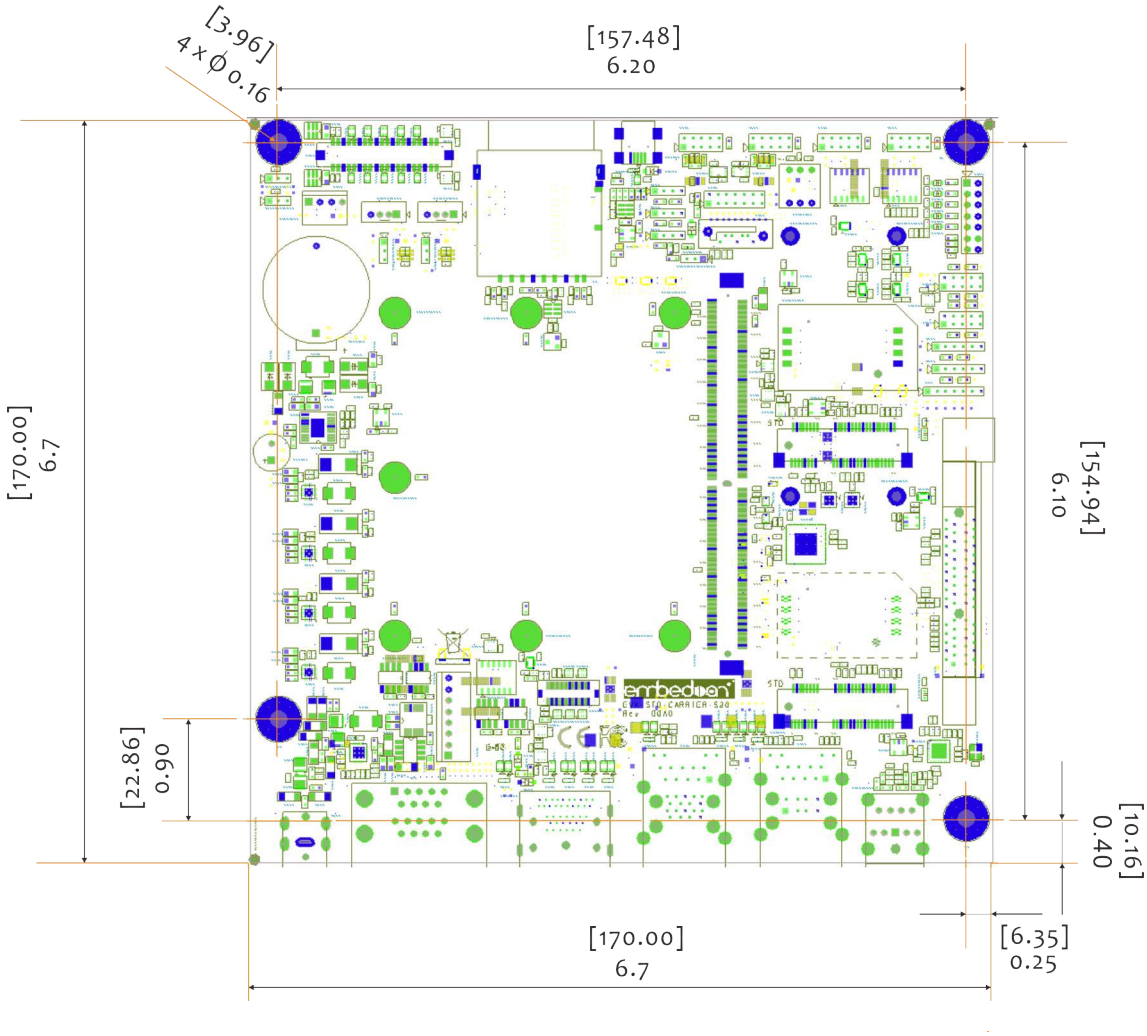


Figure 4: EVK-STD-CARRIER-S20 Mounting Holes Mechanical Drawing Information

1.7 Document and Standard References

1.7.1. External Industry Standard Documents

- ***eMMC (Embedded Multi-Media Card)*** the eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (www.jedec.org).
- ***The I2C Specification,*** Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com).
- ***I2S Bus Specification,*** Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com).
- ***JTAG (Joint Test Action Group*** defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (www.ieee.org).
- ***CAN ("Controller Area Network") Bus Standards*** – ISO 11898, ISO 11992, SAE J2411
- ***HDMI Specification, Version 1.3a***, November 10, 2006 © 2006 Hitachi and other companies (www.hdmi.org)
- ***MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification,*** Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (www.mxm-sig.org).
- ***PICMG® EEEP Embedded EEPROM Specification,*** Rev. 1.0, August 2010 (www.picmg.org).
- ***GBE MDI ("Gigabit Ethernet Medium Dependent Interface")*** This is defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (www.ieee.org)
- ***SD Specifications Part 1 Physical Layer Simplified Specification,*** Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (www.sdcard.org).
- ***SPI Bus –*** "Serial Peripheral Interface" - de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia
- ***PICMG® EEEP Embedded EEPROM Specification,*** Rev. 1.0, August 2010(www.picmg.org)
- ***PCI Express Specifications (www.pci-sig.org)***
- ***Serial ATA Revision 3.1, July 18, 2011, Gold Revision***, © Serial ATA International Organization (www.sata-io.org)
- ***SPDIF (aka S/PDIF)*** ("Sony Philips Digital Interface)- IEC 60958-3
- ***USB Specifications*** (www.usb.org).
- **DisplayPort and Embedded DisplayPort**, These standards are owned and maintained by VESA ("Video Electronics Standards Association") (www.vesa.org)

1.7.2. SGET Documents

- ***SMARC_Hardware_Specification_V200***, version 2.0, June 2, 2016.
- ***SMARC_DG_V2***, SMARC Design Guide V2.0, March 23, 2017.

1.7.3. Embedian Documents

- ***SMARC_T335x Evaluation Carrier Board Schematic***, PDF and OrCAD format
- ***SMARC_T335x Evaluation Carrier Board User's Manual***
- ***SMARC_T335x Carrier Board Hardware Design Guide***
- ***EVK-STD-CARRIER-S20 Schematic***, PDF and OrCAD format
- ***SMARC_T335x User's Manual***
- ***SMARC-FiMX6 User's Manual***
- ***SMARC-FiMX7 User's Manual***

Jumpers, Switches, LEDs and EEPROM

This Chapter provides *EVK-STD-CARRIER-S20* jumpers, switches, *LEDs* and *EEPROM/eMMC* information.

Section include：

- Jumpers
- Switches
- LEDs
- EEPROM

Chapter 2 Jumpers, Switches, LEDs and EEPROM

This chapter gives detail information of the jumpers, switches, *LEDs* and *EEPROM/eMMC*.

2.1 Jumpers

The *EVK-STD-CARRIER-S20* has a number of jumpers that allow you to configure your system to suit your application. All use 2mm shorting blocks (shunts) to select settings. Turn off power to the *EVK-STD-CARRIER-S20* before changing the position of a shunt.

2.1.1. Jumper Location

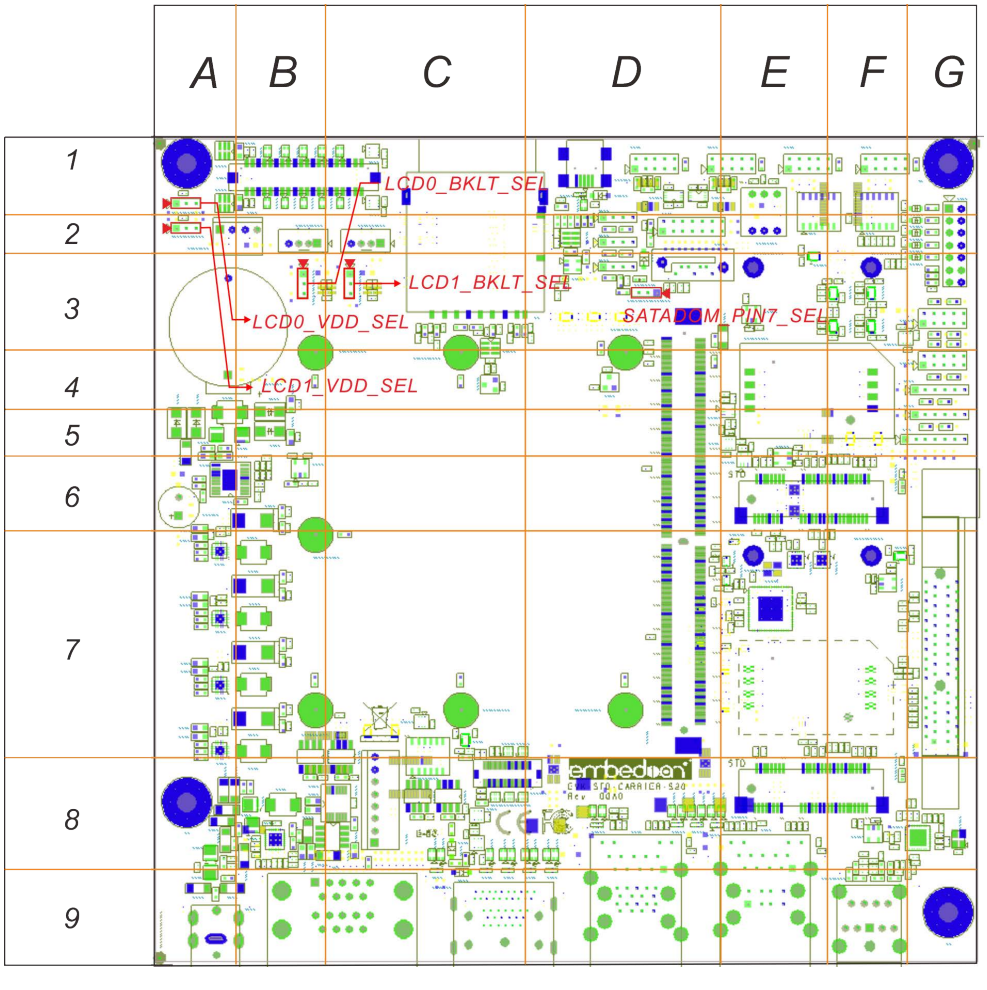


Figure 5: Jumper Locations

2.1.2. List of Jumpers

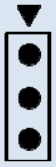
The table below lists the function of various jumpers.

Label	Function
LCD0_VDD_SEL	*3.3V/5V LVDS0 LCD Signaling Voltage*
LCD1_VDD_SEL	*3.3V/5V LVDS1 LCD Signaling Voltage*
LCD0_BKLT_SEL	*5V/12V LVDS0 LCD Backlight Voltage*
LCD1_BKLT_SEL	*5V/12V LVDS1 LCD Backlight Voltage*
SATADOM_PIN7_SEL	*GND/5V SATADOM Pin7 Selection*

2.1.3. Jumper Settings

The following tables describe how the jumper shunts to various configurations.

LCD0_VDD_SEL: *Location on Board, A1*

LCD0_VDD_SEL	3.3V/5V LCD Signaling Voltage	
	Setting	**Function**
	*LCD0_VDD_SEL (1-2)*	*3.3V*
	LCD0_VDD_SEL (2-3)	*5V*

LCD1_VDD_SEL: *Location on Board, A2*

LCD1_VDD_SEL	*3.3V/5V LCD Signaling Voltage*	
	Setting	***Function***
	*LCD1_VDD_SEL (1-2)*	*3.3V*
	LCD1_VDD_SEL (2-3)	*5V*

LCD0_BKLT_SEL: *Location on Board, B3*

LCD0_BKLT_SEL	*5V/12V LCD Backlight Voltage*	
	Setting	***Function***
	*LCD0_BKLT_SEL (1-2)*	*5V*
	LCD0_BKLT_SEL (2-3)	*12V*

LCD1_BKLT_SEL: *Location on Board, C3*

LCD1_BKLT_SEL	*5V/12V LCD Backlight Voltage*	
	Setting	***Function***
	*LCD1_BKLT_SEL (1-2)*	*5V*
	LCD1_BKLT_SEL (2-3)	*12V*

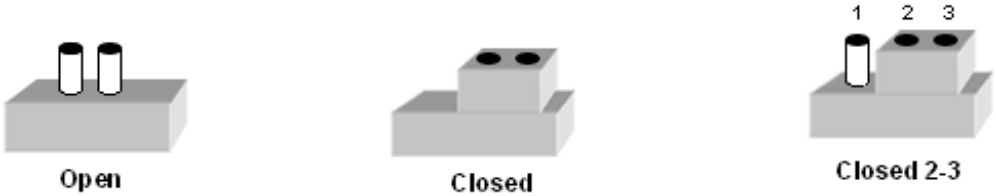
SATADOM_PIN7_SEL: *Location on Board, D3*

SATADOM_PIN7_SEL	*SATA-DOM Jumper (Power +5V pin7)*	
	Setting	***Function***
	*SATADOM_PIN7_SEL (1-2)*	*GND*
	SATADOM_PIN7_SEL (2-3)	*5V*

Make sure power is complete *OFF* when changing settings of *jumpers*.

2.1.4. Setting Jumpers

You configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip.
To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2 or 2 and 3.



The jumper settings are schematically depicted in this manual as follows.

A pair of needle-nose pliers may be helpful when working with jumpers. If you have any doubts about the best hardware configuration for your application, contact your sales representative before you make any change.

2.2 Switches

The *EVK-STD-CARRIER-S20* has some switches that allow you to switch signals to different paths.

2.2.1. Switch Location

The *BOOT_SEL* switch for boot configuration is located at *G4* as shown in the following figure.

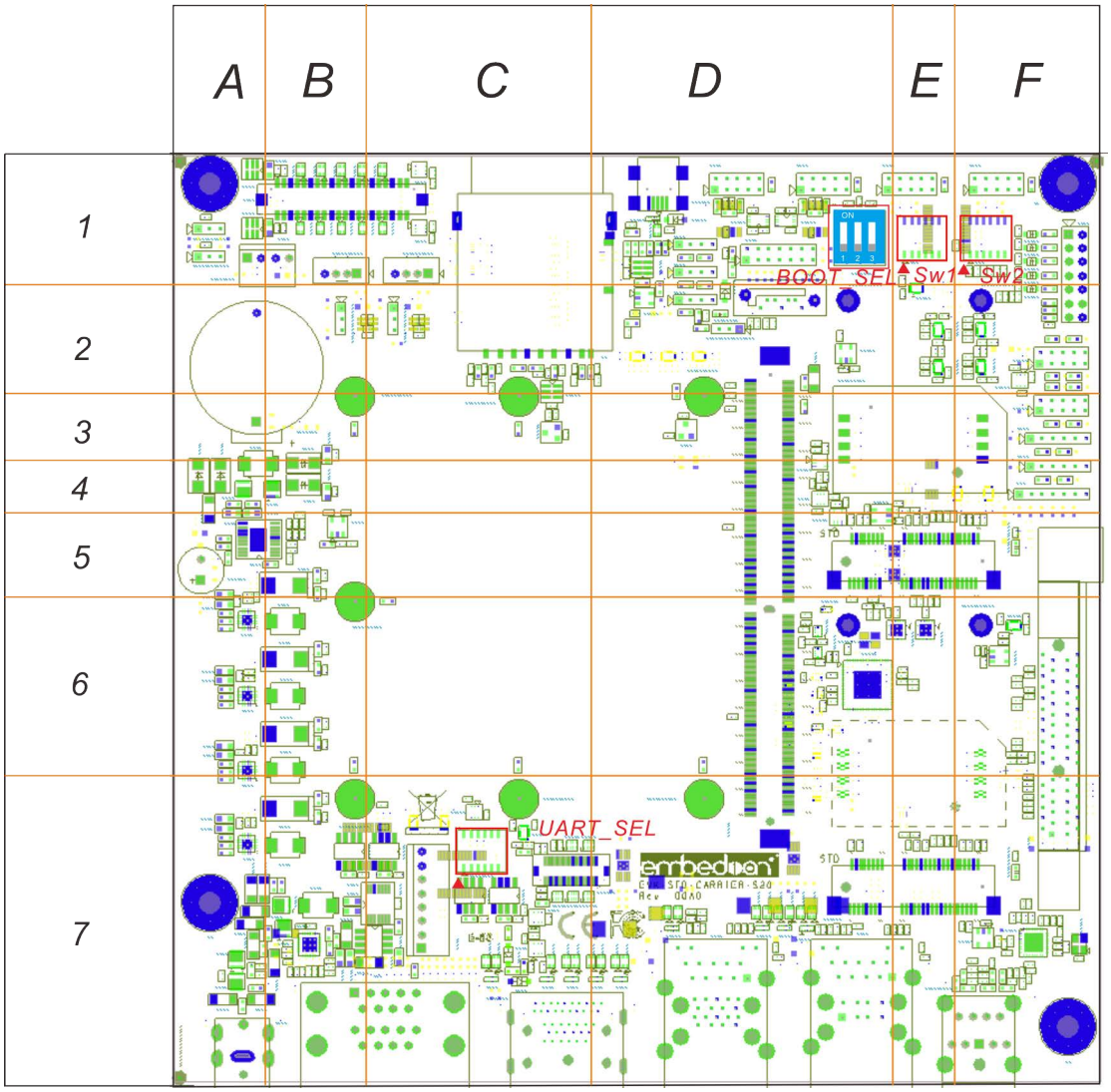


Figure 6: Switch Locations

2.2.2. List of Switches

The table below lists the function of various switches.

Label	Function
BOOT_SEL	*Boot up device selection*
UART_SEL	*SER0/SER2 RS232/RS422/RS485 Selection*
SW1	*Signals path for GPIO0~3, GPIO5, PCIe_B, PCIe_C, USB0 and USB1*
SW2	*Signals path for USB ports*

2.2.3. DIP Switch Settings

The following tables describe how the signals path related to switches settings are.

2.2.3.1 BOOT_SEL

The table below lists the booting device configuration setting by *BOOT_SEL*.

LCD0_VDD_SEL: *Location on Board, D1*

Boot_Sel			Function
1	2	3	Boot Configuration
OFF	OFF	OFF	Carrier SATA
ON	OFF	OFF	Carrier SD Card
OFF	ON	OFF	Carrier eMMC Flash
ON	ON	OFF	Carrier SPI
OFF	OFF	ON	Module Device (Vendor Specific)
ON	OFF	ON	Remote Boot (Vendor Specific)
OFF	ON	ON	Module eMMC Flash
ON	ON	ON	Module SPI

2.2.3.2 UART_SEL

UART_SEL: *Location on Board, C7*

UART_SEL	SER0/SER2 RS232/RS422/RS485 Selection		
	Pin	Switch	Signal Path
	1	ON	SER0 RS232 (Default)
		OFF	
	2	ON	SER0 RS422
		OFF	
	3	ON	SER0 RS485
		OFF	
	4	ON	SER2 RS232 (Default)
		OFF	
	5	ON	SER2 RS422
		OFF	
	6	ON	SER2 RS485
		OFF	

2.2.3.3 SW1

SW1: *Location on Board, E1*

SW1	Signals path for GPIO0~3, GPIO5, PCIe_B, PCIe_C, USB0 and USB1		
	Pin	Switch	Signal Path
	1	ON	GPIO0~GPIO3 to Camera Header
		OFF	GPIO0~GPIO3 to GPIO Header (Default)
	2	ON	GPIO5 to Buzzer Connector
		OFF	GPIO5 to GPIO Header (Default)
	3	ON	PCIe_B to mini-PCIe B (mini-PCIe1) Connector
		OFF	PCIe_B to PCIex4 Connector (Default)
	4	ON	PCIe_C to mini-PCIe C (mini-PCIe2) Connector
		OFF	PCIe_C to PCIex4 Connector (Default)
	5	ON	USB0 signals to rear-panel (GBE + USB2.0x2) connector lower port (port1 of SW2 should be ON)
		OFF	USB0 signals to OTG mini-type B Connector (Default)
	6	ON	USB1 to rear-panel (GBE + USB2.0x2) connector upper port (SW2 all ports need to be set ON, all USB signals are from golden finger connector)
		OFF	USB1 to USB2517 hub (Default, SW2 all ports need to be set OFF, all USB signals are from USB2517 hub)

2.2.3.4 SW2

SW2: *Location on Board, F1*

SW2	Signals path for USB ports		
	Pin	*Switch*	*Signal Path*
	*1*	*ON*	*USB signals on lower port of rear-panel (GBE + USB2.0x2) connector are from USB0 of golden finger connector*
		OFF	*USB signals on lower port of rear-panel (GBE + USB2.0x2) connector are from port1 of USB2517 hub (Default, port5 of SW1 should be OFF)*
	2	*ON*	*USB signals on upper port of rear-panel (GBE + USB2.0x2) connector are from USB1 of golden finger*
		OFF	*USB signals on upper port of rear-panel (GBE + USB2.0x2) connector are from port2 of USB2517 hub*
	3	*ON*	*USB signals on lower port of rear-panel (GBE + USB3.0x2) connector are from USB2 of golden finger connector*
		OFF	*USB signals on lower port of rear-panel (GBE + USB3.0x2) connector are from port3 of USB2517 hub (Default)*
	4	*ON*	*USB signals on upper port of rear-panel (GBE + USB3.0x2) connector are from USB3 of golden finger*
		OFF	*USB signals on upper port of rear-panel (GBE + USB3.0x2) connector are from port4 of USB2517 hub*
	5	*ON*	*USB signals on mini-PCIe_B connector are from USB4 of golden finger connector (Default)*
		OFF	*USB signals on mini-PCIe_B connector are from port5 of USB2517 hub (Default)*
	6	*ON*	*USB signals on mini-PCIe_C connector are from USB5 of golden finger connector (Default)*
		OFF	*USB signals on mini-PCIe_C connector are from port6 of USB2517 hub (Default)*

Note:

If port5 of *SW1* is *ON* and port1 of *SW2* is *OFF*, the *USB* signals on upper port of rear-panel *(GBE + USB2.0x2)* connector will be from port1 of *USB2517* hub.

2.3 LEDs

The *EVK-STD-CARRIER-S20* has one LED to indicate the *SATA_ACT#* signal and two LEDs to show if mini PCIes are activated. The *LED_SATA* plays a role as *SATA* activity indicator, LED_mPCI1 plays a role as mini-PCIe_B activity indicator and LED_mPCIe2 plays a role as mini-PCIe_C activity indicator

2.3.1. LED Location

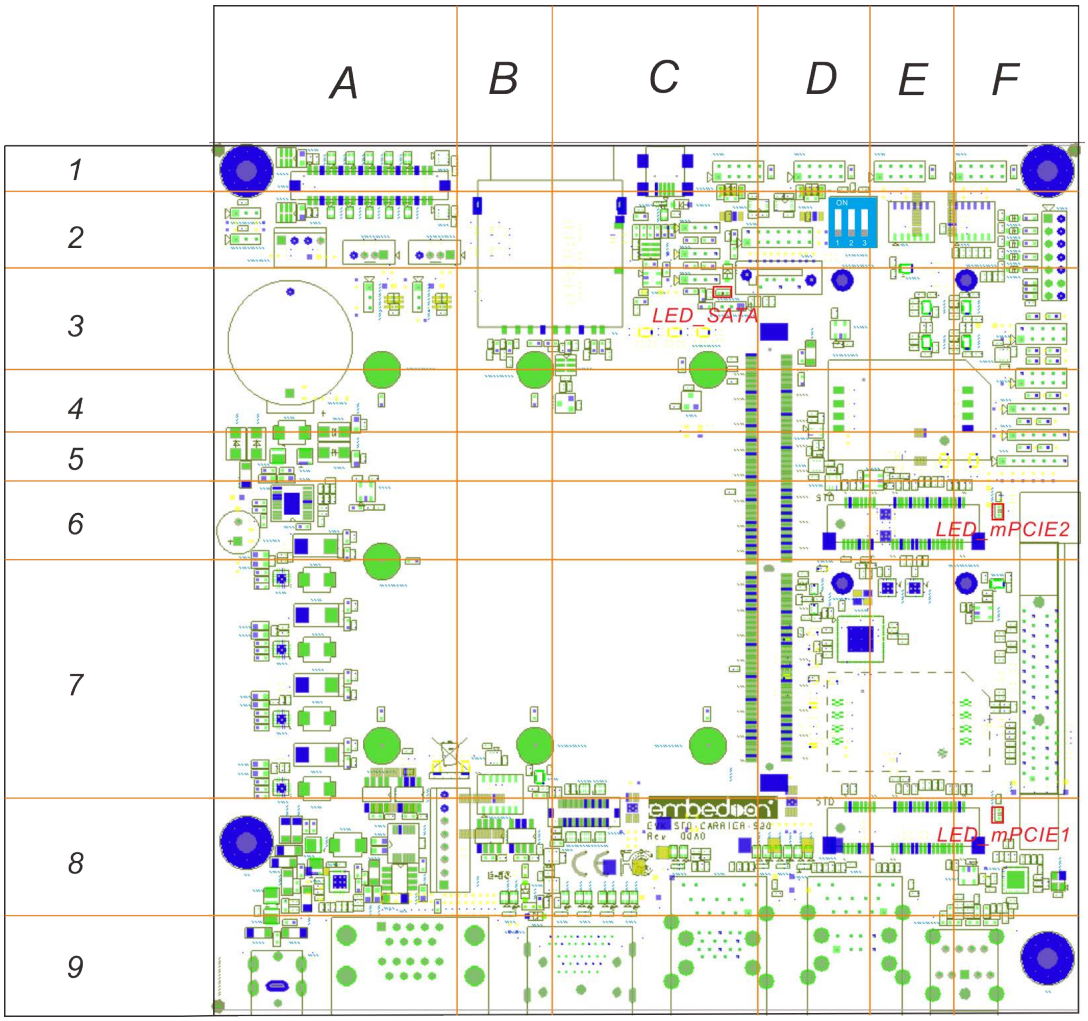


Figure 7: LED Locations

2.3.2. List of LEDs

The table below lists the function of LEDs.

Label	Function
LED_SATA	ON when there is activity on the SATA Lane
LED_mPCIE1	ON when there is activity on mini-PCIE_B
LED_mPCIe2	ON when there is activity on mini-PCIE_C

2.4 EEPROM

An *I2C AT24c32 EEPROM* is on *EVK-STD-CARRIER-S20* and is intended to retain carrier board parameter information, including a carrier serial number. The *I2C* bus is *I2C_PM* from *SMARC* module and address is *0x57*.

Rear I/O Panel and Internal I/O Headers

This Chapter gives *EVK-STD-CARRIER-S20* connectors and headers detail information.

Section include：

- Rear I/O Panel
- Internal I/O Headers

Chapter 3 Headers and Connectors

This section gives *EVK-STD-CARRIER-S20* connectors and headers detail information.

3.1 Rear I/O Panel

Rear panel I/O connectors of *EVK-STD-CARRIER-S20* Evaluation Carrier are described in this section.

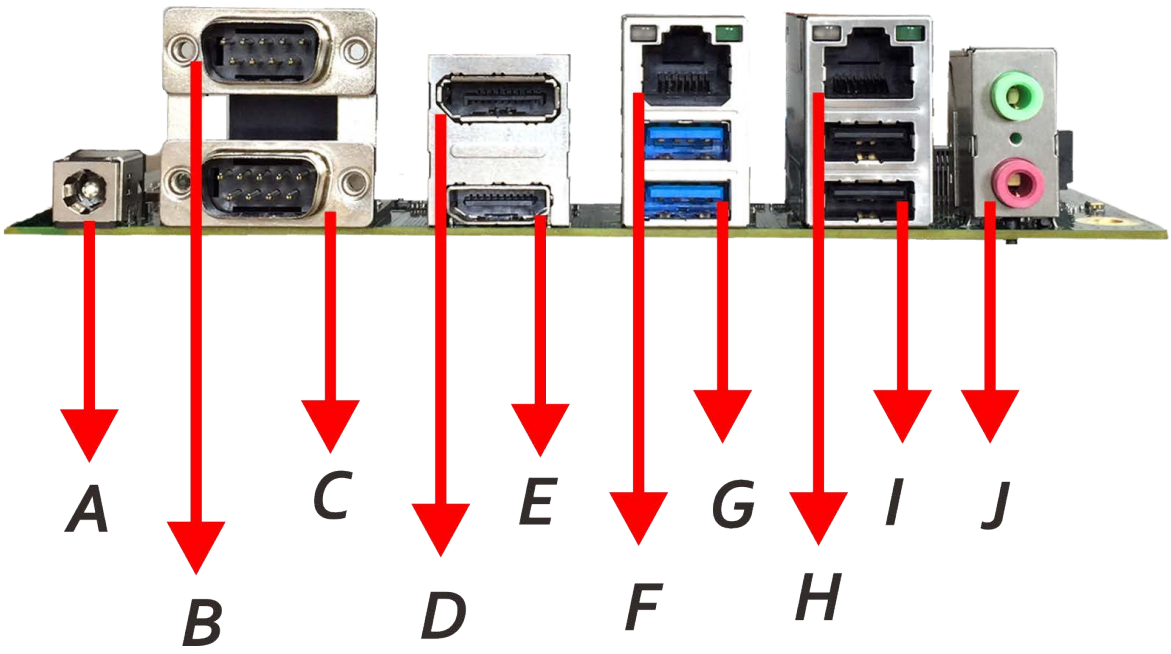


Figure 8: Rear I/O Connectors

3.1.1. List of Connectors

The table below lists the function of various connectors.

Label	Location	Description	Connector Type
DC_IN	**A**	*12V~24V Power Input DC Jack*	*DC POWER JACK 2.5mm 90D(M) DIP 2DCG213B200*
COMA	**B**	*UART Port 0*	*D-Sub 9M/9M Dual port*
COMB	**C**	*UART Port 2*	*D-Sub 9M/9M Dual port*
DP	**D**	*Display Port*	*Display Port Over HDMI Combo Connector*
HDMI	**E**	*HDMI Port*	*Display Port Over HDMI Combo Connector*
LAN1 + USB3.0 x2	**F G**	*GbE1 Ethernet RJ45 and dual USB 3.0 Host Type A Connector*	*RJ45 Tab up over USB 3.0 stack 10/100/1000 Base-T LED: L-G/0; R-G*
LAN0 + USB2.0 x2	**H I**	*GbE0 Ethernet RJ45 and dual USB 2.0 Host Type A Connector*	*RJ45 Tab up over USB 2.0 stack 10/100/1000 Base-T LED: L-G/0; R-G*
PhoneJack	**J**	*Mic. Input / Headphone Output*	*3.5mm Phone jack 90 2x01*

3.1.2. Connector Pin Assignments

The following tables describe the electrical signals available on the connectors of the *EVK-STD-CARRIER-S20*. Each section provides relevant details about the connector including part numbers, mating connectors, signal descriptions and references to related chapters.

Pinout Legend

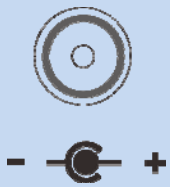
I	*Input*
O	*Output*
I/O	*Input or output*
P	*Power*
AI	*Analogue input*
AO	*Analogue output*
AIO	*Analogue Input or analogue output*
OD	*Open Drain Signal*
#	*Low level active signal*

3.1.2.1. DC Jack Power Input Connector: DC_IN

EVK-STD-CARRIER-S20 accepts DC +12V ~ DC +24V as the power input source. The power supply to SMARC CPU module is 5V via a power management IC on *EVK-STD-CARRIER-S20*.

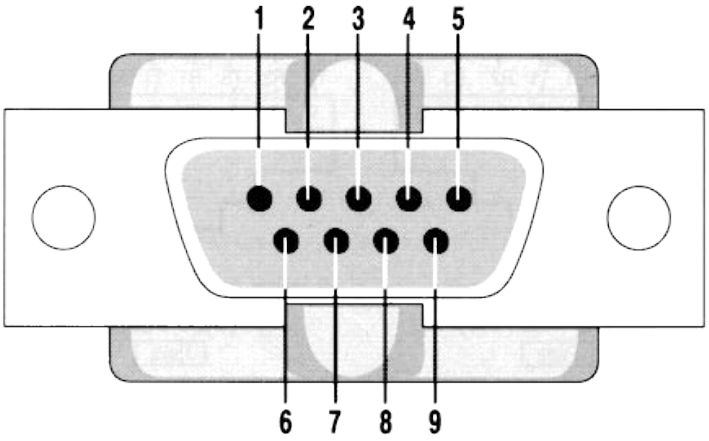
The following table shows the pin-out of the *DC_IN* power jack connector.

DC_IN: *Location on Board, A*

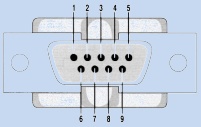
	12~24V DC Jack Power Input			***Edge Finger***	***Type***
	DC POWER JACK 2.5mm 90D(M) DIP 2DCG213B200				
Header	*Pin*	*Signal Name*	*Function*	*Pin#*	
	*1*	*12V~24V*	*DC 12V~24V Power Input*	*-*	*P*
	2	*Shield*	*Ground Power*	*-*	*P*

3.1.2.2. RS232/422/485 Port 0 Connector (4-Wire): COMA

The following table shows the pin-out of the *COMA* connector.

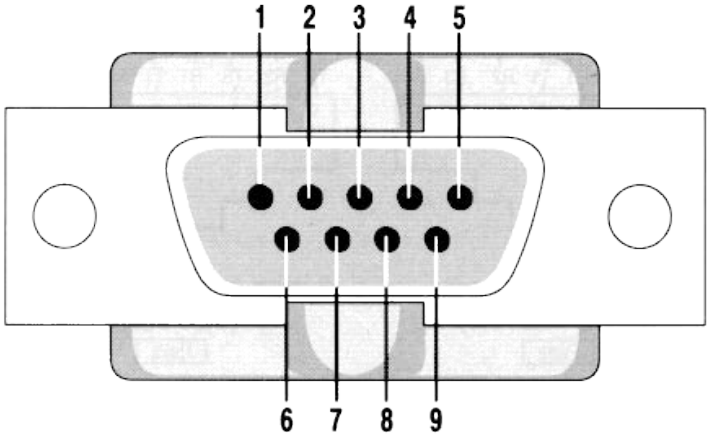


COMA: *Location on Board, B*

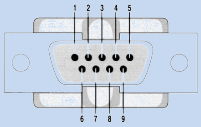
	RS232/422/485 Port0 Connector D-Sub 9M/9M Dual port (Up)			Edge Finger	Type
Header	Pin	Signal Name	Function	Pin#	
	1	RS422_0_TX+/ RS485_0_RX+		-	
	2	COM0_RXD	Receive Data	P130	I
	3	COM0_TXD	Transmit Data	P129	O
	4	RS422_0_RX+		-	
	5	GND		-	
	6	RS422_0_TX-/ RS485_0_RX-		-	
	7	COM0_RTS	Ready to Send	P131	O
	8	COM0_CTS	Clear To Send	P132	I
	9	RS422_0_RX-		-	

3.1.2.3. RS232/422/485 Port 2 Connector (4-Wire): COMB

The following table shows the pin-out of the *COMB* connector.

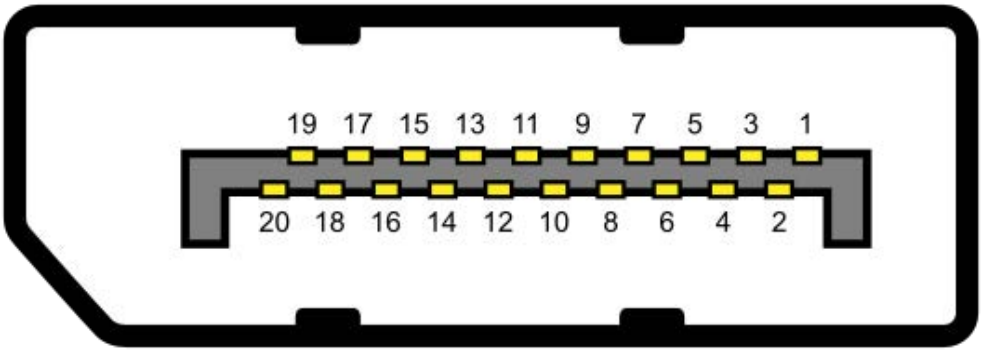


COMA: *Location on Board, C*

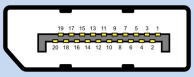
	RS232/422/485 Port2 Connector D-Sub 9M/9M Dual port (Down)			Edge Finger	Type
Header	Pin	Signal Name	Function	Pin#	
	1	RS422_2_TX+/ RS485_2_RX+		-	
	2	COM2_RXD	Receive Data	P137	I
	3	COM2_TXD	Transmit Data	P136	O
	4	RS422_2_RX+		-	
	5	GND		-	
	6	RS422_2_TX-/ RS485_2_RX-		-	
	7	COM2_RTS	Ready to Send	P138	O
	8	COM2_CTS	Clear To Send	P139	I
	9	RS422_2_RX-		-	

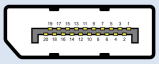
3.1.2.4. DisplayPort Connector: DP

The following table shows the pin-out of the *DisplayPort* connector.



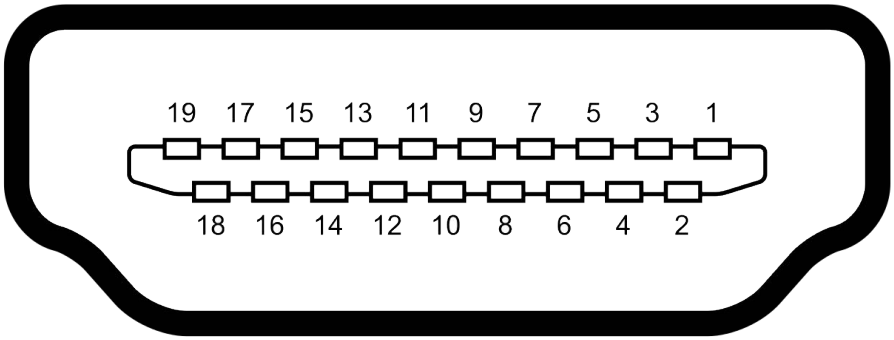
DP: *Location on Board, D*

	DisplayPort Connector Display Port Over HDMI Combo Connector			Edge Finger	Type
Header	Pin	Signal Name	Function	Pin#	
	1	ML_LANE0+	DisplayPort differential pair lines 0+	S93	AO
	2	GND	Ground		P
	3	ML_LANE0-	DisplayPort differential pair lines 0-	S94	AO
	4	ML_LANE1+	DisplayPort differential pair lines 1+	S96	AO
	5	GND	Ground		P
	6	ML_LANE1-	DisplayPort differential pair lines 1-	S97	AO
	7	ML_LANE2+	DisplayPort differential pair lines 2+	S99	AO
	8	GND	Ground		P
	9	ML_LANE2-	DisplayPort differential pair lines 2-	S100	AO
	10	ML_LANE3+	DisplayPort differential pair lines 3+	S102	AO
	11	GND	Ground		P
	12	ML_LANE3-	DisplayPort differential pair lines 3-	S103	AO

Header	DisplayPort Connector Display Port Over HDMI Combo Connector Pin	Signal Name	Function	Edge Finger Pin#	Type
	13	CONFIG1	Connected to Ground		
	14	CONFIG2	Connected to Ground		
	15	AUX_CH+	Auxiliary channel used for link management and device control. Differential pair lines.	S105	IO
	16	GND	Ground		P
	17	AUX_CH-	Auxiliary channel used for link management and device control. Differential pair lines.	S106	IO
	18	DP_HDP	Hot plug detection signal.	S98	I
	19	DP_PWR_RETURN	Return for Power		P
	20	DP_PWR	Power for Connector (3.3V 500mA)		P

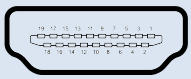
3.1.2.5. HDMI Connector: HDMI

The following table shows the pin-out of the *HDMI* connector.



HDMI: *Location on Board, E*

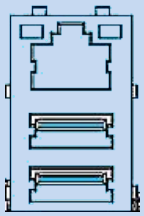
	HDMI Connector Display Port Over HDMI Combo Connector			Edge Finger	Type
Header	Pin	Signal Name	Function	Pin#	
	1	TMDS_D2+	TMDS / HDMI data differential pair 2	P92	O
	2	GND	Ground	-	P
	3	TMDS_D2-	TMDS / HDMI data differential pair 2	P93	O
	4	TDMS_D1+	TMDS / HDMI data differential pair 1	P95	O
	5	GND	Ground	-	P
	6	TMDS_D1-	TMDS / HDMI data differential pair 1	P96	O
	7	TMDS_D0+	TMDS / HDMI data differential pair 0	P98	O
	8	GND	Ground	-	P
	9	TMDS_D0-	TMDS / HDMI data differential pair 0	P99	O
	10	TMDS_CK+	HDMI differential clock output pair	P101	O
	11	GND	Ground	-	P
	12	TMDS_CK-	HDMI differential clock output pair	P102	O

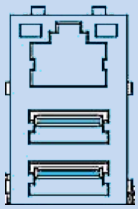
Header	HDMI Connector Display Port Over HDMI Combo Connector Pin	Signal Name	Function	Edge Finger Pin#	Type
	13	CEC	HDMI Consumer Electronics Control 1-wire peripheral control interface	P107	IO/ OD
	14	-	-	-	-
	15	SCL	I2C Clock	P105	IO/ OD
	16	SDA	I2C Data	P106	IO/ OD
	17	GND	Ground	-	P
	18	+5V	5V Power	-	P
	19	HPD	HDMI Hot Plug Detect input	P104	I

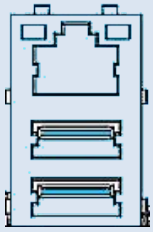
3.1.2.6. RJ45 & USB 3.0 Connector: LAN1 + USB3.0 x2

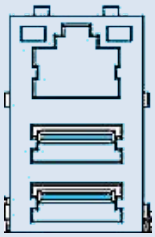
The *USB* signals can be originated from golden finger connector directly (*USB2 and USB3*) or from USB1 port of SMARC module connecting to a 7-port USB hub *USB2517* from Microchip depending on the configurations of SW1 and SW2 DIP switch. The reason for this design is because many ARM Cortex SOCs only have two USB ports.
Two ports are present in this (*LAN1+USB3.0x2*) connector. The other four ports are present at (*LAN0+USB2.0x2*) and mini-PCIE connectors. A *GigaLAN* magnet is built in the RJ45 connector.
The following table shows the pin-out of the *LAN1+USB3.0x2* connector.

LAN1+USB3.0x2: *Location on Board, F, G*

	LAN1+USB3.0x2 Connector ***RJ45 Tab up over USB 3.0 stack 10/100/1000 Base-T*** ***LED: L-G/0; R-G***			***Edge Finger***	***Type***
Header	*Pin*	*Signal Name*	*Function*	*Pin#*	
	LAN1+USBA (RJ45)				
	1	*GBE1_CTREF*	*Center tap reference voltage for GBE1 Carrier board Ethernet magnetic*	*S28*	*O*
	*2*	*GBE1_MDI0+*	*Differential Transmit/Receive Positive Channel 0*	*S17*	*AIO*
	3	*GBE1_MDI0-*	*Differential Transmit/Receive Negative Channel 0*	*S18*	*AIO*
	4	*GBE1_MDI1+*	*Differential Transmit/Receive Positive Channel 1*	*S20*	*AIO*
	5	*GBE1_MDI1-*	*Differential Transmit/Receive Negative Channel 1*	*S21*	*AIO*
	6	*GBE1_MDI2+*	*Differential Transmit/Receive Positive Channel 2*	*S23*	*AIO*
	7	*GBE1_MDI2-*	*Differential Transmit/Receive Negative Channel 2*	*S24*	*AIO*

Header	LAN1+USB3.0x2 Connector RJ45 Tab up over USB 3.0 stack 10/100/1000 Base-T LED: L-G/0; R-G			Edge Finger	Type
	Pin	Signal Name	Function	Pin#	
	LAN1+USBA (RJ45)				
	8	GBE1_MDI3+	Differential Transmit/Receive Positive Channel 3	S26	AIO
	9	GBE1_MDI3-	Differential Transmit/Receive Negative Channel 3	S27	AIO
	10	GND	Ground	-	P
	11	GBE1_LINK_ACK#	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps)	S31	O OD
	12	3.3V	3.3V Power	-	P
	13	GBE1_LINK1000#	Link Speed Indication LED for 1000Mbps	S22	O OD
	14	GBE1_LINK100#	Link Speed Indication LED for 100Mbps	S21	O OD

Header	LAN1+USB3.0x2 Connector RJ45 Tab up over USB 3.0 stack 10/100/1000 Base-T LED: L-G/0; R-G			Edge Finger	Type
	Pin	Signal Name	Function	Pin#	
	LAN1_USBB (USB Port 2)				
	15	5V	USB 2 Power Supply		P
	16	USB2_D-/ HUB_DN3_D-	Universal serial bus port 2 (-)	P70	IO
	17	USB2_D+/ HUB_DN3_D+	Universal serial bus port 2 (+)	P69	IO
	18	GND	Ground		P
	19	USB2_SSRX-	Receive signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are off-Module	S75	I
	20	USB2_SSRX+	Receive signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are off-Module	S74	I
	21	GND	Ground		P
	22	USB2_SSTX-	Transmit signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are off-Module	S72	O
	23	USB2_SSTX+	Transmit signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are off-Module	S71	O
	24	Shield	Shield		P

Header	LAN1+USB3.0x2 Connector RJ45 Tab up over USB 3.0 stack 10/100/1000 Base-T LED: L-G/0; R-G			Edge Finger	Type
	Pin	Signal Name	Function	Pin#	
	LAN1_USBC (USB Port 3)				
	25	5V	USB 3 Power Supply		
	26	USB3_D-/ HUB_DN4_D-	Universal serial bus port 3 (-)	S69	
	27	USB3_D+/ HUB_DN4_D+	Universal serial bus port 3 (+)	S68	
	28	GND	Ground		
	29	US3_SSRX-	Receive signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are off-Module	S66	I
	30	USB3_SSRX+	Receive signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are off-Module	S65	I
	31	GND	Ground		P
	32	USB3_SSTX-	Transmit signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are off-Module	S63	O
	33	USB3_SSTX+	Transmit signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are off-Module	S62	O
	34	Shield	Shield		P

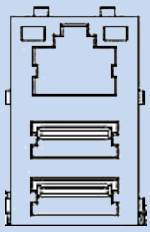
Note:

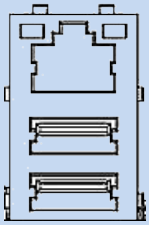
The signals of GBE1 port in the connector are originated from the 2nd defined GBE port from SMARC spec.

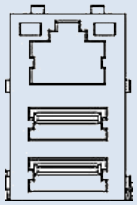
3.1.2.7. RJ45 & USB 2.0 Connector: LAN0 + USB2.0 x2

Two ports are present in this (*LAN0+USB2.0x2*) connector. The other four ports are present at (*LAN1+USB3.0x2*) and mini-PCIE connectors. A GigaLAN magnet is built in the RJ45 connector.
The following table shows the pin-out of the *LAN0+USB2.0x2* connector.

LAN0+USB2.0x2: *Location on Board, H, I*

	LAN0+USB2.0x2 Connector ***RJ45 Tab up over USB 2.0 stack 10/100/1000 Base-T*** ***LED: L-G/0; R-G***			***Edge Finger***	***Type***
Header	*Pin*	*Signal Name*	*Function*	*Pin#*	
	*LAN0+USBA (RJ45)*				
	1	*GBE_CTREF*	*Center tap reference voltage for GBE Carrier board Ethernet magnetic*	*P28*	*O*
	2	*GBE_MDI0+*	*Differential Transmit/Receive Positive Channel 0*	*P30*	*AIO*
	3	*GBE_MDI0-*	*Differential Transmit/Receive Negative Channel 0*	*P29*	*AIO*
	4	*GBE_MDI1+*	*Differential Transmit/Receive Positive Channel 1*	*P27*	*AIO*
	5	*GBE_MDI1-*	*Differential Transmit/Receive Negative Channel 1*	*P26*	*AIO*
	6	*GBE_MDI2+*	*Differential Transmit/Receive Positive Channel 2*	*P24*	*AIO*
	7	*GBE_MDI2-*	*Differential Transmit/Receive Negative Channel 2*	*P23*	*AIO*
	8	*GBE_MDI3+*	*Differential Transmit/Receive Positive Channel 3*	*P20*	*AIO*
	9	*GBE_MDI3-*	*Differential Transmit/Receive Negative Channel 3*	*P19*	*AIO*
	10	*GND*	*Ground*	*-*	*P*

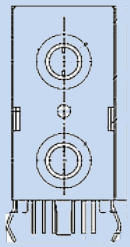
Header	LA0N+USB2.0x2 Connector RJ45 Tab up over USB 2.0 stack 10/100/1000 Base-T LED: L-G/0; R-G			Edge Finger	Type
	Pin	Signal Name	Function	Pin#	
	LAN0+USBA (RJ45)				
	11	GBE_LINK_ACK#	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps)	P25	O OD
	12	3.3V	3.3V Power	-	P
	13	GBE_LINK1000#	Link Speed Indication LED for 1000Mbps	P22	O OD
	14	GBE_LINK100#	Link Speed Indication LED for 100Mbps	P21	O OD

Header	Pin	Signal Name	Function	Edge Finger Pin#	Type
	LAN+USB Connector **RJ45 Tab up over USB 2.0 stack 10/100/1000 Base-T** **LED: L-G/0; R-G**				
		*LAN0_USBB (USB Port0)*			
	15	5V	USB 1 Power Supply	-	P
	16	USB0_D-/ HUB_DN1_D-	Universal serial bus port 0 (-)	-	IO
	17	USB0_D+/ HUB_DN1_D+	Universal serial bus port 0 (+)	-	IO
	18	GND	Ground	-	P
		LAN0_USBC (USB Port 1)			
	19	5V	USB 2 Power Supply	-	
	20	USB1_D-/ HUB_DN2_D-	Universal serial bus port 1 (-)	-	
	21	USB1_D+/ HUB_DN2_D+	Universal serial bus port 1 (+)	-	
	22	GND	Ground	-	

3.1.2.8. Audio Connector: PhoneJack

The following table shows the pin-out of the *PhoneJack* connector.

PhoneJack: *Location on Board, J*

Header	PhoneJack Connector 3.5mm Phone jack 90 2x01 Pin	Signal Name	Function	Edge Finger Pin#	Type
	1	GND	Ground	-	P
	2	-	-	-	-
	3	-	-	-	-
	4	-	-	--	-
	5	MIC In.	Microphone Input	-	AI
	6	-	-		
	7	Adio_L	Left channel of headset speaker	-	AO
	8	-	-	-	
	9	Audio_R	Right channel of headset speaker		AO

3.2 Internal I/O Headers

This section details the internal I/O header and connector information of *EVK-STD-CARRIER-S20* Evaluation Carrier.

3.2.1. Location

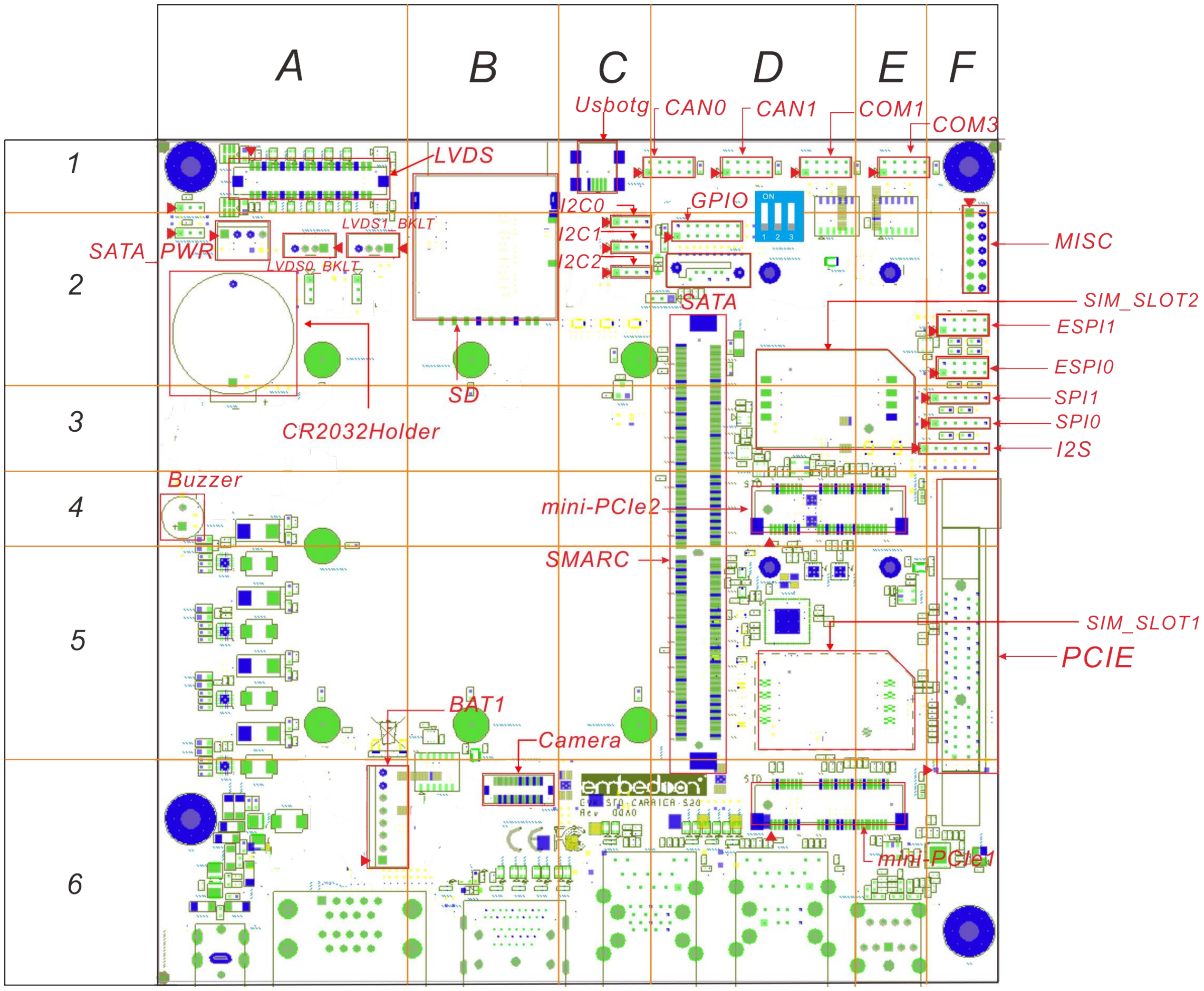


Figure 9: Internal I/O Header Locations

3.2.2. List of Headers

The table below lists the function of various headers.

Label	Description	Connector Type
BAT1	Lithium-ion Battery power input pin header	WAFER 8P 2.54mm 180D(M) DIP A2543WV2-8P
Camera	2 LANEs and 4 LANEs Camera Connector	B/B CONN. 2x20P 0.5mm 180D(M) SMD DF12(3.0)-40D
SATA	SATA Connector	Serial ATA 7P 1.27mm 180D(M) DIP WATM-07DBN4A3B8
SATA_PWR	SATA Power Connector	WAFER 4P 2.5mm 180D(M) DIP 24W1161-04S10-01T
PCIEx4	PCIex4 Connector	PCIEXPRESS 64P 180D(F) DIP 2EG01817-D2D-DF
Mini-PCIE1	PCI Express Mini Card	0.80mm Pitch, 5.20mm Height, PCI Express* Mini Card, 52 Circuit, Right Angle, Surface Mount, 0.25µm Gold (Au) Plating
Mini-PCIE2	PCI Express Mini Card	0.80mm Pitch, 5.20mm Height, PCI Express* Mini Card, 52 Circuit, Right Angle, Surface Mount, 0.25µm Gold (Au) Plating
SIM_SLOT1/ SIM_SLOT2	SIM Card Holder	Sim card hinged lock
LVDS	LVDS Connector	B/B Conn. 40P 1.25mm 90D SMD DF13-40DP-1.25V(91)
LVDS0_BKLT/ LVDS1_BKLT	LVDS Backlight Power	WAFER BOX 2.0mm 4P 180D(M) DIP WO/Pb JIH VEI
SD	SD/SDHC Connector	Right Angle, SMT, 2.75mm height, Push Push Normal Type With Detect Switch

Label	Description	Connector Type
Usbotg	USB OTG Connector	USB OTG mini Type B Connector
SPI0	SPI0 CS0 Pin Header	PIN HEADER 1x6P 2.00mm 180D(M) SMD
SPI01	SPI0 CS1 Pin Header	PIN HEADER 1x6P 2.00mm 180D(M) SMD
ESPI0	ESPI1 CS0 Pin Header	PIN HEADER 2x5P 2.00mm 180D(M) SMD
ESPI1	SPI1 CS1 Pin Header	PIN HEADER 2x5P 2.00mm 180D(M) SMD
I2S	I2S1 and I2S2 Pin Header	PIN HEADER 1x7P 2.00mm 180D(M) SMD
GPIO	GPIO Pin Header	PIN HEADER 2x7P 2.00mm 180D(M) SMD
MISC	Misc. Signals Pin Header	PIN HEADER 2x7P 2.54mm 180D(M) SMD
CAN0	CAN0 Bus Pin Header	PIN HEADER 2x5P 2.00mm 180D(M) SMD
CAN1	CAN1 Bus Pin Header	PIN HEADER 2x5P 2.00mm 180D(M) SMD
COM1	SER1 RS232 Pin Header	PIN HEADER 2x5P 2.00mm 180D(M) SMD
COM3	SER3 RS232 Pin Header	PIN HEADER 2x5P 2.00mm 180D(M) SMD
Buzzer	Buzzer Connector	ELECTRO MAGNETIC BUZZER

Label	Description	Connector Type
I2C0	I2C_GP Pin Header	PIN HEADER 1x4P 2.00mm 180D(M) SMD
I2C1	I2C_CAM0 Pin Header	PIN HEADER 1x4P 2.00mm 180D(M) SMD
I2C2	I2C_CAM1 Pin Header	PIN HEADER 1x4P 2.00mm 180D(M) SMD
CR2032Holder	CR-2032 Backup Battery Holder	BATTERY HOLDER 24.9*23.4*8.9 CR2032 BH800.4GG
SMARC	MXM3.0 Connector	MXM 3.0 SOCKET,314POTS,7.8MM HEIGHT

3.2.3. Header Pin Assignments

The following tables describe the electrical signals available on the connectors of the *EVK-STD-CARRIER-S20*. Each section provides relevant details about the connector including part numbers, mating connectors, signal descriptions and references to related chapters.

Pinout Legend

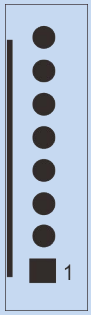
I	*Input*
O	*Output*
I/O	*Input or output*
P	*Power*
AI	*Analogue input*
AO	*Analogue output*
AIO	*Analogue Input or analogue output*
OD	*Open Drain Signal*
#	*Low level active signal*

3.2.3.1. Lithium-ion Battery power input pin header: BAT1

EVK-STD-CARRIER-S20 uses TI *BQ24773* NVDC-1 battery charge controllers. It allows the system to be regulated at battery voltage but does not drop below system minimum voltage. With this feature, the system keeps operating even when the battery is completely discharged or removed.

The following table shows the pin-out of the *BAT1* connector.

Bat1: *Location on Board, A6*

	Lithium-ion Battery power input pin header ***WAFER 8P 2.54mm 180D(M) DIP A2543WV2-8P***			***Edge Finger***	***Type***
Header	*Pin*	*Signal Name*	*Function*	*Pin#*	
	*1*	*+VDD_BAT*	*Battery Supply Voltage*	*-*	*P*
	2	*+VDD_BAT*	*Battery Supply Voltage*	*-*	*P*
	3	*I2C_PM_DAT_3V3*	*Power management I2C bus data*	*P122*	*IO OD*
	4	*I2C_PM_CLK_3V3*	*Power management I2C bus clock*	*P121*	*IO OD*
	5	*NC*	*Not Connected*		
	6	*NC*	*Not Connected*		
	7	*GND*	*Ground*	*-*	*P*
	8	*GND*	*Ground*	*-*	*P*

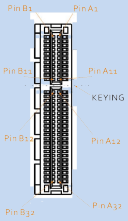
Note:

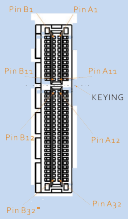
The I2C address for *TI BQ24773* smart charger IC is *0x6A* and connects to *I2C_PM* bus from SMARC module. The *EVK-STD-CARRIER-S20* supports 2-pack or above battery only.

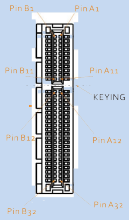
3.2.3.2. PCIe x4 Card Slot: PCIE

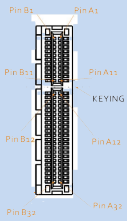
The signals of *PCIex4* card slot are originated from *PCIE_A, PCIe_B, PCIe_C and PCIe_D* of *SMRAC* card. The following table shows the pin-out of the *PCIEx4* connector.

PCIEx4: *Location on Board, F4/F5/F6*

Header	PCIe x4 Card Slot PCIEXPRESS 64P 180D(F) DIP 2EG01817-D2D-DF			Edge Finger	Type
	Pin	Signal Name	Function	Pin#	
	Side A Connector				
	A1	PCIE_A_PRSNT1#	Hot plug presence detect	P74	I
	A2	+12V	+12V Power	-	P
	A3	+12V	+12V Power	-	P
	A4	GND	Ground	-	P
	A5	PCIEA_JTAG2	TCK	-	I
	A6	PCIEA_JTAG3	TDI	-	I
	A7	PCIEA_JTAG4	TDO	-	O
	A8	PCIEA_JTAG5	TMS	-	I
	A9	+3.3V	+3.3V Power	-	P
	A10	+3.3V	+3.3V Power	-	P
	A11	PWRGD	Power Good	-	O
	Mechanical Key				
	A12	GND	Ground	-	P
	A13	PCIE_A_REFCK+	Reference Clock Differential Pair	P83	O
	A14	PCIE_A_REFCK-		P84	O
	A15	GND	Ground	-	P
	A16	PCIE_A_RX+	Receiver Lane A, Differential Pair	P86	I
	A17	PCIE_A_RX-		P87	I
	A18	GND	Ground	-	P

	PCIe x4 Card Slot PCIEXPRESS 64P 180D(F) DIP 2EG01817-D2D-DF			Edge Finger	Type
Header	Pin	Signal Name	Function	Pin#	
	A19	NC	Not Connected		
	A20	GND	Ground	-	P
	A21	PCIE_B_RX+	Receiver Lane B, Differential Pair	S87	I
	A22	PCIE_B_RX-		P88	I
	A23	GND	Ground	-	P
	A24	GND	Ground	-	P
	A25	PCIE_C_RX+	Receiver Lane C, Differential Pair	S78	I
	A26	PCIE_C_RX-		P79	I
	A27	GND	Ground	-	P
	A28	GND	Ground	-	P
	A29	PCIE_D_RX+	Receiver Lane D, Differential Pair	S78	I
	A30	PCIE_D_RX-		P79	I
	A31	GND	Ground	-	P
	A32	NC	Not Connected		

Header	PCIe x4 Card Slot PCIEXPRESS 64P 180D(F) DIP 2EG01817-D2D-DF Pin	Signal Name	Function	Edge Finger Pin#	Type
	Side B Connector				
	B1	+12V	+12V Power	-	P
	B2	+12V	+12V Power	-	P
	B3	RSVD	Reserved	-	-
	B4	GND	Ground	-	P
	B5	I2C_PM_CK_3V3	I2C Clock	P121	IO OD
	B6	I2C_PM_DAT_3V3	I2C Data	P122	IO OD
	B7	GND	Ground	-	P
	B8	+3.3V	+3.3V Power	-	P
	B9	PCIEA_JTAG1	+TRST#		I
	B10	+3.3V	+3.3V Power	-	P
	B11	PCIE_A_WAKE#	Link Reactivation	S146	I
	Mechanical Key				
	B12	RSVD	Reserved	-	-
	B13	GND	Ground	-	P
	B14	PCIE_A_TX+	Transmitter Lane A, Differential Pair	P89	O
	B15	PCIE_A_TX-		P90	O
	B16	GND	Ground	-	P
	B17	NC	Not Connected		
	B18	GND	Ground	-	P

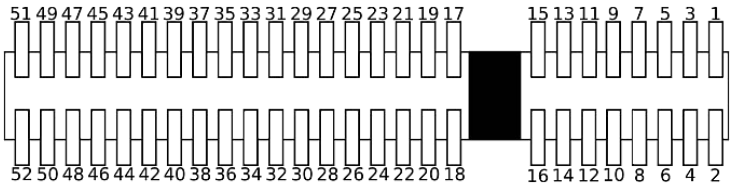
Header	PCIe x4 Card Slot PCIEXPRESS 64P 180D(F) DIP 2EG01817-D2D-DF Pin	Signal Name	Function	Edge Finger Pin#	Type
	B19	PCIE_B_TX+	Transmitter Lane B, Differential Pair	S90	O
	B20	PCIE_B_TX-		P91	O
	B21	GND	Ground	-	P
	B22	GND	Ground	-	P
	B23	PCIE_C_TX+	Transmitter Lane C, Differential Pair	S81	O
	B24	PCIE_C_TX-		P82	O
	B25	GND	Ground	-	P
	B26	GND	Ground	-	P
	B27	PCIE_D_TX+	Transmitter Lane D, Differential Pair	S29	O
	B28	PCIE_D_TX-		P30	O
	B29	GND	Ground	-	P
	B30	NC	Not Connected		
	B31	NC	Not Connected		
	B32	GND	Ground	-	P

Note:

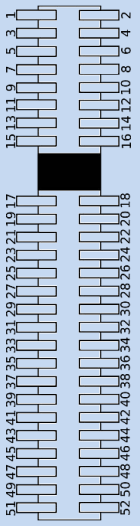
When port 3 of *SW1* dip switch is off, the *PCIe_B* signals are present on this *PCIex4* connector. When port 4 of *SW1* dip switch is off, the *PCIe_C* signals are present on this PCIex4 connector as well.

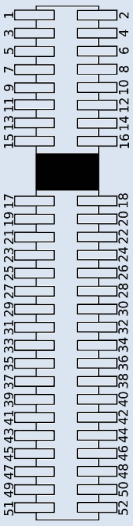
3.2.3.3. mini-PCIE Card Slot: mini-PCIE1

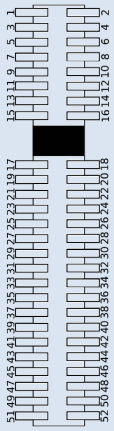
The signals of *mini-PCIE1* card slot are originated from *PCIE_B* of *SMRAC* card. The 5th set of USB signals (USB4 or port 5 of USB2517 hub) are also connected to this connector. The following table shows the pin-out of the *mini-PCIE1* connector.



Mini-PCIE1: *Location on Board, D6/E6*

Header	Mini-PCIE Card Slot 0.80mm Pitch, 5.20mm Height, PCI Express* Mini Card, 52 Circuit, Right Angle, Surface Mount, 0.25µm Gold (Au) Plating					
	Pin	Signal Name	Function	Pin	Signal Name	Function
	Top Side			Bottom Side		
	1	PCIE_B_WAKE#	Link Reactivation	2	+3.3V	+3.3V Power
	3	RSVD	Reserved	4	GND	Ground
	5	RSVD	Reserved	6	1.5V	+1.5V Power
	7	PCIE_B_CKREQ#	Request running clock	8	UIM_PWR	Sim card VDC power supply
	9	GND	Ground	10	UIM_DATA	Sim card serial data
	11	PCIE_B_REFCK+	Reference Clock Differential Pair	12	UIM_CLK	Sim card clock signal
	13	PCIE_B_REFCK-		14	UIM_RESET	Sim card reset signal
	15	GND	Ground	16	UIM_VPP	Programing voltage input

Header	Mini-PCIE Card Slot 0.80mm Pitch, 5.20mm Height, PCI Express* Mini Card, 52 Circuit, Right Angle, Surface Mount, 0.25µm Gold (Au) Plating					
	Pin	Signal Name	Function	Pin	Signal Name	Function
	Top Side			Bottom Side		
	Mechanical Key					
	17	UIM_C8	Optionally used for USB interfaces and other uses.	18	GND	Ground
	19	UIM_C4	Optionally used for USB interfaces and other uses.	20	+3.3V	+3.3V Power
	21	GND	Ground	22	PCIE_B_PERST#	PCIe Fundamental Reset output
	23	PCIE_B_RX-	Receiver, Differential Pair	24	+3.3Vaux	+3.3V Power
	25	PCIE_B_RX+		26	GND	Ground
	27	GND	Ground	28	+1.5V	+1.5V Power
	29	GND	Ground	30	I2C_PM_CK_3V3	I2C Clock
	31	PCIE_B_TX-	Transmitter, Differential Pair	32	I2C_PM_DAT_3V3	I2C Data
	33	PCIE_B_TX+		34	GND	Ground
	35	GND	Ground	36	USB_PCIE_B_D-	Universal serial bus port 3 (-)
	37	RSVD	Reserved	38	USB_PCIE_B_D+	Universal serial bus port 3 (+)
	39	RSVD	Reserved	40	GND	Ground

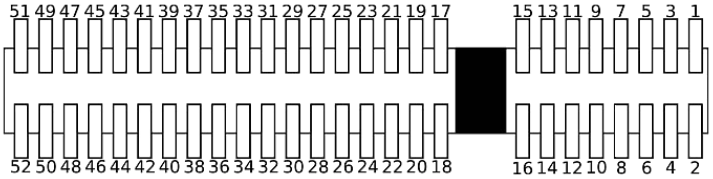
Header	Mini-PCIE Card Slot 0.80mm Pitch, 5.20mm Height, PCI Express* Mini Card, 52 Circuit, Right Angle, Surface Mount, 0.25µm Gold (Au) Plating					
	Pin	Signal Name	Function	Pin	Signal Name	Function
	Top Side			Bottom Side		
	41	RSVD	Reserved	42	LED_WWAN#	Wireless Card Status Indicator
	43	RSVD	Reserved	44	LED_WLAN#	
	45	RSVD	Reserved	46	LED_WPAN	
	47	RSVD	Reserved	48	+1.5V	+1.5V Power
	49	RSVD	Reserved	50	GND	Ground
	51	RSVD	Reserved	52	+3.3V	+3.3V Power

Note:

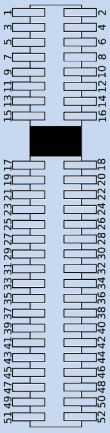
When port 3 of *SW1* dip switch is ON, the *PCIe_B* signals are present on this *mini-PCIE1* connector.

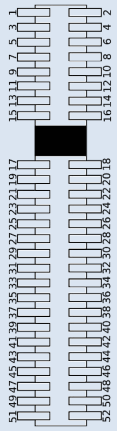
3.2.3.4. mini-PCIE Card Slot: mini-PCIE2

The signals of *mini-PCIE2* card slot are originated from *PCIE_C* of *SMRAC* card. The 6th set of *USB* signals USB5 or port 6 of USB2517 hub are also connected to this connector. The following table shows the pin-out of the *mini-PCIE2* connector.



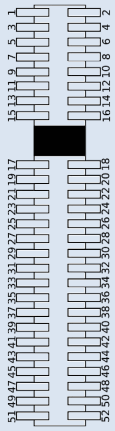
Mini-PCIE2: *Location on Board, D4/E4*

	Mini-PCIE Card Slot ***0.80mm Pitch, 5.20mm Height, PCI Express* Mini Card, 52 Circuit, Right Angle, Surface Mount, 0.25µm Gold (Au) Plating***				
Header	*Pin*	*Signal Name*	*Function*	*Pin*	*Signal Name*	*Function*
	Top Side			*Bottom Side*		
	*1*	*PCIE_C_ WAKE#*	*Link Reactivation*	*2*	*+3.3V*	*+3.3V Power*
	3	*RSVD*	*Reserved*	*4*	*GND*	*Ground*
	5	*RSVD*	*Reserved*	*6*	*1.5V*	*+1.5V Power*
	7	*PCIE_C_ CKREQ#*	*Request running clock*	*8*	*UIM_PWR*	*Sim card VDC power supply*
	9	*GND*	*Ground*	*10*	*UIM_DATA*	*Sim card serial data*
	11	*PCIE_C_ REFCK+*	*Reference Clock Differential Pair*	*12*	*UIM_CLK*	*Sim card clock signal*
	13	*PCIE_C_ REFCK-*		*14*	*UIM_RESET*	*Sim card reset signal*
	15	*GND*	*Ground*	*16*	*UIM_VPP*	*Programing voltage input*

Header	Mini-PCIE Card Slot 0.80mm Pitch, 5.20mm Height, PCI Express* Mini Card, 52 Circuit, Right Angle, Surface Mount, 0.25µm Gold (Au) Plating					
	Pin	Signal Name	Function	Pin	Signal Name	Function
	Top Side			Bottom Side		
	Mechanical Key					
	17	UIM_C8	Optionally used for USB interfaces and other uses.	18	GND	Ground
	19	UIM_C4	Optionally used for USB interfaces and other uses.	20	+3.3V	+3.3V Power
	21	GND	Ground	22	PCIE_C_PERST#	PCIe Fundamental Reset output
	23	PCIE_C_RX-	Receiver, Differential Pair	24	+3.3Vaux	+3.3V Power
	25	PCIE_C_RX+		26	GND	Ground
	27	GND	Ground	28	+1.5V	+1.5V Power
	29	GND	Ground	30	I2C_PM_CK_3V3	I2C Clock
	31	PCIE_C_TX-	Transmitter, Differential Pair	32	I2C_PM_DAT_3V3	I2C Data
	33	PCIE_C_TX+		34	GND	Ground
	35	GND	Ground	36	USB_PCIE_C_D-	Universal serial bus port 4 (-)
	37	RSVD	Reserved	38	USB_PCIE_C_D+	Universal serial bus port 4 (+)
	39	RSVD	Reserved	40	GND	Ground

Mini-PCIE Card Slot

0.80mm Pitch, 5.20mm Height, PCI Express* Mini Card, 52 Circuit, Right Angle, Surface Mount, 0.25µm Gold (Au) Plating

Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	Top Side			Bottom Side		
	41	RSVD	Reserved	42	LED_WWAN#	Wireless Card Status Indicator
	43	RSVD	Reserved	44	LED_WLAN#	
	45	RSVD	Reserved	46	LED_WPAN	
	47	RSVD	Reserved	48	+1.5V	+1.5V Power
	49	RSVD	Reserved	50	GND	Ground
	51	RSVD	Reserved	52	+3.3V	+3.3V Power

Note:

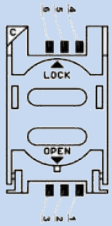
When port 4 of *SW1* dip switch is ON, the *PCIe_C* signals are present on this *mini-PCIE2* connector.

3.2.3.5. SIM Card Holder: SIM_SLOT1 and SIM_SLOT2

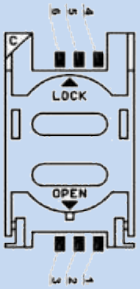
Two *SIM* card holders are present on *EVK-STD-CARRIER-S20* for *3G/HSPA mini-PCIE* module. The signals of the *SIM_SLOT1* are connected to *mini-PCIE1* connector and *SIM_SLOT2* are connected to *mini-PCIE2* connector..

The following table shows the pin-out of *SIM_SLOT1* connector.

SIM_SLOT1: *Location on Board, D5/E5*

	SIM Card Holder1 ***WAFER 8P 2.54mm 180D(M) DIP A2543WV2-8P***			***Edge Finger***	***Type***
Header	*Pin*	*Signal Name*	*Function*	*Pin#*	
	*1*	*UIM_B_PWR*	*Power Supply Input*	-	*P*
	2	*UIM_B_RESET*	*Reset signal, used to reset the card's communications.*	-	*O*
	3	*UIM_B_CLK*	*Provides the card with a clock signal, from which data communications timing is derived*	-	*O*
	4	*UIM_B_C4*	*AUX1, optionally used for USB interfaces and other uses.*	-	-
	5	*GND*	*Ground*	-	*P*
	6	*UIM_B_VPP*	*Programing voltage input*		*P*
	7	*UIM_B_DATA*	*Serial Data*	-	*IO*
	8	*UIM_B_C8*	*AUX2, optionally used for USB interfaces and other uses.*	-	-

SIM_SLOT2: *Location on Board, D2/E2/D3/E3*

	SIM Card Holder2 ***WAFER 8P 2.54mm 180D(M) DIP A2543WV2-8P***			***Edge Finger***	***Type***
Header	*Pin*	*Signal Name*	*Function*	*Pin#*	
	*1*	*UIM_C_PWR*	*Power Supply Input*	-	*P*
	2	*UIM_C_RESET*	*Reset signal, used to reset the card's communications.*	-	*O*
	3	*UIM_C_CLK*	*Provides the card with a clock signal, from which data communications timing is derived*	-	*O*
	4	*UIM_C_C4*	*AUX1, optionally used for USB interfaces and other uses.*	-	-
	5	*GND*	*Ground*	-	*P*
	6	*UIM_C_VPP*	*Programing voltage input*		*P*
	7	*UIM_C_DATA*	*Serial Data*	-	*IO*
	8	*UIM_C_C8*	*AUX2, optionally used for USB interfaces and other uses.*	-	-

3.2.3.6. SATA Connector: SATA

The following table shows the pin-out of *SATA* connector.

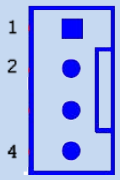
SATA: *Location on Board, D2*

	SATA Connector Serial ATA 7P 1.27mm 180D(M) DIP WATM-07DBN4A3B8			Edge Finger	Type
Header	Pin	Signal Name	Function	Pin#	
	1	GND	Ground	-	P
	2	SATA_TX+	Transmit Output differential pair.	P48	
	3	SATA_TX-	Transmit Output differential pair.	P49	
	4	GND	Ground	-	P
	5	SATA_RX-	Receive Input differential pair	P52	I
	6	SATA_RX+	Receive Input differential pair	P51	I
	7	SATADOM	Sata Dom Pin 7 Power		P

3.2.3.7. SATA Power Connector: SATA_PWR

The following table shows the pin-out of *SATA Power* connector.

SATA_PWR: *Location on Board, A2*

	SATA Power Connector WAFER 4P 2.5mm 180D(M) DIP 24W1161-04S10-01T			Edge Finger	Type
Header	Pin	Signal Name	Function	Pin#	
	1	+5V	+5V Power	-	P
	2	GND	Ground	-	P
	3	GND	Ground	-	P
	4	GND	Ground	-	P
	5	+12V	+12V Power	-	P

Note:

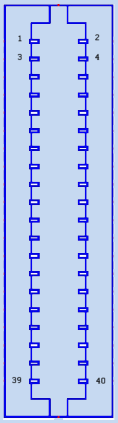
SATA Power cable is available from *Embedian* and come with *EVK-STD-CARRIER-S20*. The part number from *Embedian* is *MKSA-041522-F35C-LF*.

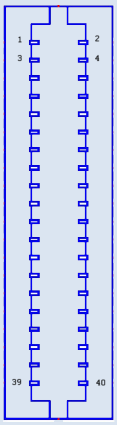
Figure 10: SATA Power Cable

3.2.3.8. 2-LANE and 4-LANE CAMERA Connector: CAMERA

The following table shows the pin-out of *CAMERA* connector.

CAMERA: *Location on Board, B6*

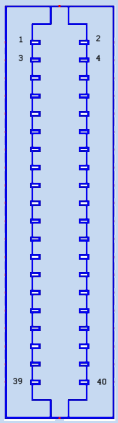
	2-LANE and 4-LANE CAMERA Connector B/B CONN. 2x20P 0.5mm 180D(M) SMD DF12(3.0)-40DS					
Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	Odd Side			Even Side		
	1	GND	Ground	2	GND	Ground
	3	CSI1_CK+	CSI1 differential clock inputs	4	CSI0_CK+	CSI0 differential clock inputs
	5	CSI1_CK-	CSI1 differential clock inputs	6	CSI0_CK-	CSI0 differential clock inputs
	7	GND	Ground	8	GND	Ground
	9	CSI1_D0+	CSI1 differential data inputs 0	10	CSI0_D0+	CSI0 differential data inputs 0
	11	CSI1_D0-	CSI1 differential data inputs 0	12	CSI0_D0-	CSI0 differential data inputs 0
	13	GND	Ground	14	GND	Ground
	15	CSI1_D1+	CSI1 differential data inputs 1	16	CSI0_D1+	CSI0 differential data inputs 1
	17	CSI1_D1-	CSI1 differential data inputs 1	18	CSI0_D1-	CSI0 differential data inputs 1
	19	GND	Ground	20	GND	Ground

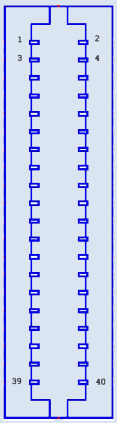
Header	2-LANE and 4-LANE CAMERA Connector B/B CONN. 2x20P 0.5mm 180D(M) SMD DF12(3.0)-30D					
	Pin	Signal Name	Function	Pin	Signal Name	Function
	Odd Side			Even Side		
	21	CSI1_D2+	CSI1 differential data inputs 2	22	I2C_CAM0_CK	Camera0 I2C bus clock
	23	CSI1_D2-	CSI1 differential data inputs 2	24	I2C_CAM0_DAT	Camera0 I2C bus data
	25	GND	Ground	26	CAM0_PWR#	Camera 0 Power Enable, active low output
	27	CSI1_D3+	CSI1 differential data inputs 3	28	CAM0_RST#	Camera 0 Reset, active low output
	29	CSI1_D3-	CSI1 differential data inputs 3	30	I2C_CAM1_CK	Camera1 I2C bus clock
	31	GND	Ground	32	I2C_CAM1_DAT	Camera1 I2C bus data
	33	CAM_MCK	Master clock output for CSI1 camera support	34	CAM1_PWR#	Camera 1 Power Enable, active low output
	35	GND	Ground	36	CAM1_RST#	Camera 1 Reset, active low output
	37	+3.3V	+3.3V Power	38	+1.8V	+1.8V Power
	39	+3.3V	+3.3V Power	40	+1.8V	+1.8V Power

3.2.3.9. LVDS Connector: LVDS

The following table shows the pin-out of *LVDS* connector.

LVDS: *Location on Board, A1*

	LVDS Connector					
	B/B Conn. 40P 1.25mm 90D SMD DF13-40DP-1.25V(91)					
Header	*Pin*	*Signal Name*	*Function*	*Pin*	*Signal Name*	*Function*
	Odd Side (Channel 0)			*Even Side (Channel 1)*		
	*1*	*VDD_LCD*	*LVDS panel VDD*	*2*	*VDD_LCD*	*LVDS panel VDD*
	3	*VDD_LCD*	*LVDS panel VDD*	*4*	*VDD_LCD*	*LVDS panel VDD*
	5	*GND*	*Ground*	*6*	*GND*	*Ground*
	7	*LVDS0_D0-*	*LVDS0 LCD data channel differential pairs 1*	*8*	*LVDS1_D0-*	*LVDS1 LCD data channel differential pairs 1*
	9	*LVDS0_D0+*		*10*	*LVDS1_D0+*	
	11	*GND*	*Ground*	*12*	*GND*	*Ground*
	13	*LVDS0_D1-*	*LVDS0 LCD data channel differential pairs 2*	*14*	*LVDS1_D1-*	*LVDS1 LCD data channel differential pairs 2*
	15	*LVDS0_D1+*		*16*	*LVDS1_D1+*	
	17	*GND*	*Ground*	*18*	*GND*	*Ground*
	19	*LVDS0_D2-*	*LVDS0 LCD data channel differential pairs 3*	*20*	*LVDS1_D2-*	*LVDS1 LCD data channel differential pairs 3*
	21	*LVDS0_D2+*		*22*	*LVDS1_D2+*	

Header	LVDS Connector B/B Conn. 40P 1.25mm 90D SMD DF13-40DP-1.25V(91)					
	Pin	Signal Name	Function	Pin	Signal Name	Function
	Odd Side (Channel 0)			Even Side (Channel 1)		
	23	GND	Ground	24	GND	Ground
	25	LVDS0_CK-	LVDS0 LCD differential clock pairs	26	LVDS1_CK-	LVDS1 LCD differential clock pairs
	27	LVDS0_CK+		28	LVDS1_CK+	
	29	GND	Ground	30	GND	Ground
	31	LVDS0_D3-	LVDS0 LCD data channel differential pairs 4	32	LVDS1_D3-	LVDS1 LCD data channel differential pairs 4
	33	LVDS0_D3+		34	LVDS1_D3+	
	35	GND	Ground	36	GND	Ground
	37	I2C_LCD_CK	I2C_LCD bus clock	38	I2C_LCD_DAT	I2C_LCD bus data
	39	EDP0_HPD	eDP0 Hot Plug Detect	40	EDP1_HPD	eDP1 Hot Plug Detect

Note:

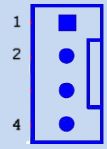
1. *EVK-STD-CARRIER-S20* supports dual-channel *LVDS* (*LVDS0* and *LVDS1*).
2. *LVDS cables support the following panels.*
   AUO G240HW01 V0 24 inch-wide 1920 (H) x 1080 (V) TFT color LCD
   or
   AUO G185XW01 V2 18.5 inch-wide WXGA 1366 (H) x 768 (V) TFT color LCD or
   AUO G070VW01 V0 7 inch WVGA 800 (H) x 480 (V) TFT color LCD

   For detail part number, please see the following section.

3.2.3.10. LVDS Backlight Power Connector: LVDS0_BKLT and LVDS1_BKLT

The following table shows the pin-out of *LVDS0 Backlight Power* connector.

LVDS0_BKLT: *Location on Board, A2*

	LVDS0 Backlight Connector WAFER BOX 2.0mm 4P 180D(M) DIP WO/Pb JIH VEI			Edge Finger	Type
Header	Pin	Signal Name	Function	Pin#	
	1	VDD_BKLT	Backlight Power	-	P
	2	LCD0_BKLT_EN	High enables panel backlight	S127	O
	3	LCD_BKLT_PWM	Display backlight PWM control	S141	O
	4	GND	Ground	-	P

The following table shows the pin-out of *LVDS1 Backlight Power* connector.

LVDS1_BKLT: *Location on Board, A2*

	LVDS1 Backlight Connector WAFER BOX 2.0mm 4P 180D(M) DIP WO/Pb JIH VEI			Edge Finger	Type
Header	Pin	Signal Name	Function	Pin#	
	1	VDD_BKLT	Backlight Power	-	P
	2	LCD1_BKLT_EN	High enables panel backlight	S107	O
	3	LCD_BKLT_PWM	Display backlight PWM control	S122	O
	4	GND	Ground	-	P

Note:

The following table shows the part number of *LVDS* cables and *LVDS* backlight cables for supported panel. These cables are available from Embedian.

Supported Panel	*P/N (LVDS Cable + LVDS Backlight Cable)*
AUO G240HW01 V0 (1080p dual channel)	*DF13FIXL-B203028-A55CB-LF*
AUO G185XW01 V2 (1366x768 single channel)	*DF13FIXL-B203028-A45CA-LF*
AUO G070VW01 V0 (800x480 single channel)	*DF13DF19-B202028-F30CA-LF*

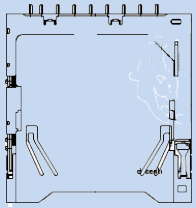
The default packing list comes with *DF13DF19-B202028-F30CA-LF* unless specified.

Figure 11: LVDS Cable and LVDS Backlight Cable

3.2.3.11. SD/SDHC Card Connector: SD

The following table shows the pin-out of *SD* connector.

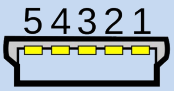
SD: *Location on Board, B1/B2*

Header	SD/SDHC Card Connector Right Angle, SMT, 2.75mm height, Push Push Normal Type With Detect Switch			Edge Finger	Type
	Pin	Signal Name	Function	Pin#	
	1	SDIO_D3	SD receive/transmit data	P42	IO
	2	SDIO_CMD	SD receive response/ transmit command	P34	IO
	3	VSS1	Ground	-	P
	4	VDD_SD0	Power	-	P
	5	SDIO_CK	SD Clock	P36	O
	6	VSS2	Ground	-	P
	7	SDIO_D0	SD receive/transmit data	P39	IO
	8	SDIO_D1	SD receive/transmit data	P40	IO
	9	SDIO_D2	SD receive/transmit data	P41	IO
	10	SDIO_CD#	SD Insert Detect	P35	I
	11	SDIO_WP	SD Write Protect	P33	I

3.2.3.12. USB OTG Connector: USBOTG

The following table shows the pin-out of *USB OTG* connector.

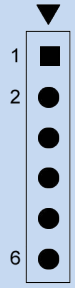
USBOTG: *Location on Board, C1*

	SD/SDHC Card Connector USB OTG mini Type B Connector			Edge Finger	Type
Header	Pin	Signal Name	Function	Pin#	
	1	USB0_VBus	Power Supply	-	P
	2	USB0-	Data-	P61	IO
	3	USB0+	Data+	P60	IO
	4	USB0_OTG_ID	Host cable identification	P64	IO
	5	GND	Ground	-	P

3.2.3.13. SPI0 CS0 Pin Header: SPI0

The following table shows the pin-out of *SPI0 CS0* pin header.

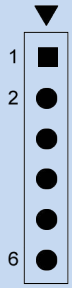
SPI0: *Location on Board, F3*

	SPI0 CS0 Pin Header PIN HEADER 1x6P 2.00mm 180D(M) SMD			Edge Finger	Type
Header	Pin	Signal Name	Function	Pin#	
	1	+3.3V	+3.3V Power	-	P
	2	SPI00_SCLK	SPI0 Master Clock output	P44	O
	3	SPI00_MOSI	SPI0 Master Data output	P46	O
	4	SPI00_MISO	SPI0 Master Data input	P45	I
	5	SPI00_CS#	SPI0 Master Chip Select 0 output	P43	O
	6	GND	Ground	-	P

3.2.3.14. SPI0 CS1 Pin Header: SPI1

The following table shows the pin-out of *SPI0 CS1* pin header.

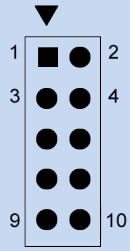
SPI1: *Location on Board, F3*

	SPI0 CS1 Pin Header ***PIN HEADER 1x6P 2.00mm 180D(M) SMD***			***Edge Finger***	***Type***
Header	*Pin*	*Signal Name*	*Function*	*Pin#*	
	*1*	*+3.3V*	*+3.3V Power*	*-*	*P*
	2	*SPI01_SCLK*	*SPI0 Master Clock output*	*P44*	*O*
	3	*SPI01_MOSI*	*SPI0 Master Data output*	*P46*	*O*
	4	*SPI01_MISO*	*SPI0 Master Data input*	*P45*	*I*
	5	*SPI01_CS#*	*SPI0 Master Chip Select 1 output*	*P31*	*O*
	6	*GND*	*Ground*	*-*	*P*

3.2.3.15. ESPI/SPI1 CS0 Pin Header: ESPI0

The following table shows the pin-out of *ESPI/SPI1 CS0* pin header.

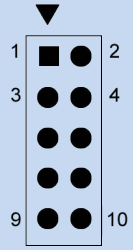
ESPI0: *Location on Board, F2*

Header	ESPI1 CS0 Pin Header PIN HEADER 2x5P 2.00mm 180D(M) SMD			Edge Finger	Type
	Pin	Signal Name	Function	Pin#	
	1	+3.3V	+3.3V Power	-	P
	2	GND	Ground	-	P
	3	ESPI10_CS#	ESPI/SPI1 Master Chip Select 0 output	P54	O
	4	ESPI0_SCLK	ESPI/SPI1 Master Clock output	P56	O
	5	ESPI0_ALERT#	This pin is used by eSPI slave to request service from eSPI master.	S43	I
	6	ESPI0_RESET#	ESPI reset	S58	O
	7	ESPI0_IO0	ESPI Master Data Input / Outputs /SPI1_MOSI	P57	IO
	8	ESPI0_IO1	ESPI Master Data Input / Outputs /SPI1_MISO	P58	IO
	9	ESPI0_IO2	ESPI Master Data Input / Outputs	S56	IO
	10	ESPI0_IO3	ESPI Master Data Input / Outputs	S57	IO

3.2.3.16. ESPI/SPI1 CS1 Pin Header: ESPI1

The following table shows the pin-out of *ESPI/SPI1 CS1* pin header.

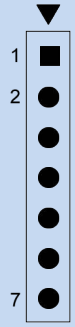
ESPI1: *Location on Board, F2*

Header	ESPI1 CS0 Pin Header PIN HEADER 2x5P 2.00mm 180D(M) SMD			Edge Finger	Type
	Pin	Signal Name	Function	Pin#	
	1	+3.3V	+3.3V Power	-	P
	2	GND	Ground	-	P
	3	ESPI1_CS#	ESPI/SPI1 Master Chip Select 0 output	P55	O
	4	ESPI1_SCLK	ESPI/SPI1 Master Clock output	P56	O
	5	ESPI1_ALERT#	This pin is used by eSPI slave to request service from eSPI master.	S44	I
	6	ESPI1_RESET#	ESPI reset	S58	O
	7	ESPI1_IO0	ESPI Master Data Input / Outputs /SPI1_MOSI	P57	IO
	8	ESPI1_IO1	ESPI Master Data Input / Outputs /SPI1_MISO	P58	IO
	9	ESPI1_IO2	ESPI Master Data Input / Outputs	S56	IO
	10	ESPI1_IO3	ESPI Master Data Input / Outputs	S57	IO

3.2.3.17. I2S2 Pin Header: I2S

The *I2S0* signals from SMARC module connect to a *SGTL5000* audio codec. *I2S2* signals form SMARC module leave as a 1x7 2.0mm pin header. The following table shows the pin-out of *I2S2* pin header.

I2S: *Location on Board, F3*

Header	I2S2 Pin Header PIN HEADER 1x7P 2.00mm 180D(M) SMD			Edge Finger	Type
	Pin	Signal Name	Function	Pin#	
	1	+3.3V	+3.3V Power	-	P
	2	HDA_RST#	HDA reset output (GPIO4)	P112	O
	3	I2S2_LRCK/ HDA_SYNC	Left& Right audio synchronization clock	S50	IO
	4	I2S2_SDOUT HDA_SDO	Digital audio Output	S51	O
	5	I2S2_SDIN HDA_SDI	Digital audio Input	S52	I
	6	I2S2_CK/ HAD_CK	Digital audio clock	S53	IO
	7	GND	Ground	-	P

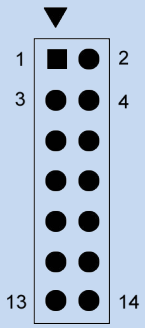
Note:

I2S1 instance is depreciated from *SMARC 2.0* spec.

3.2.3.18. GPIO Pin Header: GPIO

The following table shows the pin-out of *GPIO* pin header.

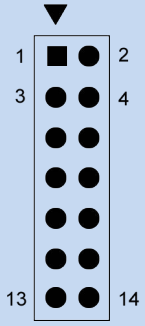
GPIO: *Location on Board, D2*

Header	GPIO Pin Header PIN HEADER 2x7P 2.00mm 180D(M) SMD			Edge Finger	Type
	Pin	Signal Name	Function	Pin#	
	1	+3.3V	+3.3V Power	-	P
	2	GND	Ground	-	P
	3	GPIO0	Camera 0 Power Enable	P108	IO
	4	GPIO6	Tachometer input	P114	IO
	5	GPIO1	Camera 1 Power Enable	P109	IO
	6	GPIO7	PCAM_FLD signal input	P115	IO
	7	GPIO2	Camera 0 Reset	P110	IO
	8	GPIO8	CAN0 Error signal,	P116	IO
	9	GPIO3	Camera 1 Reset	P111	IO
	10	GPIO9	CAN1 Error signal, active low input	P117	IO
	11	GPIO4	HD Audio Reset	P112	IO
	12	GPIO10		P118	IO
	13	GPIO5	PWM output	P113	IO
	14	GPIO11		P119	IO

3.2.3.19. MISC. Signals Pin Header: MISC

The following table shows the pin-out of misc. signals pin header.

MISC: *Location on Board, F2*

Header	MISC Signals Pin Header PIN HEADER 2x7P 2.54mm 180D(M) SMD			Edge Finger	Type
	Pin	Signal Name	Function	Pin#	
	1	POWER_BTN#	Power-button input from Carrier board	P128	I
	2	GND	Ground	-	P
	3	SLEEP#	Sleep indicator from Carrier board	S149	I
	4	GND	Ground	-	P
	5	LID#	Lid open/close indication to Module	S148	I
	6	GND	Ground	-	P
	7	FORCE_RECOV#	Force Recovery	S155	I
	8	GND	Ground	-	P
	9	TEST#	Test Pin	S158	I
	10	GND	Ground	-	P
	11	WDI_Z	Watchdog input transition	-	I
	12	WDI	Wdatchdog input	-	I
	13	RESET_IN#	Reset input from Carrier board	P127	I
	14	GND	Ground	-	P

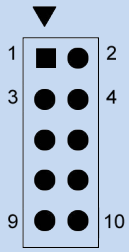
Note:

1. When pin 11 and pin 12 are shunt, *WDT_TIME_OUT#* will be high and reset will be triggered after 200ms.

3.2.3.20. CAN0 Bus Pin Header: CAN0

The following table shows the pin-out of *CAN0* bus pin header.

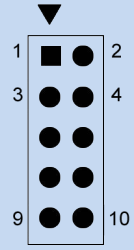
CAN0: *Location on Board, D1*

	CAN0 Bus Pin Header PIN HEADER 2x5P 2.00mm 180D(M) SMD			Edge Finger	Type
Header	Pin	Signal Name	Function	Pin#	
	1	NC	Not Connected	-	-
	2	NC	Not Connected	-	-
	3	CAN0L	CAN Signal Low	P144	I
	4	CAN0H	CAN Signal High	P143	O
	5	NC	Not Connected	-	-
	6	NC	Not Connected	-	-
	7	NC	Not Connected	-	-
	8	NC	Not Connected	-	-
	9	GND	Ground	-	P
	10	NC	Not Connected	-	-

3.2.3.21. CAN1 Bus Pin Header: CAN1

The following table shows the pin-out of *CAN1* bus pin header.

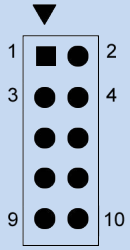
CAN1: *Location on Board, D1*

Header	CAN1 Bus Pin Header PIN HEADER 2x5P 2.00mm 180D(M) SMD			Edge Finger	Type
	Pin	Signal Name	Function	Pin#	
	1	NC	Not Connected	-	-
	2	NC	Not Connected	-	-
	3	CAN1L	CAN Signal Low	P146	I
	4	CAN1H	CAN Signal High	P145	O
	5	NC	Not Connected	-	-
	6	NC	Not Connected	-	-
	7	NC	Not Connected	-	-
	8	NC	Not Connected	-	-
	9	GND	Ground	-	P
	10	NC	Not Connected	-	-

3.2.3.22. SER1 RS232 (2 wires) Pin Header: COM1

The following table shows the pin-out of *COM1* pin header.

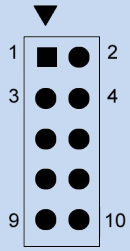
COM1: *Location on Board, D1*

Header	COM1 Pin Header PIN HEADER 2x5P 2.00mm 180D(M) SMD			Edge Finger	Type
	Pin	Signal Name	Function	Pin#	
	1	NC	Not Connected	-	-
	2	NC	Not Connected	-	-
	3	COM1_RXD	Receive Data	P135	I
	4	NC	Not Connected	-	-
	5	COM1_TXD	Transmit Data	P134	O
	6	NC	Not Connected	-	-
	7	NC	Not Connected	-	-
	8	NC	Not Connected	-	-
	9	GND	Ground	-	P
	10	NC	Not Connected	-	-

3.2.3.23. SER3 RS232 (2 wires) Pin Header: COM3

The following table shows the pin-out of *COM3* pin header.

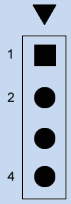
COM3: *Location on Board, E1*

	COM3 Pin Header ***PIN HEADER 2x5P 2.00mm 180D(M) SMD***			***Edge Finger***	***Type***
Header	*Pin*	*Signal Name*	*Function*	*Pin#*	
	*1*	*NC*	*Not Connected*	*-*	*-*
	2	*NC*	*Not Connected*	*-*	*-*
	3	*COM3_RXD*	*Receive Data*	*P141*	*I*
	4	*NC*	*Not Connected*	*-*	*-*
	5	*COM3_TXD*	*Transmit Data*	*P140*	*O*
	6	*NC*	*Not Connected*	*-*	*-*
	7	*NC*	*Not Connected*	*-*	*-*
	8	*NC*	*Not Connected*	*-*	*-*
	9	*GND*	*Ground*	*-*	*P*
	10	*NC*	*Not Connected*	*-*	*-*

3.2.3.24. I2C_GP Pin Header: I2C0

The following table shows the pin-out of *I2C_GP* pin header.

I2C0: *Location on Board, C2*

Header	I2C_GP Pin Header PIN HEADER 1x4P 2.00mm 180D(M) SMD			Edge Finger	Type
	Pin	Signal Name	Function	Pin#	
	1	+3.3V	+3.3V Power	-	P
	2	I2C_GP_CK_3V3	General purpose I2C bus clock	S48	O OD
	3	I2C_GP_DAT_3V3	General purpose I2C bus data	S49	IO OD
	4	GND	Ground	-	P

3.2.3.25. I2C_CAM0 Pin Header: I2C1

The following table shows the pin-out of *I2C_CAM0* pin header.

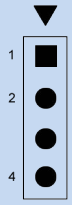
I2C1: *Location on Board, C2*

Header	I2C_CAM0 Pin Header PIN HEADER 1x4P 2.00mm 180D(M) SMD			Edge Finger	Type
	Pin	Signal Name	Function	Pin#	
	1	+3.3V	+3.3V Power	-	P
	2	I2C_CAM0_CK_3V3	Serial Camera0 Support Link - I2C bus clock	S5	O OD
	3	I2C_CAM0_DAT_3V3	Serial Camera0 Support Link - I2C bus data	S7	IO OD
	4	GND	Ground	-	P

3.2.3.26. I2C_CAM1 Pin Header: I2C2

The following table shows the pin-out of *I2C_CAM1* pin header.

I2C2: *Location on Board, C2*

	I2C_CAM1 Pin Header PIN HEADER 1x4P 2.00mm 180D(M) SMD			Edge Finger	Type
Header	Pin	Signal Name	Function	Pin#	
	1	+3.3V	+3.3V Power	-	P
	2	I2C_CAM1_CK_3V3	Serial Camer1a Support Link - I2C bus clock	S1	O OD
	3	I2C_CAM1_DAT_3V3	Serial Camera1 Support Link - I2C bus data	S2	IO OD
	4	GND	Ground	-	P

3.2.3.27. Buzzer: Buzzer

The buzzer on *EVK-STD_CARRIER* is controlled by *PWM* (*GPIO5*). The rated frequency is 2731 + 200Hz.

Buzzer: *Location on Board, A2*

	Buzzer Connector ELECTRO MAGNETIC BUZZER			Edge Finger	Type
Header	Pin	Signal Name	Function	Pin#	
	1	+5V	+5V Power	-	P
	2	GPIO5	PWM Out	P113	O

Note:

To route *GPIO5* to buzzer, port 2 of *SW1* has to be *ON*.

3.2.3.28. MXM3.0 Connector: SMARC

The following table shows the pin-out of *MXM 3.0* pin header.

SMARC: *Location on Board, D3/D4/D5/D6/D7*

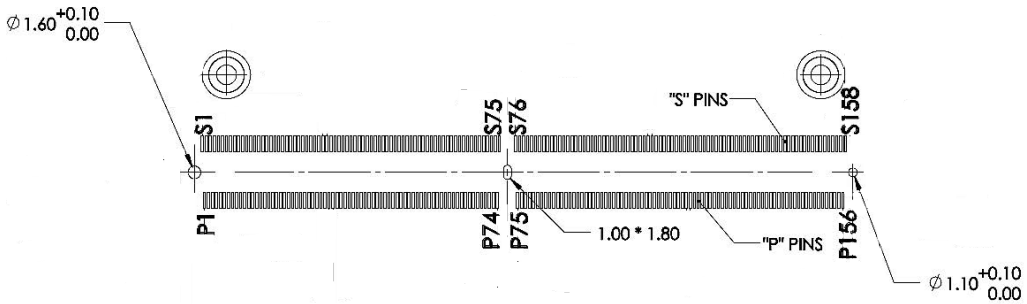


Figure 12: MXM3.0 Connector Pin Layout

MXM 3.0 Connector MXM 3.0 SOCKET,314POTS,7.8MM HEIGHT			
Pin	Signal Name	Pin	Signal Name
P1	SMB_ALERT_1V8#	S1	CS1_TX+ /I2C_CAM1_CK
P2	GND	S2	CS1_TX- /I2C_CAM1_DAT
P3	CSI1_CK+	S3	GND
P4	CSI1_CK-	S4	RSVD
P5	GBE1_SDP	S5	CSI0_TX- / I2C_CAM0_CK
P6	GBE0_SDP	S6	CAM_MCK
P7	CSI1_RX0+	S7	CSI0_TX+ / I2C_CAM0_DAT
P8	CSI1_RX0-	S8	CSI0_CK+
P9	GND	S9	CSI0_CK-
P10	CSI1_RX1+	S10	GND
P11	CSI1_RX1-	S11	CSI0_RX0+
P12	GND	S12	CSI0_RX0-
P13	CSI1_RX2+	S13	GND
P14	CSI1_RX2-	S14	CSI0_RX1+
P15	GND	S15	CSI0_RX1-
P16	CSI1_RX3+	S16	GND
P17	CSI1_RX3-	S17	GbE1_MDI0+
P18	GND	S18	GbE1_MDI0-
P19	GbE0_MDI3-	S19	GbE1_LINK100#
P20	GbE0_MDI3+	S20	GbE1_MDI1+
P21	GbE0_LINK100#	S21	GbE1_MDI1-
P22	GbE0_LINK1000#	S22	GbE1_LINK1000#
P23	GbE0_MDI2-	S23	GbE1_MDI2+

MXM 3.0 Connector MXM 3.0 SOCKET,314POTS,7.8MM HEIGHT			
Pin	Signal Name	Pin	Signal Name
P24	GbE0_MDI2+	S24	GbE1_MDI2-
P25	GbE0_LINK_ACT#	S25	GND
P26	GbE0_MDI1-	S26	GbE1_MDI3+
P27	GbE0_MDI1+	S27	GbE1_MDI3-
P28	GbE0_CTREF	S28	GbE1_CTREF
P29	GbE0_MDI0-	S29	PCIE_D_TX+
P30	GbE0_MDI0+	S30	PCIE_D_TX-
P31	SPI0_CS1#	S31	GBE1_LINK_ACK#
P32	GND	S32	PCIE_D_RX+
P33	SDIO_WP	S33	PCIE_D_RX-
P34	SDIO_CMD	S34	GND
P35	SDIO_CD#	S35	USB4+
P36	SDIO_CK	S36	USB4-
P37	SDIO_PWR_EN	S37	USB3_VBUS_DET
P38	GND	S38	AUDIO_MCK
P39	SDIO_D0	S39	I2S0_LRCK
P40	SDIO_D1	S40	I2S0_SDOUT
P41	SDIO_D2	S41	I2S0_SDIN
P42	SDIO_D3	S42	I2S0_CK
P43	SPI0_CS0#	S43	ESPI_ALERT0#
P44	SPI0_CK	S44	ESPI_ALERT1#
P45	SPI0_DIN	S45	RSVD
P46	SPI0_DO	S46	RSVD

MXM 3.0 Connector MXM 3.0 SOCKET,314POTS,7.8MM HEIGHT			
Pin	Signal Name	Pin	Signal Name
P47	GND	S47	GND
P48	SATA_TX+	S48	I2C_GP_CK
P49	SATA_TX-	S49	I2C_GP_DAT
P50	GND	S50	HDA_SYNC / I2S2_LRCK
P51	SATA_RX+	S51	HDA_SDO / I2S2_SDOUT
P52	SATA_RX-	S52	HDA_SDI / I2S2_SDIN
P53	GND	S53	HDA_CK / I2S2_CK
P54	ESPI1_CS0#	S54	SATA_ACT#
P55	ESPI1_CS1#	S55	USB5_EN_OC#
P56	ESPI1_CK	S56	ESPI_IO_2
P57	ESPI1_IO_0	S57	ESPI_IO_3
P58	ESPI1_IO_1	S58	ESPI_RESET#
P59	GND	S59	USB5+
P60	USB0+	S60	USB5-
P61	USB0-	S61	GND
P62	USB0_EN_OC#	S62	USB3_SSTX+
P63	USB0_VBUS_DET	S63	USB3_SSTX-
P64	USB0_OTG_ID	S64	GND
P65	USB1+	S65	USB3_SSRX+
P66	USB1-	S66	USB3_SSRX-
P67	USB1_EN_OC#	S67	GND
P68	GND	S68	USB3+
P69	USB2+	S69	USB3-

MXM 3.0 Connector MXM 3.0 SOCKET,314POTS,7.8MM HEIGHT			
Pin	Signal Name	Pin	Signal Name
P70	USB2-	S70	GND
P71	USB2_EN_OC#	S71	USB2_SSTX+
P72	RSVD	S72	USB2_SSTX--
P73	RSVD	S73	GND
P74	USB3_EN_OC#	S74	USB2_SSRX+
P75	PCIE_A_RST#	S75	USB2_SSRX-
P76	USB4_EN_OC#	S76	PCIE_B_RST#
P77	RSVD	S77	PCIE_C_RST#
P78	RSVD	S78	PCIE_C_RX+
P79	GND	S79	PCIE_C_RX-
P80	PCIE_C_REFCK+	S80	GND
P81	PCIE_C_REFCK-	S81	PCIE_C_TX+
P82	GND	S82	PCIE_C_TX-
P83	PCIE_A_REFCK+	S83	GND
P84	PCIE_A_REFCK-	S84	PCIE_B_REFCK+
P85	GND	S85	PCIE_B_REFCK-
P86	PCIE_A_RX+	S86	GND
P87	PCIE_A_RX-	S87	PCIE_B_RX+
P88	GND	S88	PCIE_B_RX-
P89	PCIE_A_TX+	S89	GND
P90	PCIE_A_TX-	S90	PCIE_B_TX+
P91	GND	S91	PCIE_B_TX-
P92	HDMI_D2+ /DP1_LANE0+	S92	GND

MXM 3.0 Connector MXM 3.0 SOCKET,314POTS,7.8MM HEIGHT			
Pin	Signal Name	Pin	Signal Name
P93	HDMI_D2- /DP1_LANE0-	S93	DP0_LAN0+
P94	GND	S94	DP0_LAN0-
P95	HDMI_D1+ /DP1_LANE1+	S95	DP0_AUX_SEL
P96	HDMI_D1- /DP1_LANE1-	S96	DP0_LANE1+
P97	GND	S97	DP0_LANE1-
P98	HDMI_D0+ /DP1_LANE2+	S98	DP0_HDP
P99	HDMI_D0- /DP1_LAN2-	S99	DP0_LANE2+
P100	GND	S100	DP0_LAN2-
P101	HDMI_CK+ /DP1_LANE3+	S101	GND
P102	HDMI_CK- /DP1_LANE3-	S102	DP0_LANE3+
P103	GND	S103	DP0_LANE3-
P104	HDMI_HPD /DP1_HPD	S104	USB3_OTG_ID
P105	HDMI_CTRL_CK /DP1_AUX+	S105	DP0_AUX+
P106	HDMI_CTRL_DAT /DP1_AUX-	S106	DP0_AUX-
P107	DP1_AUX_SEL	S107	LCD1_BKLT_EN
P108	GPIO0 / CAM0_PWR#	S108	LVDS1_CK+/eDP1_AUX+/ DSI1_CLK+
P109	GPIO1 / CAM1_PWR#	S109	LVDS1_CK-/eDP1_AUX-/ DSI1_CLK-
P110	GPIO2 / CAM0_RST#	S110	GND
P111	GPIO3 / CAM1_RST#	S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+
P112	GPIO4 / HDA_RST#	S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-
P113	GPIO5 / PWM_OUT	S113	eDP1_HPD
P114	GPIO6 / TACHIN	S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+
P115	GPIO7 / PCAM_FLD	S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-

MXM 3.0 Connector MXM 3.0 SOCKET,314POTS,7.8MM HEIGHT			
Pin	Signal Name	Pin	Signal Name
P116	GPIO8 / CAN0_ERR#	S116	LCD1_VDD_EN
P117	GPIO9 / CAN1_ERR#	S117	LVDS1_2+ /eDP1_TX2+ / DSI1_D2+
P118	GPIO10	S118	LVDS1_2- /eDP1_TX2- / DSI1_D2-
P119	GPIO11	S119	GND
P120	GND	S120	LVDS1_3+ /eDP1_TX3+ / DSI1_D3+
P121	I2C_PM_CK	S121	LVDS1_3- /eDP1_TX3- / DSI1_D3-
P122	I2C_PM_DAT	S122	LCD1_BKLT_PWM
P123	BOOT_SEL0#	S123	RSVD
P124	BOOT_SEL1#	S124	GND
P125	BOOT_SEL2#	S125	LVDS0_0+ /eDP0_TX0+ /DSI0_D0+
P126	RESET_OUT#	S126	LVDS0_0- /eDP0_TX0- /DSI0_D0-
P127	RESET_IN#	S127	LCD_BKLT_EN
P128	POWER_BTN#	S128	LVDS0_1+ /eDP0_TX1+ /DSI0_D1+
P129	SER0_TX	S129	LVDS0_1- /eDP0_TX1- /DSI0_D1-
P130	SER0_RX	S130	GND
P131	SER0_RTS#	S131	LVDS0_2+ /eDP0_TX2+ /DSI0_D2+
P132	SER0_CTS#	S132	LVDS0_2- /eDP0_TX2- /DSI0_D2-
P133	GND	S133	LCD_VDD_EN
P134	SER1_TX	S134	LVDS0_CK+ /eDP0_AUX+/DSI0_CLK+
P135	SER1_RX	S135	LVDS0_CK-/eDP0_AUX-/DSI0_CLK-
P136	SER2_TX	S136	GND
P137	SER2_RX	S137	LVDS0_3+ /eDP0_TX3+ /DSI0_D3+
P138	SER2_RTS#	S138	LVDS0_3- /eDP0_TX3- /DSI0_D3-

MXM 3.0 Connector MXM 3.0 SOCKET,314POTS,7.8MM HEIGHT			
Pin	Signal Name	Pin	Signal Name
P139	SER2_CTS#	S139	I2C_LCD_CK
P140	SER3_TX	S140	I2C_LCD_DAT
P141	SER3_RX	S141	LCD_BKLT_PWM
P142	GND	S142	RSVD
P143	CAN0_TX	S143	GND
P144	CAN0_RX	S144	eDP0_HPD
P145	CAN1_TX	S145	WDT_TIME_OUT#
P146	CAN1_RX	S146	PCIE_WAKE#
P147	VDD_IN	S147	VDD_RTC
P148	VDD_IN	S148	LID#
P149	VDD_IN	S149	SLEEP#
P150	VDD_IN	S150	VIN_PWR_BAD#
P151	VDD_IN	S151	CHARGING#
P152	VDD_IN	S152	CHARGER_PRSNT#
P153	VDD_IN	S153	CARRIER_STBY#
P154	VDD_IN	S154	CARRIER_PWR_ON
P155	VDD_IN	S155	FORCE_RECOV#
P156	VDD_IN	S156	BATLOW#
		S157	TEST#
		S158	VDD_IO_SEL#

Quick Hardware Installation Guide

The purpose of this chapter is to provide a quick hardware installation guide so that developers can easily get the board up and running in few minutes.

Chapter 4 Quick Hardware Installation Guide

The quick hardware installation guides are intended to provide developers with simple instructions on how to install *EVK-STD-CARRIER-S20* evaluation kit from very beginning and have it monitoring your local device in few minutes. No advanced installation options are discussed here - just the basics that will work for 95% of users who want to get started. This guide will lead you through the process of configuring, installing, and developing SMARC module. This guide was written to be as clear as possible and to provide only the details necessary to get you up and running. For more in-depth information, links to other chapters will be located where appropriate.

Step1. Insert SMARC CPU module

Install SMARC CPU module to *EVK-STD-CARRIER-S20 SMARC* connector at 30 degree angle.

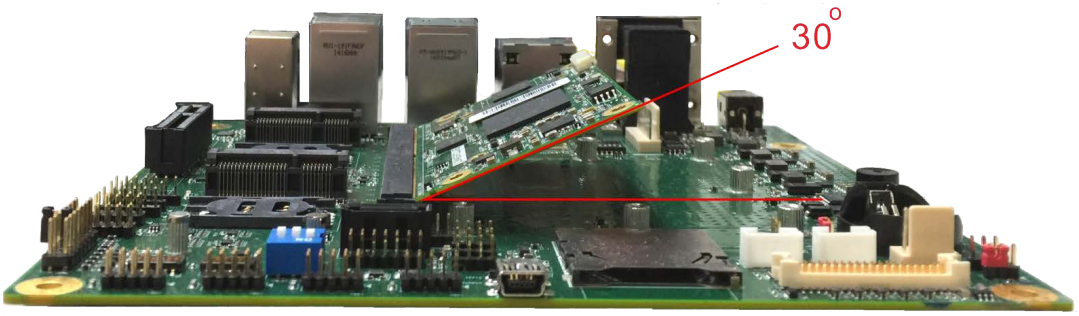


Figure 13: Insert SMARC Module

Step2. Fasten SMARC Module

Press down SMARC CPU module and fasten it by M2.5x 5mm screws.

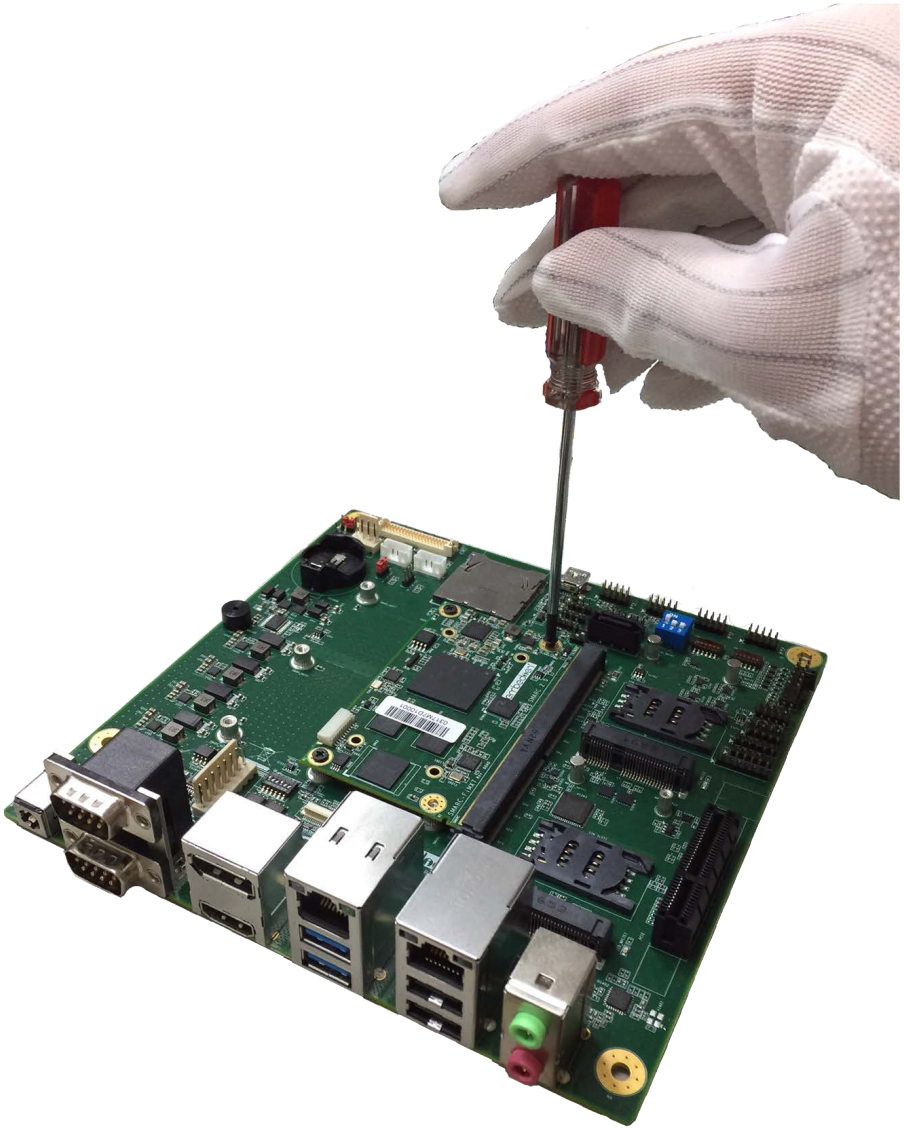


Figure 14: Fasten SMARC Module

Step3. Check Jumper and switch Settings

Before power on, it is very important to check if the jumpers and switches are set properly.
Below picture shows those need to be cared at power up.

1. ***SW1***:
   ON OFF OFF ON OFF OFF: if your debug port is set to *SER0 or SER2.*.

If you need to connect to an LVDS LCD, you will also need to check the *LCD0_VDD_SEL*, *LCD0_BKLT_SEL. LCD0_BKLT_SEL and LCD1_BKLT_SEL*.

2. ***LCD0_BKLT_SEL***:
   Shunt 1-2: 5V
   Shunt 2-3: 12V

3. ***LCD1_BKLT_SEL***:
   Shunt 1-2: 5V
   Shunt 2-3: 12V

4. ***LCD0_VDD_SEL***:
   Shunt 1-2: 3.3V
   Shunt 2-3: 5V

5. ***LCD1_VDD_SEL***:
   Shunt 1-2: 3.3V
   Shunt 2-3: 5V

If your *SMARC* module only has two USB ports, set SW1 and SW2 to all *OFF*.

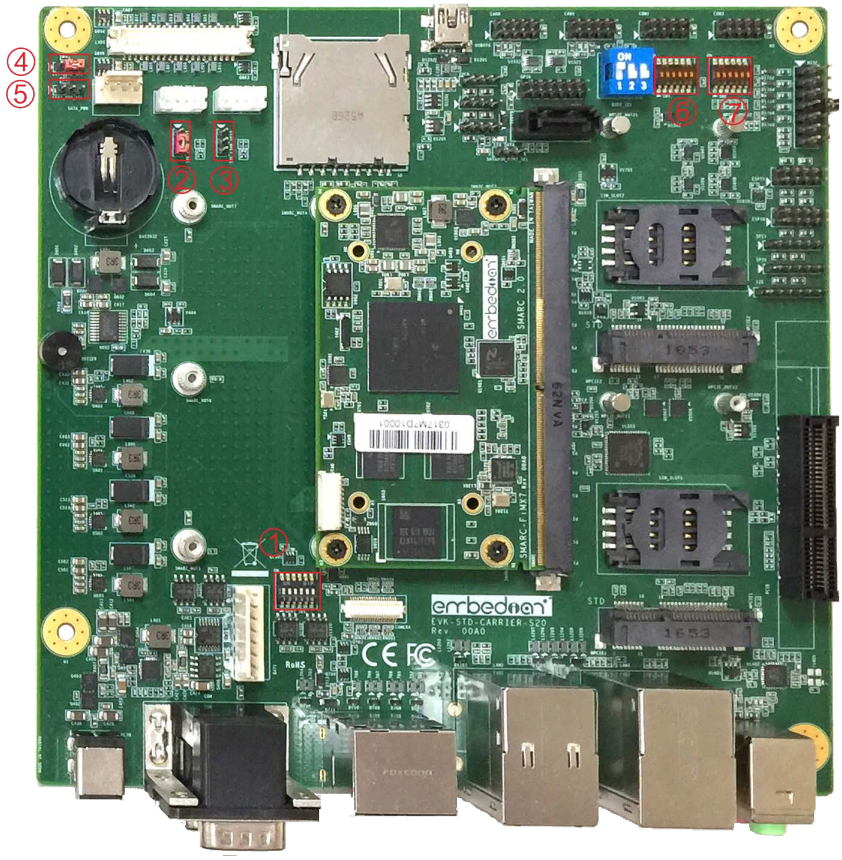


Figure 15: Check Jumpers and switches Settings

Step4. Check BOOT_SEL Settings and Insert Bootable SD card

If *TEST#* pin is shunt crossed, the *SMARC* module will always boot up from SD card. If *TEST#* pin is open, the *SMARC* module will always boot up from on-module SPI NOR flash. Once the bootloader (u-boot) is up, it will read the *BOOT_SEL* setting and decides where to load kernel.
Usually, the first boot-up is from SD card. Please insert the bootable SD card and set the *BOOT_SEL* switch to *ON OFF OFF* as shown in the following picture.
.

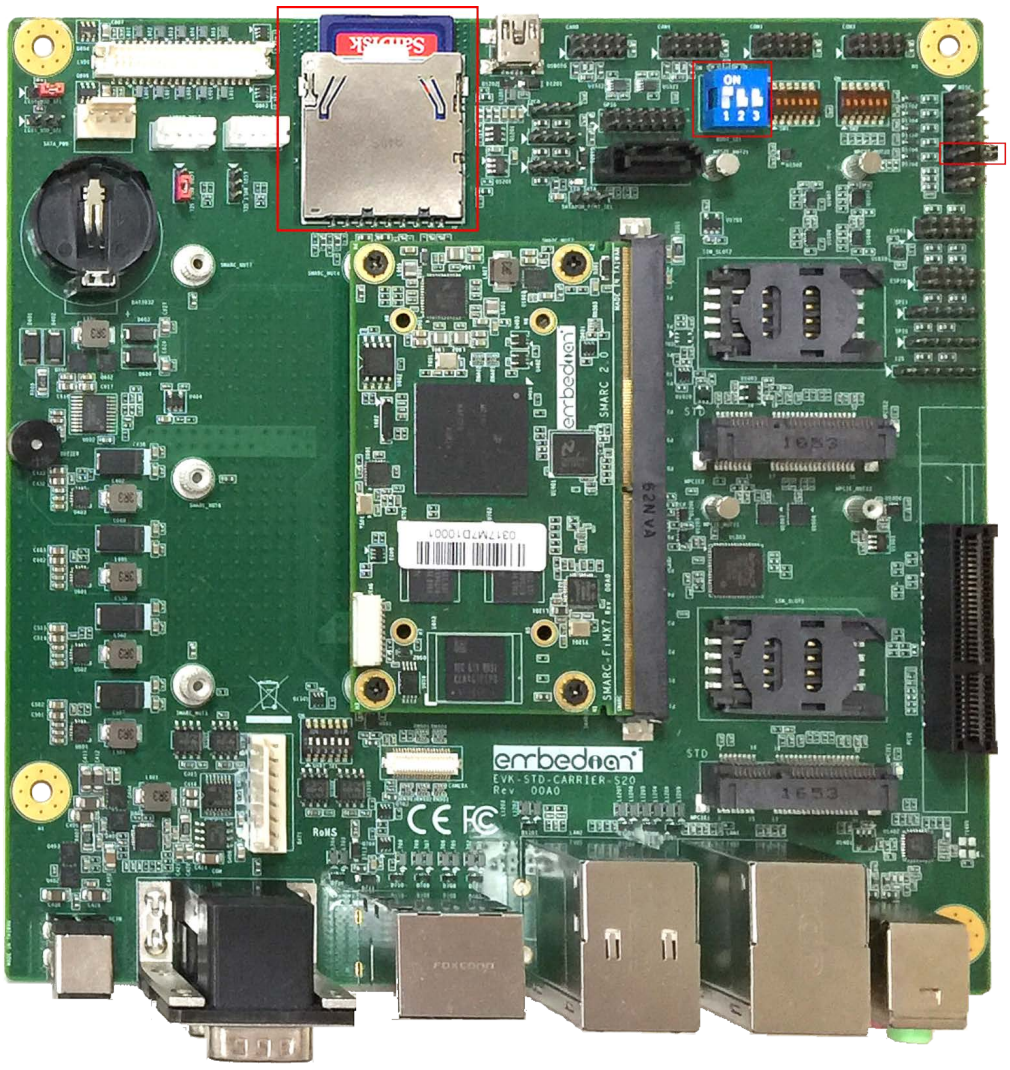


Figure 16: Check BOOT_SEL+ Settings and Insert Bootable SD Card

Step5. Connect Debug Cable, Ethernet Cable and LCD Cable (if necessary) and Apply Power

Step 1~3 assumes that your debug port is set to *SER3*. If you use *SER0* as your debug port, neglect step 1 below.

1. Connect *COM3* header of *EVK-STD-CARRIE*R-*S20* to the 2x5 box header to DB9 cable.
2. Connect the 2x5 box header to a null modem cable (tx/rx crossed).
3. Connect the null modem cable to the *RS232* port of your host PC. Set the baud rate of the serial port as *115200, 8n1*.
4. Connect Ethernet cable to the RJ45 connector (*GBE0*) of *EVK-STD-CARRIER-S20.*

If LVDS *LCD* is required in your application, follow step 5 and step 6 below.

5. Connect *LVDS* cable to *LVDS* connector.
6. Connect *LVDS LCD* backlight cable to *LCD0_BKLT* connector (or *LCD1_BKLT* if you use channel 2).

Bring up the board.

7. Apply 12V~ 24V (~36W power adaptor) DC power to *EVK-STD-CARRIER-S20*, you should be able to see debug message from your putty or serial terminal of your host PC. No root password needed for Yocto rootfs. The default root password for Ubuntu 14.04 is *root*, and default *ubuntu* user is *temppwd*.

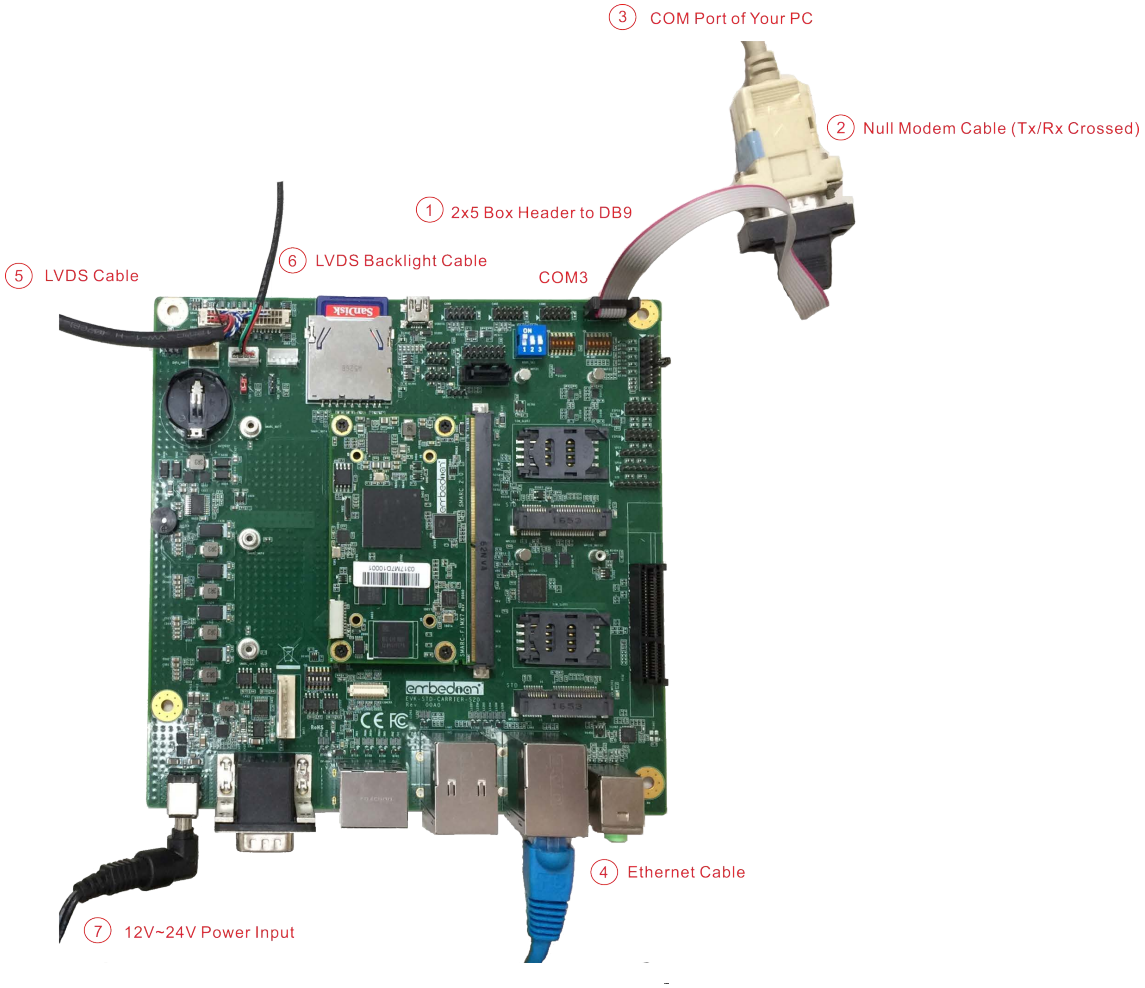


Figure 17: Wiring Diagram