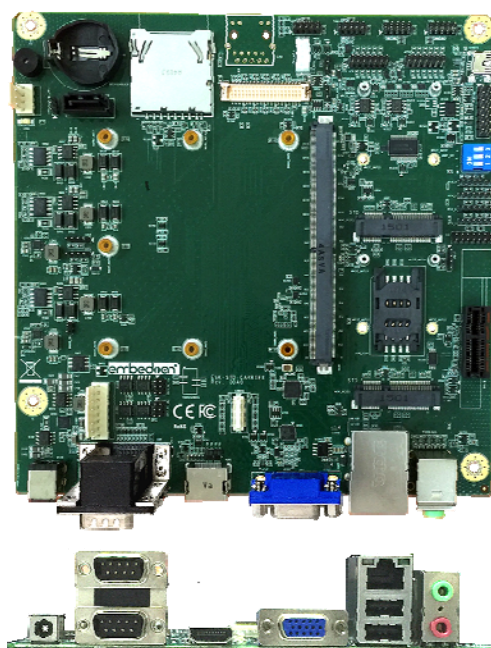


User's Manual

EVK-STD-CARRIER



**Development Board for SMARC
v1.0 and v1.1 compliant modules**

embedian

Revision History

<i>Revision</i>	<i>Date</i>	<i>Changes from Previous Revision</i>
<i>1.0</i>	<i>2015/7/09</i>	<i>Initial Release</i>
<i>2.0</i>	<i>2017/5/08</i>	<i>Change Pin Define of Camera and LVDS Connector for Hardware Revision 00B0</i>

USER INFORMATION

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Using this Manual

This guide provides information about the *SMARC Evaluation Carrier* for embedded *SMARC* core module family. All *SMARC* v 1.0 and v1.1 compliant modules should be able to work under *EVK-STD-CARRIER*.

Conventions used in this guide

This table describes the typographic conventions used in this guide:

<i>This Convention</i>	<i>Is used for</i>
<i>Italic type</i>	Emphasis, new terms, variables, and document titles.
monospaced type	Filenames, pathnames, and code examples.

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Declaration of Conformity

FCC Class B

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the *FCC Rules*. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Packing List

Before installation, please ensure the following items have been shipped.

<i>Items</i>	
<i>EVK-STD-CARRIER</i>	<i>1</i>
<i>12V/3A Power Adapter</i>	<i>1</i>
<i>LDVS Cable (*)</i>	<i>1</i>
<i>LVDS Backlight Cable (*)</i>	<i>1</i>
<i>Pre-Installed Bring Up SD Card (**)</i>	<i>1</i>
<i>2x5 Box Header to DB9 Cable</i>	<i>1</i>
<i>SATA Power Cable</i>	<i>1</i>

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Note 1:

LVDS cables and LVDS backlight cables support the following panels.

1. *AUO G240HW01 V0* 24 inch-wide 1920 (H) x 1080 (V) TFT color LCD or
2. *AUO G185XW01 V2* 18.5 inch-wide WXGA 1366 (H) x 768 (V) TFT color LCD or
3. *AUO G070VW01 V0* 7 inch WVGA 800 (H) x 480 (V) TFT color LCD

If not specified, the default shipping will be cables for 7-inch G070VW01.

Note 2:

Pre-installed SD card only come with the case when users also purchase *Embedian's SMARC* module at the same time.

Embedian SMARC CPU Boards

Part Number	Description
SMARC-T3354-600	TI AM3352 600MHz, 3.3V VDDIO (0°C~60°C)
SMARC-T3354-01G	TI AM3354 1GHz, 3.3V VDDIO (0°C~60°C)
SMARC-T3354-800-I	TI AM3352 800MHz, 3.3V VDDIO (-40°C~85°C)
SMARC-T4378-800	TI AM4378 Cortex-A9 800MHz, 3.3V and 1.8V VDDIO (0°C~60°C)
SMARC-T4378-01G	TI AM4378 Cortex-A9 1GHz, 3.3V and 1.8V VDDIO (0°C~60°C)
SMARC-T4378-800-I	TI AM4378 Cortex-A9 1GHz, 3.3V and 1.8V VDDIO (-40°C~85°C)
SMARC-T4378-01G-I	TI AM4378 Cortex-A9 1GHz, 3.3V and 1.8V VDDIO (-40°C~85°C)
SMARC-FiMX6-S	Freescale i.MX6 Solo Core 1GHz with 512MB memory, 1.8V and 3.3V VDDIO (0°C~60°C)
SMARC-FiMX6-U-1G	Freescale i.MX6 Dual Lite Core 1GHz with 1GB memory, 1.8V and 3.3V VDDIO (0°C~60°C)
SMARC-FiMX6-D-1G	Freescale i.MX6 Dual Core 1GHz with 1GB memory, 1.8V and 3.3V VDDIO (0°C~60°C)
SMARC-FiMX6-D-2G	Freescale i.MX6 Dual Core 1GHz with 2GB memory, 1.8V and 3.3V VDDIO (0°C~60°C)
SMARC-FiMX6-Q-1G	Freescale i.MX6 Quad Core 1GHz with 1GB memory, 1.8V and 3.3V VDDIO (0°C~60°C)
SMARC-FiMX6-Q-2G	Freescale i.MX6 Quad Core 1GHz with 2GB memory, 1.8V and 3.3V VDDIO (0°C~60°C)
SMARC-FiMX6-S-I	Freescale i.MX6 Solo Core 800MHz with 512MB memory, 1.8V and 3.3V VDDIO (-40°C~85°C)
SMARC-FiMX6-Q-1G-I	Freescale i.MX6 Quad Core 800MHz with 1GB memory, 1.8V and 3.3V VDDIO (-40°C~85°C)
SMARC-FiMX7-S	Freescale i.MX7 Solo Core 800MHz with 512MB memory, 1.8V VDDIO (-20°C~85°C)
SMARC-FiMX7-D	Freescale i.MX7 Dual Core 1.2GHz with 1GB memory, 1.8V VDDIO (-20°C~85°C)

Chapter 1

Introduction

This Chapter gives background information on the *EVK-STD-CARRIER* Evaluation Carrier

Section include :

- *EVK-STD-CARRIER* Evaluation Carrier Goals
- Feature Set Overview
- Block Diagram
- Peripheral Overview
- Layout Diagram
- Document and Standard References

Chapter 1 Introduction

This document serves as a user manual and technical reference for the *EMBEDIAN EVK-STD-CARRIER* Evaluation Baseboard. The manual is intended for use by engineering personnel working with *SMARC* modules. It will be very helpful if developers can refer together with the carrier board schematics. *EVK-STD-CARRIER* accepts *SMARC 1.0* AND *SMARC 1.1* compliant modules.

1.1 EVK-STD-CARRIER Evaluation Carrier Goals

EMBEDIAN EVK-STD-CARRIER evaluation carrier is equipped with all mechanical and electrical components necessary for the rapid start-up of the *SMARC* compliant computer on module. The *EVK-STD-CARRIER* is designed for evaluation, testing and prototyping of the *SMARC* modules in development environments prior to use in customer designed applications. It can also be used together with *SMARC* module as an “application ready” *mini-ITX* single board computer.

The *EVK-STD-CARRIER* Evaluation Carrier is intended to serve multiple needs and summarized as followed:

- *SMARC* Module bring-up platform for hardware and software development.
- Module validation platform.
- Customer evaluation platform.
- Customer design reference.
- Manufacturing test platform.
- Flexible prototyping vehicle (facilitated by multiple mezzanines).
- An “application ready” single board computer. (together with *SMARC* module)

1.2 Feature Set Overview

The *EVK-STD-CARRIER* has the following features for supporting the *SMARC* modules:

Computer on Module	SMARC v1.0 and v1.1 Compliant Module	
Graphic	HDMI	1 x HDMI Type A
	LVDS	1 dual-channel 24-bit LVDS
	VGA	1 DSUB15 with female connector (from 24-bit parallel RGB interface)
Ethernet	10/100/1000Mbps	2 RJ45 (one is not populated unless specified for TI AM335X)
Storage	eMMC	Onboard 4GB eMMC
	EEPROM	Onboard AT24C32 EEPROM
	SD	1 SD card slot
	SATA	1 SATAII Connector (with SATA-DOM support)
IO	USB	2 USB 2.0 Type A, 2 USB 2.0 to mini PCIeB and mini PCIeC, 1 USB OTG mini Type AB
	UART	4 RS232 Ports (two of them can be configured as RS422/4845)
	Audio	3.5mm Audio Jack (Headphone and Microphone, SGT5000 Audio Codec)
	Camera input	2 MIPI Connectors (2 LANEs and 4 LANEs)
	CAN	2 CAN 2.0B ports, Differential mode +5V
	GPIO	12 GPIO Ports
	I2C	I2C_GP and I2C_CAM pin header
	SPI	SPI0 and SPI1 pin header with 2 chip selects for each port
	4-Wire Touch	1 x 4-wire touch connector
Expansion	PCIe	1 PCIe and 2 mini PCIe Slots
Communication	SIM Card Holder	For 2.5G/3G PCIe Card

<i>Computer on Module</i>	<i>SMARC v1.0 and v1.1 Compliant Module</i>	
<i>Power Input</i>	<i>Power</i>	<i>Power Inputs (+12V~+24V DC-Jack, Lithium-ion battery socket)</i>
<i>Physical Characters</i>	<i>Dimensions</i>	<i>170mm x 170mm (mini-ITX form factor)</i>

1.3 Block Diagram

An overall system block diagram for the *EVK-STD-CARRIER* Evaluation Carrier is shown on the following page. The following color coding is used on the block diagram:

- Industry standard wired I/O connectors are shown in orange.
- Embedian defined wired I/O connectors and headers are shown in red.
- Industry standard mezzanine and slot format connectors are shown in blue.
- ICs on the board are shown in pale yellow.
- Miscellaneous features (jumpers, switches) are shown in drab green.

Much may be gleaned from this diagram:

- How SMARC resources are used on the Evaluation Carrier.
- What the major Evaluation Carrier Features are.
- An indication of the power supply architecture.

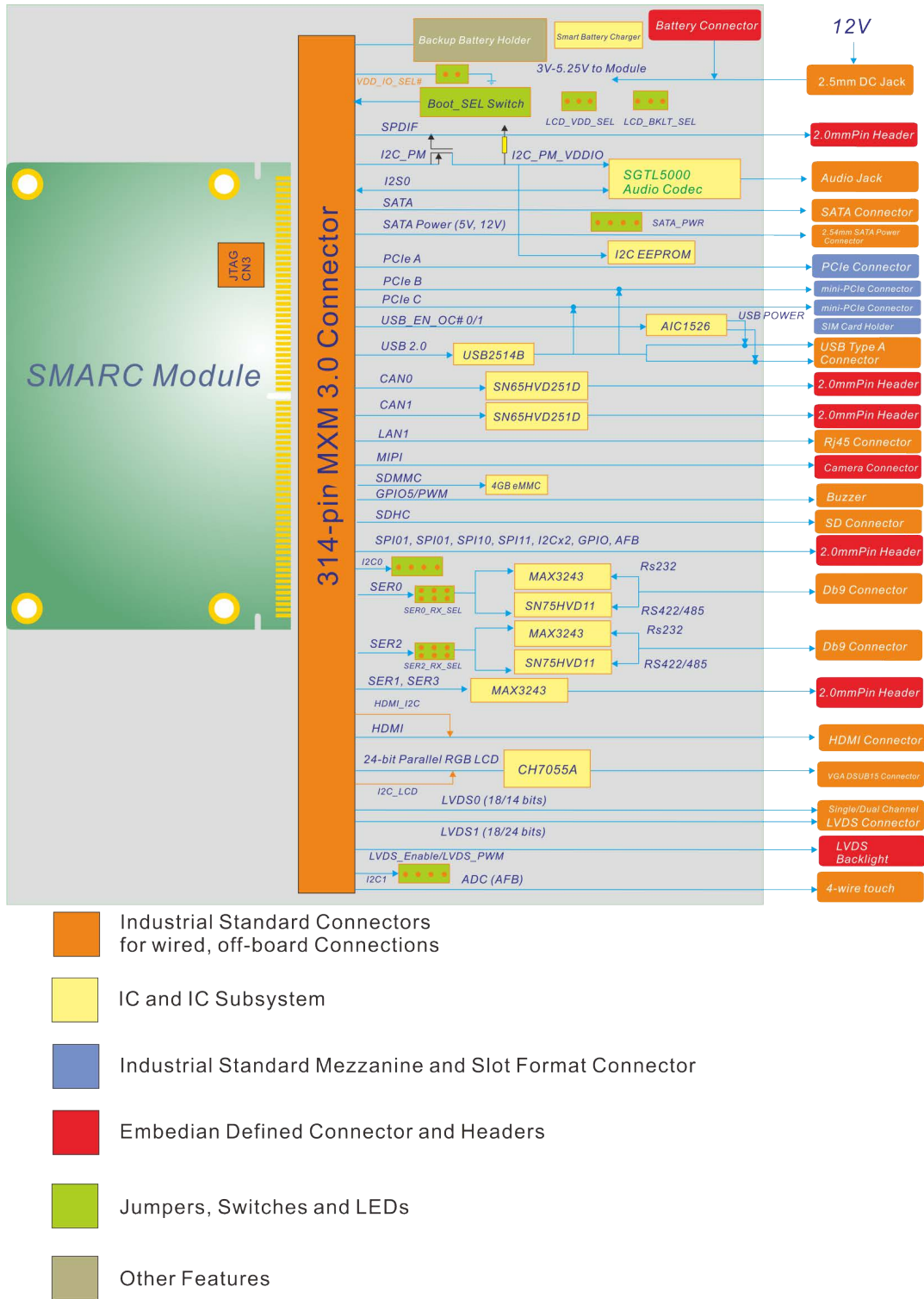


Figure 1: EVK-STD-CARRIER Evaluation Carrier Block Diagram

Details for this diagram will be explained in the following chapters.

1.4 Peripheral Overview

The following diagram shows the function of all peripherals including of connectors, headers, configuration jumpers and other important features on the *EVK-STD-CARRIER* Evaluation Carrier.

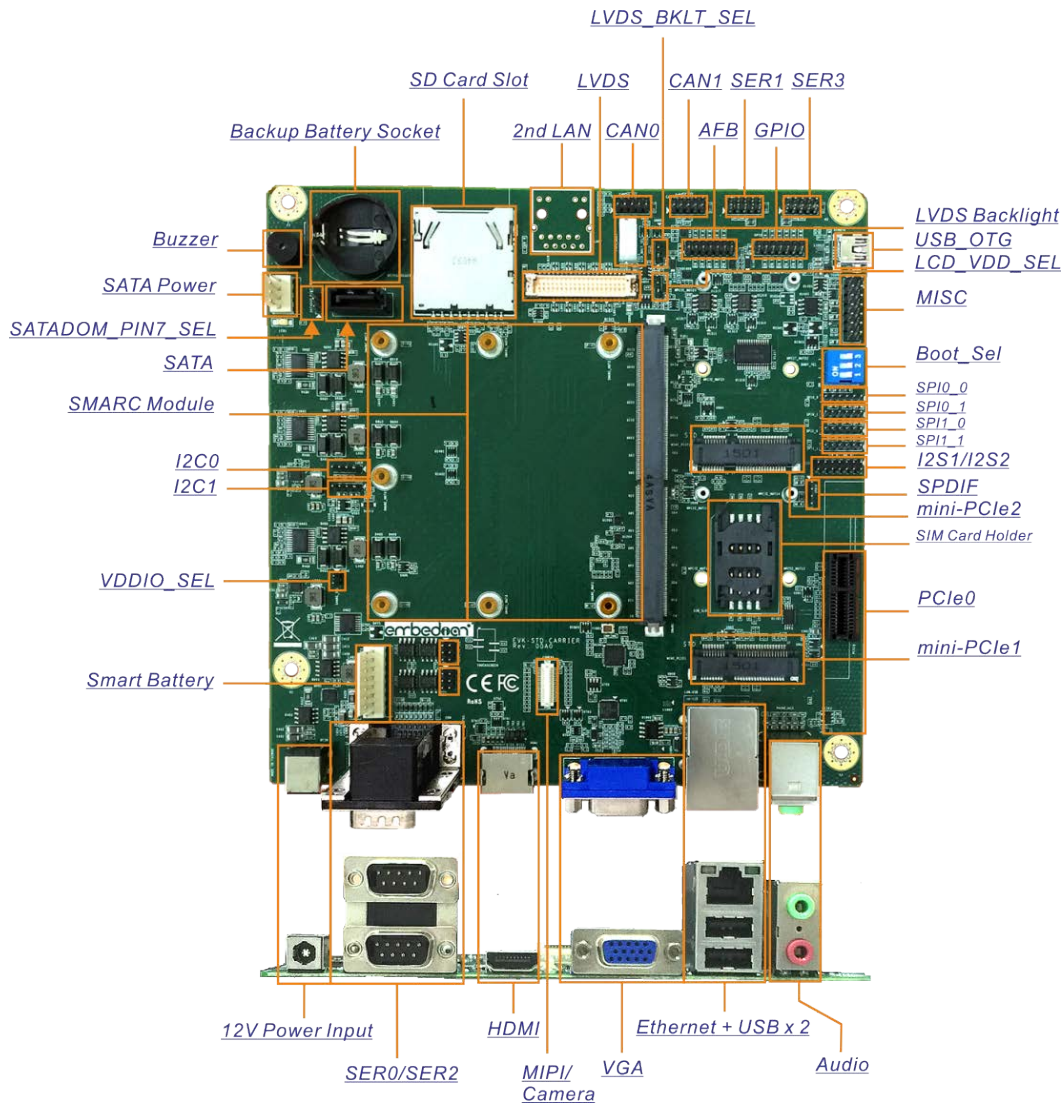


Figure 2: EVK-STD-CARRIER Peripheral Diagram

1.5 Layout Diagram

The following section shows the physical location and reference designator of connectors, configuration jumpers and other important features on the *EVK-STD-CARRIER* Evaluation Carrier.

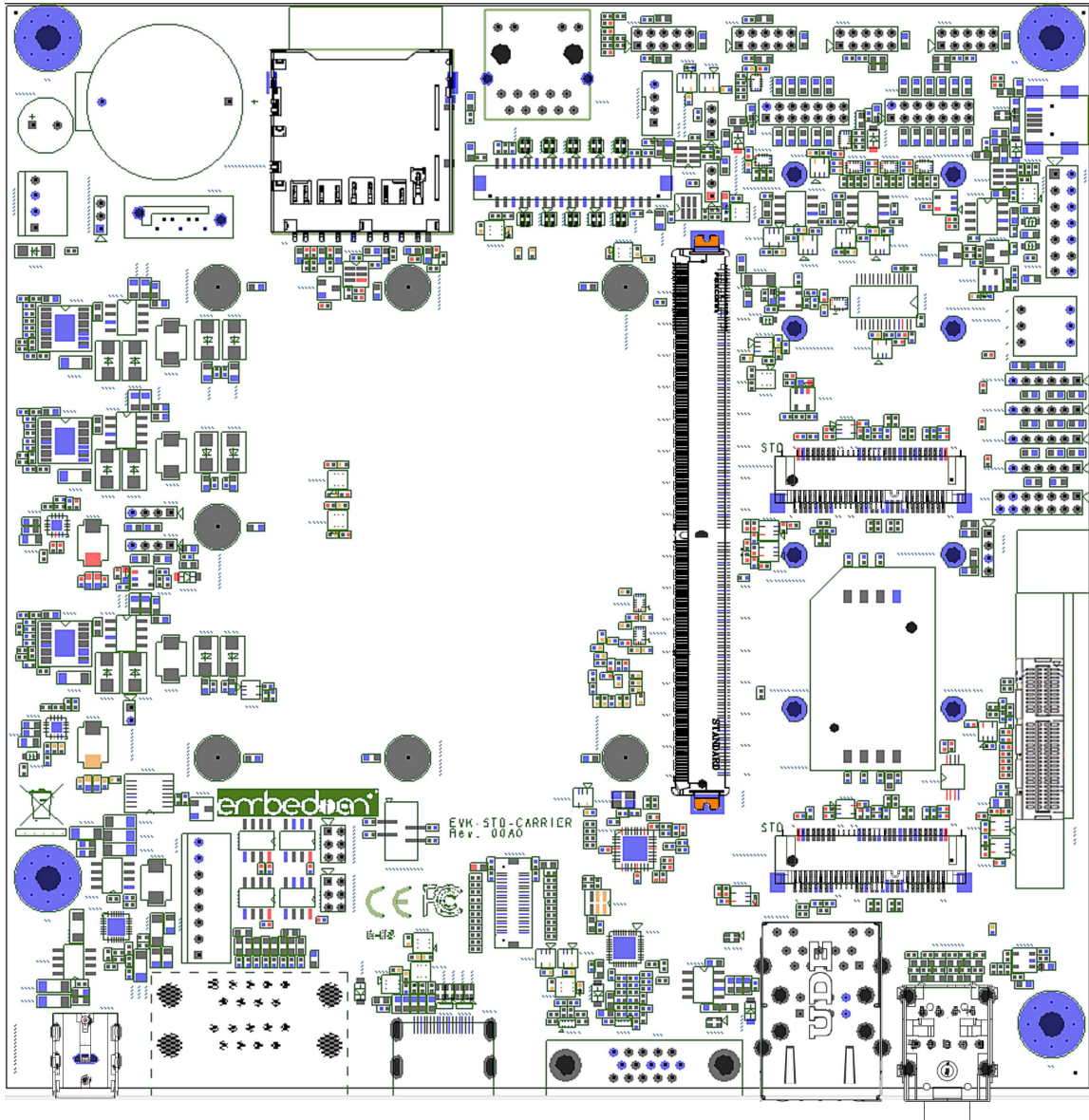


Figure 3: EVK-STD-CARRIER Connectors, Headers and Jumpers

1.6 Mounting Holes Mechanical Drawing

Figure 4 shows the mounting holes information of *EVK-STD-CARRIER*. The diameter of mounting hole is 3.96mm and the diameter of the ring is 6mm.

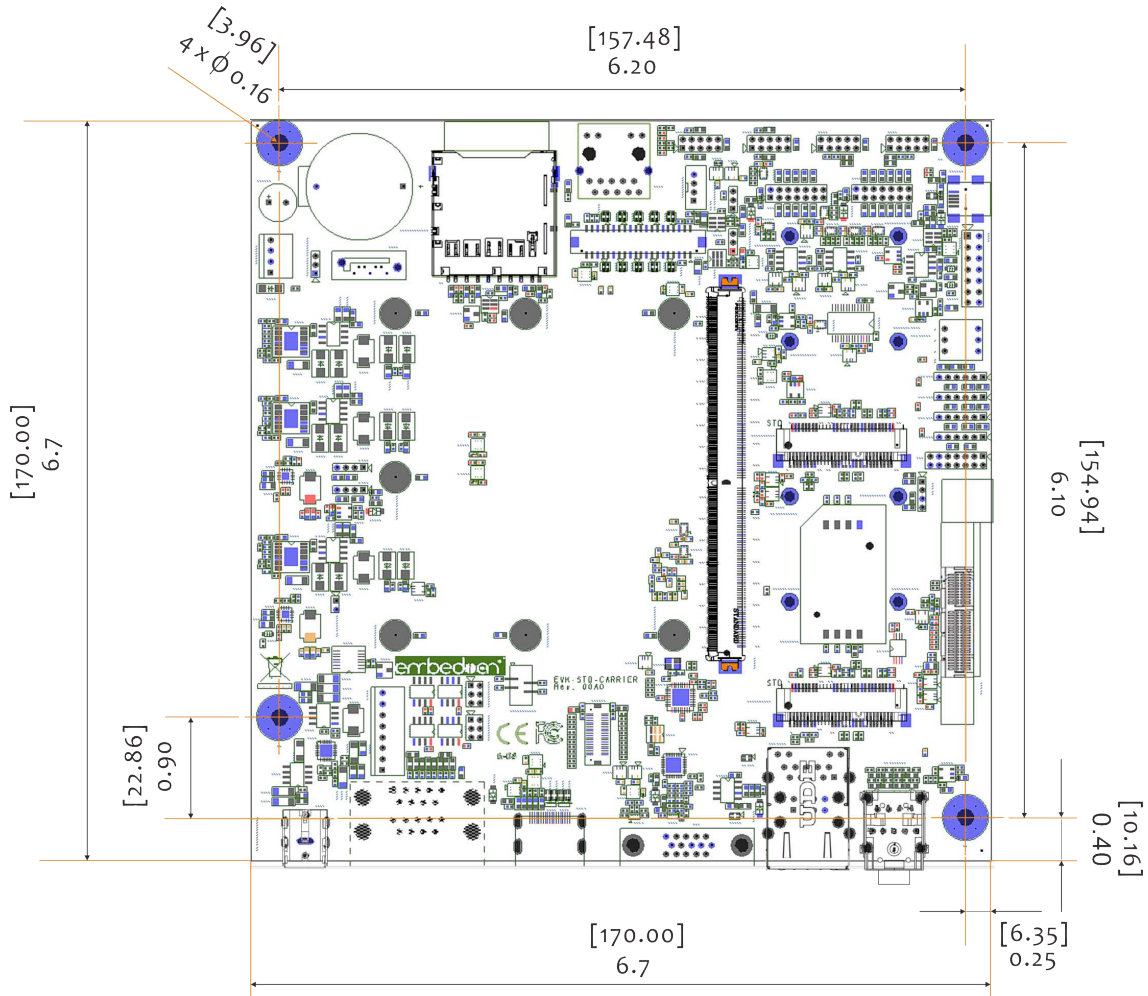


Figure 4: EVK-STD-CARRIER Mounting Holes Mechanical Drawing Information

1.7 Document and Standard References

1.7.1. External Industry Standard Documents

- **eMMC (Embedded Multi-Media Card)** the eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (www.jedec.org).
- **The I2C Specification**, Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com).
- **I2S Bus Specification**, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com).
- **JTAG (Joint Test Action Group)** defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (www.ieee.org).
- **CAN (“Controller Area Network”) Bus Standards** – ISO 11898, ISO 11992, SAE J2411
- **HDMI Specification, Version 1.3a**, November 10, 2006 © 2006 Hitachi and other companies (www.hdmi.org)
- **MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification**, Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (www.mxm-sig.org).
- **PICMG® EEPROM Embedded EEPROM Specification**, Rev. 1.0, August 2010 (www.picmg.org).
- **GBE MDI (“Gigabit Ethernet Medium Dependent Interface”)** This is defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (www.ieee.org)
- **SD Specifications Part 1 Physical Layer Simplified Specification**, Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (www.sdcard.org).
- **SPI Bus** – “Serial Peripheral Interface” - de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia
- **PICMG® EEPROM Embedded EEPROM Specification**, Rev. 1.0, August 2010(www.picmg.org)
- **PCI Express Specifications** (www.pci-sig.org)
- **Serial ATA Revision 3.1, July 18, 2011, Gold Revision**, © Serial ATA International Organization (www.sata-io.org)
- **SPDIF (aka S/PDIF)** (“Sony Philips Digital Interface)- IEC 60958-3
- **USB Specifications** (www.usb.org).

1.7.2. SGET Documents

- ***SMARC_Hardware_Specification_V1p0***, version 1.0, December 20, 2012.
- ***SMARC_Hardware_Specification_V1p1***, version 1.1, May 29, 2014.
- ***SMARC_DG_V1p0***, version 1.0, July 9, 2013.

1.7.3. Embedian Documents

- ***SMARC_T335x Evaluation Carrier Board Schematic***, PDF and OrCAD format
- ***SMARC_T335x Evaluation Carrier Board User's Manual***
- ***SMARC_T335x Carrier Board Hardware Design Guide***
- ***EVK-STD-CARRIER Schematic***, PDF and OrCAD format
- ***SMARC_T335x User's Manual***
- ***SMARC-FiMX6 User's Manual***

Chapter 2

Jumpers, Switches, LEDs and EEPROM

This Chapter provides *EVK-STD-CARRIER* jumpers, switches, *LEDs* and *EEPROM/eMMC* information.

Section include :

- Jumpers
- Switches
- LEDs
- EEPROM and eMMC

Chapter 2 Jumpers, Switches, LEDs and EEPROM

This chapter gives detail information of the jumpers, switches, LEDs and EEPROM/eMMC.

2.1 Jumpers

The *EVK-STD-CARRIER* has a number of jumpers that allow you to configure your system to suit your application. All use 2mm shorting blocks (shunts) to select settings. Turn off power to the *EVK-STD-CARRIER* before changing the position of a shunt.

2.1.1. Jumper Location

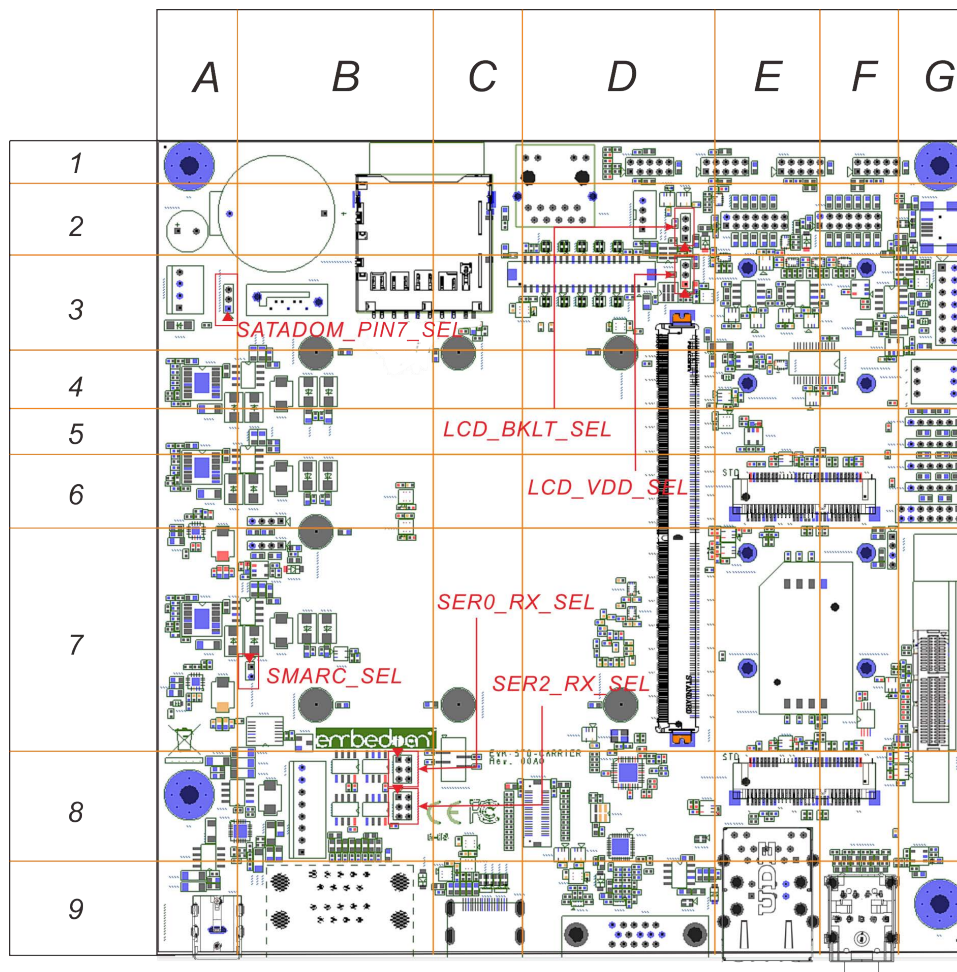


Figure 5: Jumper Locations

2.1.2. List of Jumpers


The table below lists the function of various jumpers.

Label	Function
LCD_VDD_SEL	3.3V/5V LCD Signaling Voltage
LCD_BKLT_SEL	5V/12V LCD Backlight Voltage
SER0_RX_SEL	RS232/RS422/RS485 Setting for SER0 (UART0)
SER2_RX_SEL	RS232/RS422/RS485 Setting for SER2 (UART2)
SATADOM_PIN7_SEL	GND/5V SATADOM Pin7 Selection
SMARC_SEL	SMARC VDDIO 1.8V or 3.3V Selection


2.1.3. Jumper Settings

The following tables describe how the jumper shunts to various configurations.


LCD_VDD_SEL: Location on Board, D3

LCD_VDD_SEL	3.3V/5V LCD Signaling Voltage	
	Setting	Function
	LCD_VDD_SEL (1-2)	3.3V
	LCD_VDD_SEL (2-3)	5V

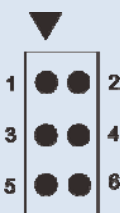
LCD_BKLT_SEL: Location on Board, D2

LCD_BKLT_SEL		5V/12V LCD Backlight Voltage	
	Setting	Function	
	LCD_BKLT_SEL (1-2)	5V	
	LCD_BKLT_SEL (2-3)	12V	


SER0_RX_SEL: Location on Board, B8

SER0_RX_SEL		RS232/RS422/RS485 Settings	
	Setting	Function	
	SER0_RX_SEL (1-2)	RS232	
	SER0_RX_SEL (3-4)	RS422/RS485 half duplex	
	SER0_RX_SEL (5-6)	RS422/RS485 full duplex	

SER2_RX_SEL: Location on Board, B8

SER2_RX_SEL		RS232/RS422/RS485 Settings	
	Setting	Function	
	SER2_RX_SEL (1-2)	RS232	
	SER2_RX_SEL (3-4)	RS422/RS485 half duplex	
	SER2_RX_SEL (5-6)	RS422/RS485 full duplex	

SATADOM_PIN7_SEL: Location on Board, A3

SATADOM_PIN7_SEL SATA-DOM Jumper (Power +5V pin7)		
	Setting	Function
	SATADOM_PIN7_SEL (1-2)	GND
	SATADOM_PIN7_SEL (2-3)	5V

SMARC_SEL: Location on Board, B7

SMARC_SEL SMARC VDDIO 1.8V or 3.3V Selection		
	Setting	Function
	SMARC_SEL Open	3.3V VDDIO (SMARC 1.0 Compliant) SMARC module
	SMARC_SEL Closed	1.8V VDDIO (SMARC 1.1 Compliant) SMARC module



Make sure power is complete *OFF* when changing settings of SMARC_SEL.

2.1.4. Setting Jumpers

You configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip.

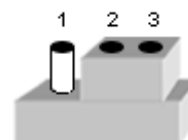
To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2 or 2 and 3.



Open

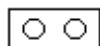


Closed



Closed 2-3

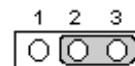
The jumper settings are schematically depicted in this manual as follows.



Open



Closed



Closed 2-3

A pair of needle-nose pliers may be helpful when working with jumpers. If you have any doubts about the best hardware configuration for your application, contact your sales representative before you make any change.

2.2 Switches

The *EVK-STD-CARRIER* has one switch (*BOOT_SEL*) that could determine the boot devices.

2.2.1. Switch Location

The *BOOT_SEL* switch for boot configuration is located at *G4* as shown in the following figure.

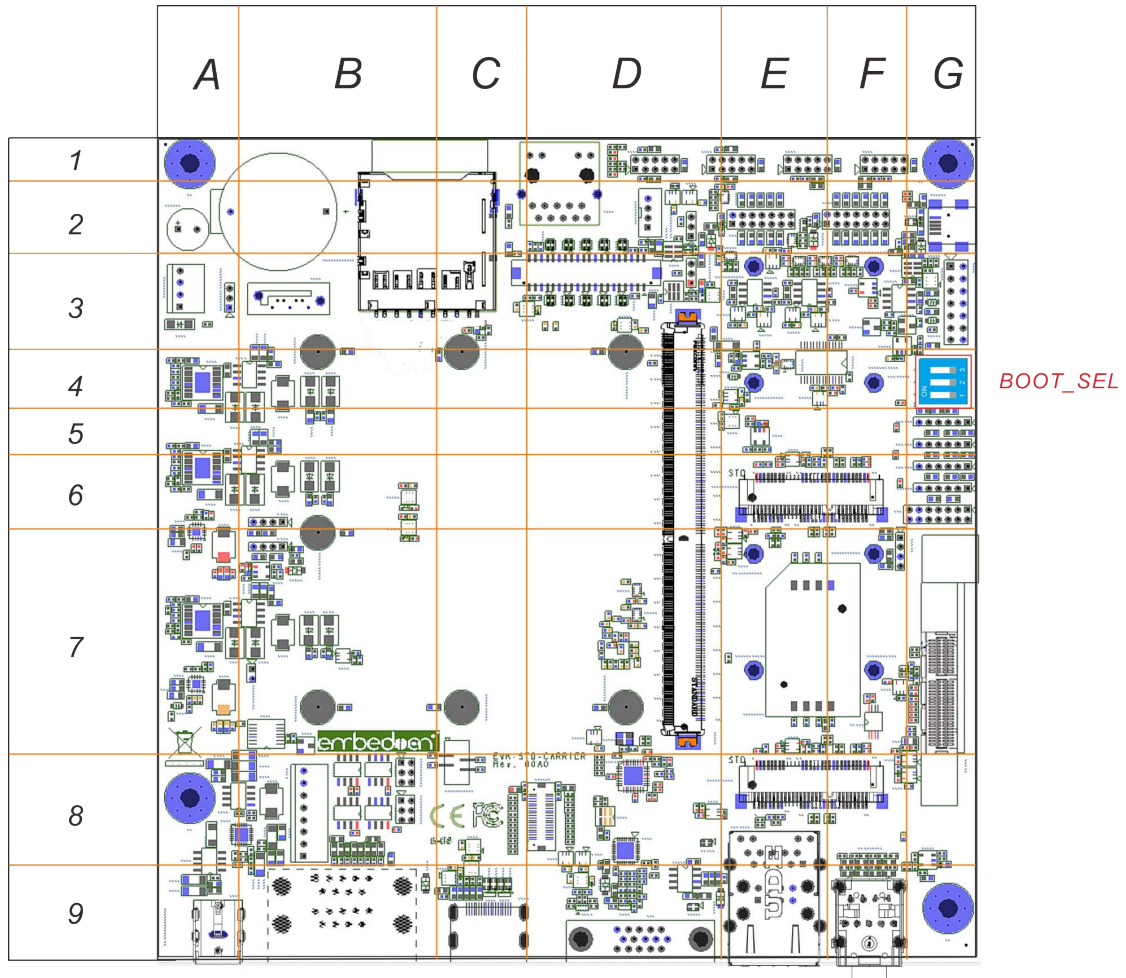


Figure 6: Switch Locations

2.2.2. List of Booting Device Configuration

The table below lists the booting device configuration setting by *BOOT_SEL*.

<i>Boot_Sel</i>			<i>Function</i>
1	2	3	Boot Configuration
<i>OFF</i>	<i>OFF</i>	<i>OFF</i>	<i>Carrier SATA</i>
<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>Carrier SD Card</i>
<i>OFF</i>	<i>ON</i>	<i>OFF</i>	<i>Carrier eMMC Flash</i>
<i>ON</i>	<i>ON</i>	<i>OFF</i>	<i>Carrier SPI</i>
<i>OFF</i>	<i>OFF</i>	<i>ON</i>	<i>Module Device (Vendor Specific)</i>
<i>ON</i>	<i>OFF</i>	<i>ON</i>	<i>Remote Boot (Vendor Specific)</i>
<i>OFF</i>	<i>ON</i>	<i>ON</i>	<i>Module eMMC Flash</i>
<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>Module SPI</i>

2.3 LEDs

The *EVK-STD-CARRIER* has one LED to indicate the *SATA_ACT#* signal. The *LED* plays a role as *SATA* activity indicator.

2.3.1. LED Location

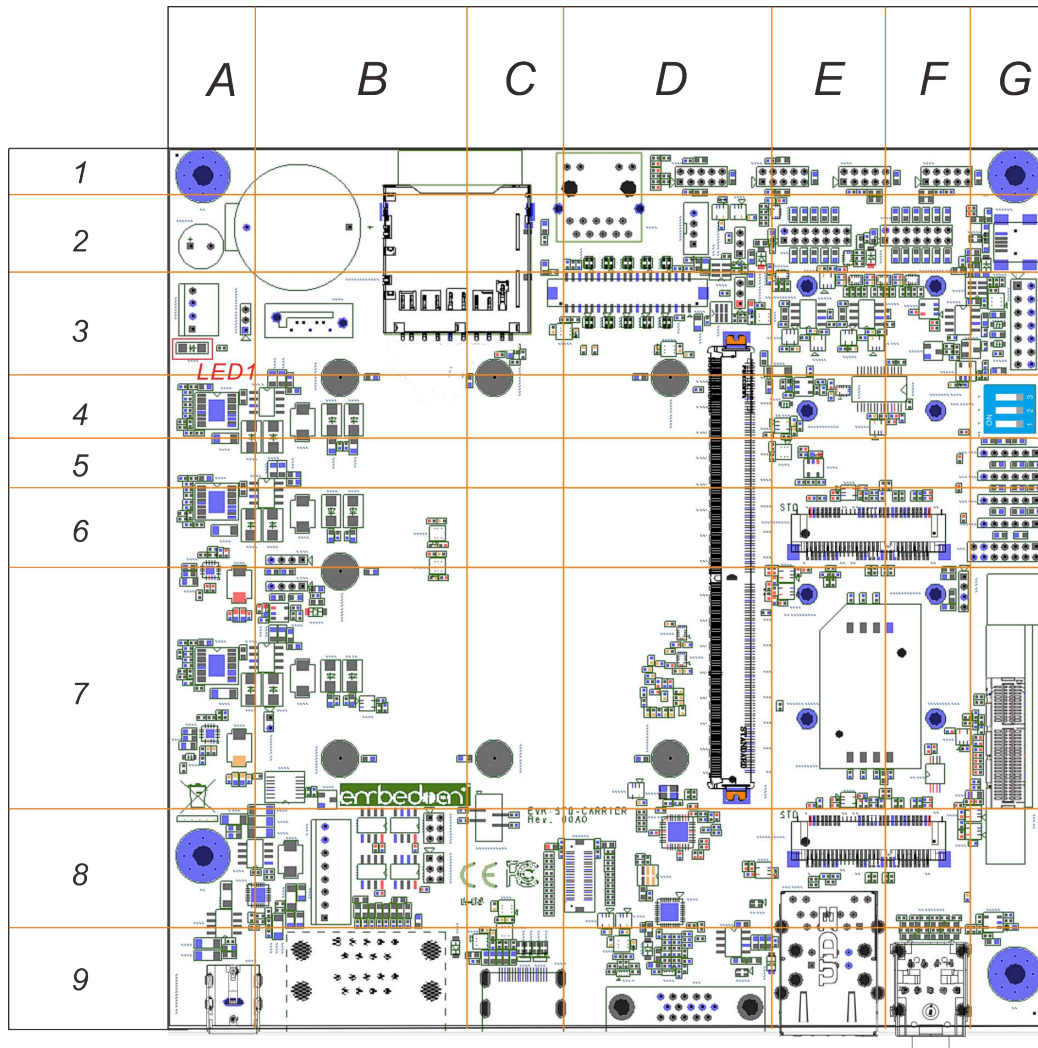


Figure 7: LED Locations

2.3.2. List of LEDs

The table below lists the function of LEDs.

Label	Function
LED1	<i>ON when there is activity on the SATA Lane</i>

2.4 EEPROM and eMMC

An *I2C AT24c32 EEPROM* is on *EVK-STD-CARRIER* and is intended to retain carrier board parameter information, including a carrier serial number. The *I2C* bus is *I2C_PM* from *SMARC* module and address is *0x57*.

An 8-bit 4GB *eMMC* is also present on *EVK-STD-CARRIER* from *SDMMC* bus of *SMARC* interface.

Chapter 3

Rear I/O Panel and Internal I/O Headers

This Chapter gives *EVK-STD-CARRIER* connectors and headers detail information.

Section include :

- Rear I/O Panel
- Internal I/O Headers

Chapter 3 Headers and Connectors

This section gives *EVK-STD-CARRIER* connectors and headers detail information.

3.1 Rear I/O Panel

Rear panel I/O connectors of *EVK-STD-CARRIER* Evaluation Carrier are described in this section.

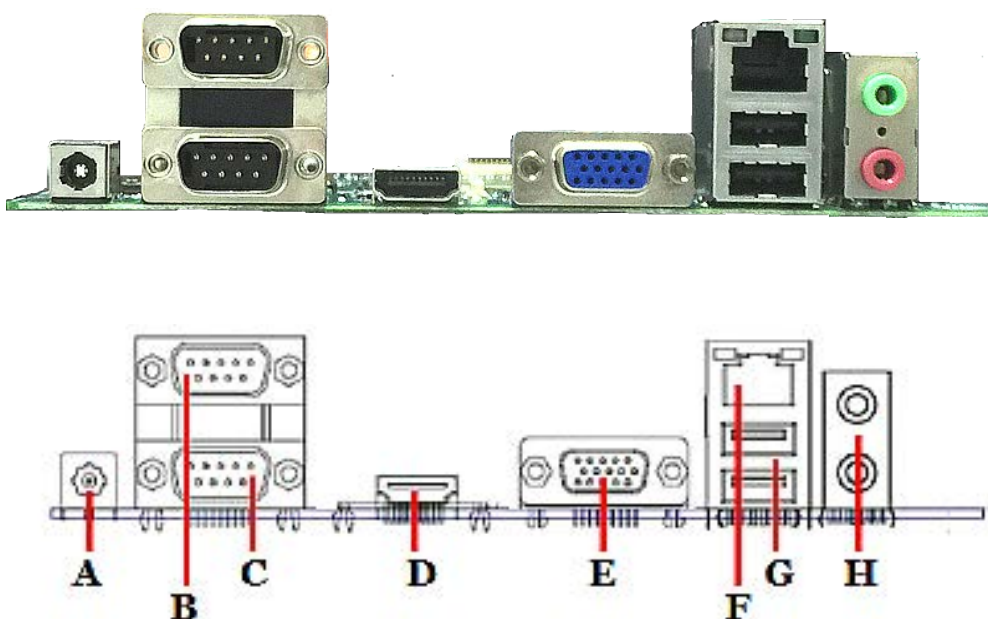


Figure 8: Rear I/O Connectors

3.1.1. List of Connectors

The table below lists the function of various connectors.

<i>Label</i>	<i>Description</i>	<i>Connector Type</i>
<i>DC_IN</i>	<i>12V Power Input DC Jack</i>	<i>DC POWER JACK 2.5mm 90D(M) DIP 2DCG213B200</i>
<i>COMA</i>	<i>UART Port 0</i>	<i>D-Sub 9M/9M Dual port</i>
<i>COMB</i>	<i>UART Port 2</i>	<i>D-Sub 9M/9M Dual port</i>
<i>HDMI</i>	<i>HDMI Port</i>	<i>HDMI Female smt 19p</i>
<i>VGA</i>	<i>VGA Port</i>	<i>D-sub h=3.08 Female 15p</i>
<i>LAN + USB</i>	<i>GbE Ethernet RJ45 and dual USB Host Type A Connector</i>	<i>RJ45 Tab up over USB 2.0 stack 10/100/1000 Base-T LED: L-G/0; R-G</i>
<i>PhoneJack</i>	<i>Mic. Input / Headphone Output</i>	<i>3.5mm Phone jack 90 2x01</i>

3.1.2. Connector Pin Assignments

The following tables describe the electrical signals available on the connectors of the *EVK-STD-CARRIER*. Each section provides relevant details about the connector including part numbers, mating connectors, signal descriptions and references to related chapters.

Pinout Legend


<i>I</i>	<i>Input</i>
<i>O</i>	<i>Output</i>
<i>I/O</i>	<i>Input or output</i>
<i>P</i>	<i>Power</i>
<i>AI</i>	<i>Analogue input</i>
<i>AO</i>	<i>Analogue output</i>
<i>AIO</i>	<i>Analogue Input or analogue output</i>
<i>OD</i>	<i>Open Drain Signal</i>
<i>#</i>	<i>Low level active signal</i>

3.1.2.1. DC Jack Power Input Connector: DC_IN

EVK-STD-CARRIER accepts DC +12V ~ DC +24V as the power input source. The power supply to SMARC CPU module is 5V via a power management IC on EVK-STD-CARRIER.

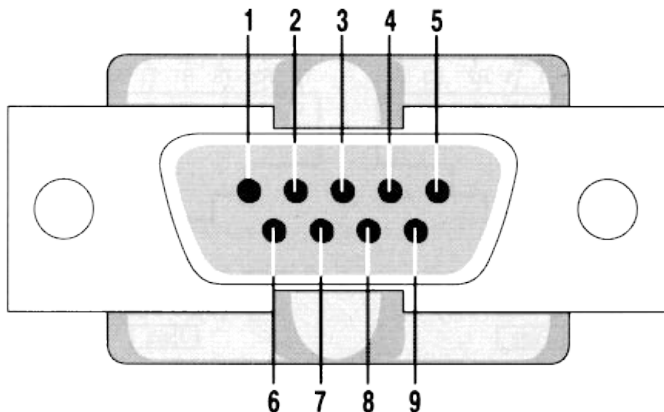
The following table shows the pin-out of the DC_IN power jack connector.

DC_IN: Location on Board, A

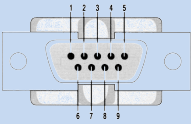
12V DC Jack Power Input					Edge Finger	Type
DC POWER JACK 2.5mm 90D(M) DIP 2DCG213B200						
Header	Pin	Signal Name	Function	Pin#		
	1	12V	DC 12V Power Input	-		P
	2	Shield	Ground Power	-		P

3.1.2.2. RS232/422/485 Port 0 Connector (4-Wire): COMA

The following table shows the pin-out of the COMA connector.

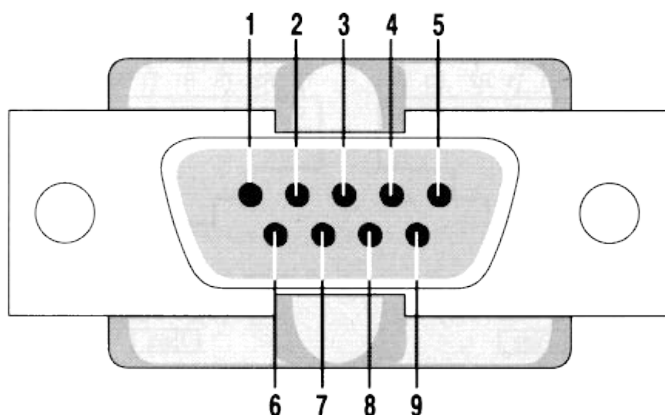


COMA: Location on Board, B

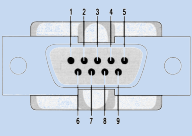
RS232/422/485 Port0 Connector					Edge Finger	Type
D-Sub 9M/9M Dual port (Up)						
Header	Pin	Signal Name	Function	Pin#		
	1	RS422_0_TX+/ RS485_0_RX+		-		
	2	COM0_RXD	Receive Data	P130	I	
	3	COM0_TXD	Transmit Data	P129	O	
	4	RS422_0_RX+		-		
	5	GND		-		
	6	RS422_0_TX-/ RS485_0_RX-		-		
	7	COM0_RTS	Ready to Send	P131	O	
	8	COM0_CTS	Clear To Send	P132	I	
	9	RS422_0_RX-		-		

3.1.2.3. RS232/422/485 Port 2 Connector (4-Wire): COMB

The following table shows the pin-out of the COMB connector.

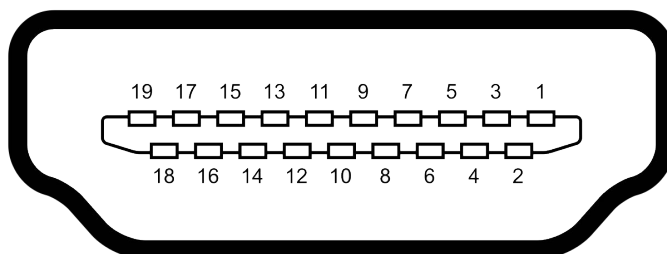


COMA: Location on Board, C

RS232/422/485 Port2 Connector					Edge Finger	Type
D-Sub 9M/9M Dual port (Down)						
Header	Pin	Signal Name	Function	Pin#		
	1	RS422_2_TX+/ RS485_2_RX+		-		
	2	COM2_RXD	Receive Data	P137	I	
	3	COM2_TXD	Transmit Data	P136	O	
	4	RS422_2_RX+		-		
	5	GND		-		
	6	RS422_2_TX-/ RS485_2_RX-		-		
	7	COM2_RTS	Ready to Send	P138	O	
	8	COM2_CTS	Clear To Send	P139	I	
	9	RS422_2_RX-		-		

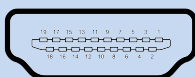
3.1.2.4. HDMI Connector: HDMI

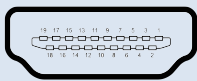
The following table shows the pin-out of the *HDMI* connector.



HDMI: Location on Board, D

HDMI Connector				Edge Finger	Type
HDMI Female smt 19p					
Header	Pin	Signal Name	Function	Pin#	
	1	TMDS_D2+	TMDS / HDMI data differential pair 2	P92	O
	2	GND	Ground	-	P
	3	TMDS_D2-	TMDS / HDMI data differential pair 2	P93	O
	4	TMDS_D1+	TMDS / HDMI data differential pair 1	P95	O
	5	GND	Ground	-	P
	6	TMDS_D1-	TMDS / HDMI data differential pair 1	P96	O
	7	TMDS_D0+	TMDS / HDMI data differential pair 0	P98	O
	8	GND	Ground	-	P
	9	TMDS_D0-	TMDS / HDMI data differential pair 0	P99	O
	10	TMDS_CK+	HDMI differential clock output pair	P101	O
	11	GND	Ground	-	P
	12	TMDS_CK-	HDMI differential clock output pair	P102	O

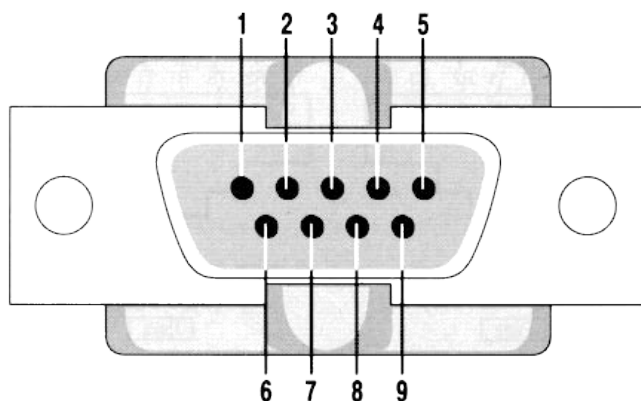


HDMI Connector					Edge Finger	Type
HDMI Female smt 19p						
Header	Pin	Signal Name	Function	Pin#		
	13	CEC	HDMI Consumer Electronics Control 1-wire peripheral control interface	P107		IO/OD
	14	-	-	-		-
	15	SCL	I2C Clock	P105		IO/OD
	16	SDA	I2C Data	P106		IO/OD
	17	GND	Ground	-		P
	18	+5V	5V Power	-		P
	19	HPD	HDMI Hot Plug Detect input	P104		I

3.1.2.5. VGA Connector: VGA

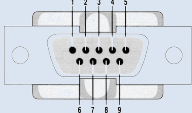
VGA signals are converted from 24-bit parallel *rgb* data by Chrontel *CH7055A*. The maximum conversion resolutions for *CH7055A* are 1920x1200.

The following table shows the pin-out of the VGA connector.



VGA: Location on Board, E

VGA Connector					Edge Finger	Type
D-sub h=3.08 Female 15p						
Header	Pin	Signal Name	Function	Pin#		
	1	VGA_R_Z	Red Videl	-		IO
	2	VGA_G_Z	Green Video	-		IO
	3	VGA_B_Z	Blue Video	-		IO
	4	-	-	-		-
	5	GND	Ground	-		P
	6	GND	Ground	-		P
	7	GND	Ground	-		P
	8	GND	Ground	-		P
	9	+5V	5V Power	-		P

VGA Connector					Edge Finger	Type
D-sub h=3.08 Female 15p						
Header	Pin	Signal Name	Function	Pin#		
	10	GND	Ground	-		P
	11	-	-	-		-
	12	VGA_Z_SDA	I2C Data	S140		IO/OD
	13	VGA_Z_HSYC	Horizontal Sync	S122		O
	14	VGA_Z_VSYNC	Vertical Sync	S121		O
	15	VGA_Z_SCL	I2C Clock	S139		IO/OD

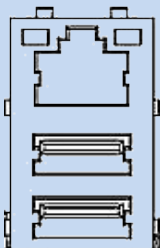
Note:

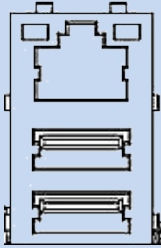
The *I2C_LCD* slave address for *CH7055A* is *0x76*.

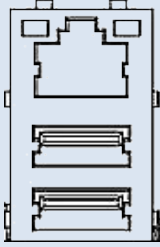
3.1.2.6. RJ45 & USB 1/2 Connector: LAN + USB

The USB signals are originated from USB1 port of SMARC module connecting to a 4-port USB hub *USB2514B* from Microchip. Two ports are present in this LAN+USB connector. The other two ports are present at mini-PCIE connectors. A GigaLAN magnet is built in the RJ45 connector. The following table shows the pin-out of the *LAN+USB* connector.

LAN+USB: Location on Board, F

LAN+USB Connector					Edge Finger	Type
RJ45 Tab up over USB 2.0 stack 10/100/1000 Base-T LED: L-G/0; R-G						
Header	Pin	Signal Name	Function	Pin#		
LAN+USBA (RJ45)						
	1	GBE_CTREF	Center tap reference voltage for GBE Carrier board Ethernet magnetic	P28		O
	2	GBE_MDI0+	Differential Transmit/Receive Positive Channel 0	P30		AIO
	3	GBE_MDI0-	Differential Transmit/Receive Negative Channel 0	P29		AIO
	4	GBE_MDI1+	Differential Transmit/Receive Positive Channel 1	P27		AIO
	5	GBE_MDI1-	Differential Transmit/Receive Negative Channel 1	P26		AIO
	6	GBE_MDI2+	Differential Transmit/Receive Positive Channel 2	P24		AIO
	7	GBE_MDI2-	Differential Transmit/Receive Negative Channel 2	P23		AIO
	8	GBE_MDI3+	Differential Transmit/Receive Positive Channel 3	P20		AIO
	9	GBE_MDI3-	Differential Transmit/Receive Negative Channel 3	P19		AIO
	10	GND	Ground		-	

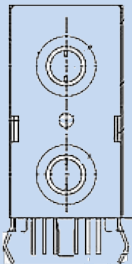
LAN+USB Connector					Edge Finger	Type
RJ45 Tab up over USB 2.0 stack 10/100/1000 Base-T LED: L-G/0; R-G						
Header	Pin	Signal Name	Function	Pin#		
	LAN+USBA (RJ45)					
	11	GBE_LINK_ACK#	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps)	P25	O	OD
	12	3.3V	3.3V Power	-	P	
	13	GBE_LINK1000#	Link Speed Indication LED for 1000Mbps	P22	O	OD
	14	GBE_LINK100#	Link Speed Indication LED for 100Mbps	P21	O	OD

LAN+USB Connector					Edge Finger	Type
RJ45 Tab up over USB 2.0 stack 10/100/1000 Base-T						
LED: L-G/0; R-G						
<i>Header</i>	<i>Pin</i>	<i>Signal Name</i>	<i>Function</i>	<i>Pin#</i>		
	LAN_USBB (USB Port 2)					
	15	5V	USB 1 Power Supply	-	P	
	16	USB_UZ_D-	Universal serial bus port 1 (-)	-	IO	
	17	USB_UZ_D+	Universal serial bus port 1 (+)	-	IO	
	18	GND	Ground	-	P	
	LAN_USBC (USB Port 1)					
	19	5V	USB 2 Power Supply	-		
	20	USB_LZ_D-	Universal serial bus port 2 (-)	-		
	21	USB_LZ_D+	Universal serial bus port 2 (+)	-		
	22	GND	Ground	-		

3.1.2.7. Audio Connector: PhoneJack

The following table shows the pin-out of the *PhoneJack* connector.

PhoneJack: Location on Board, H

PhoneJack Connector					Edge Finger	Type
3.5mm Phone jack 90 2x01						
Header	Pin	Signal Name	Function	Pin#		
	1	GND	Ground	-	P	
	2	-	-	-	-	
	3	-	-	-	-	
	4	-	-	-	--	
	5	MIC In.	Microphone Input	-	AI	
	6	-	-	-	-	
	7	Adio_L	Left channel of headset speaker	-	AO	
	8	-	-	-	-	
	9	Audio_R	Right channel of headset speaker	-	AO	

3.2 Internal I/O Headers

This section details the internal I/O header and connector information of EVK-STD-CARRIER Evaluation Carrier.

3.2.1. Location

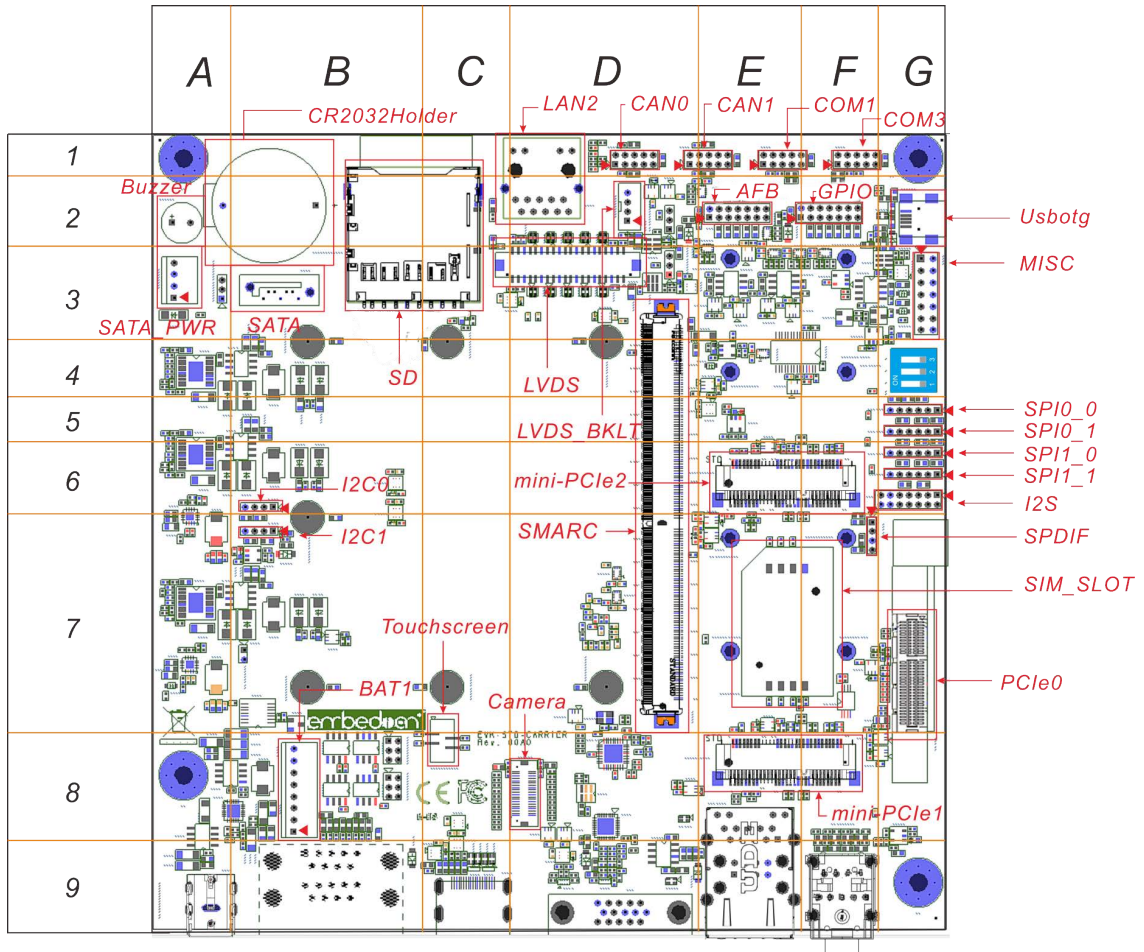


Figure 9: Internal I/O Header Locations

3.2.2. List of Headers

The table below lists the function of various headers.

Label	Description	Connector Type
BAT1	<i>Lithium-ion Battery power input pin header</i>	<i>WAFER 8P 2.54mm 180D(M) DIP A2543WV2-8P</i>
Camera	<i>2 LANEs and 4 LANEs Camera Connector</i>	<i>B/B CONN. 2x20P 0.5mm 180D(M) SMD DF12(3.0)-30D</i>
SATA	<i>SATA Connector</i>	<i>Serial ATA 7P 1.27mm 180D(M) DIP WATM-07DBN4A3B8</i>
SATA_PWR	<i>SATA Power Connector</i>	<i>WAFER 4P 2.5mm 180D(M) DIP 24W1161-04S10-01T</i>
PCIE0	<i>PClex1 Connector</i>	<i>PCIEXPRESS 36P 180D(F) DIP 2EG01817-D2D-DF</i>
Mini-PCIE1	<i>PCI Express Mini Card</i>	<i>0.80mm Pitch, 5.20mm Height, PCI Express* Mini Card, 52 Circuit, Right Angle, Surface Mount, 0.25µm Gold (Au) Plating</i>
Mini-PCIE2	<i>PCI Express Mini Card</i>	<i>0.80mm Pitch, 5.20mm Height, PCI Express* Mini Card, 52 Circuit, Right Angle, Surface Mount, 0.25µm Gold (Au) Plating</i>
SIM_SLOT	<i>SIM Card Holder</i>	<i>Sim card hinged lock</i>
LVDS	<i>LVDS Connector</i>	<i>B/B Conn. 40P 1.25mm 90D SMD DF13-40DP-1.25V(91)</i>
LVDS_BKLT	<i>LVDS Backlight Power</i>	<i>WAFER BOX 2.0mm 4P 180D(M) DIP WO/Pb JIH VEI</i>
SD	<i>SD/SDHC Connector</i>	<i>Right Angle, SMT, 2.75mm height, Push Push Normal Type With Detect Switch</i>

Label	Description	Connector Type
Usbotg	USB OTG Connector	USB OTG mini Type B Connector
SPI0_0	SPI0 CS0 Pin Header	PIN HEADER 1x6P 2.00mm 180D(M) SMD
SPI0_1	SPI0 CS1 Pin Header	PIN HEADER 1x6P 2.00mm 180D(M) SMD
SPI1_0	SPI1 CS0 Pin Header	PIN HEADER 1x6P 2.00mm 180D(M) SMD
SPI1_1	SPI1 CS1 Pin Header	PIN HEADER 1x6P 2.00mm 180D(M) SMD
I2S	I2S1 and I2S2 Pin Header	PIN HEADER 2x7P 2.00mm 180D(M) SMD
SPDIF	SPDIF Pin Header	PIN HEADER 1x4P 2.00mm 180D(M) SMD
GPIO	GPIO Pin Header	PIN HEADER 2x7P 2.00mm 180D(M) SMD
MISC	Misc. Signals Pin Header	PIN HEADER 2x7P 2.54mm 180D(M) SMD
AFB	AFB Signals Pin Header	PIN HEADER 2x7P 2.00mm 180D(M) SMD
CAN0	CAN0 Bus Pin Header	PIN HEADER 2x5P 2.00mm 180D(M) SMD
CAN1	CAN1 Bus Pin Header	PIN HEADER 2x5P 2.00mm 180D(M) SMD
COM1	SER1 RS232 Pin Header	PIN HEADER 2x5P 2.00mm 180D(M) SMD
COM3	SER3 RS232 Pin Header	PIN HEADER 2x5P 2.00mm 180D(M) SMD

Label	Description	Connector Type
I2C0	<i>I2C_GP Pin Header</i>	<i>PIN HEADER 1x4P 2.00mm 180D(M) SMD</i>
I2C1	<i>I2C_CAM Pin Header</i>	<i>PIN HEADER 1x4P 2.00mm 180D(M) SMD</i>
Buzzer	<i>Buzzer Connector</i>	<i>ELECTRO MAGNETIC BUZZER</i>
CR2032Holder	<i>CR-2032 Backup Battery Holder</i>	<i>BATTERY HOLDER 24.9*23.4*8.9 CR2032 BH800.4GG</i>
Touchscreen(*)	<i>4-wire resistive touch connector</i>	<i>1.0 ZIF FPC SMT V/T</i>
LAN2(**)	<i>LAN2 Connector</i>	<i>RJ45 1x1 Tab down Through Hole Gold Flash 10/100/1000 Base=T LED:L-Y;R-O/G</i>
SMARC	<i>MXM3.0 Connector</i>	<i>MXM 3.0 SOCKET,314POTS,7.8MM HEIGHT</i>

3.2.3. Header Pin Assignments

The following tables describe the electrical signals available on the connectors of the *EVK-STD-CARRIER*. Each section provides relevant details about the connector including part numbers, mating connectors, signal descriptions and references to related chapters.

Pinout Legend

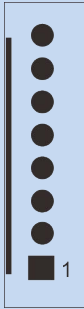
<i>I</i>	<i>Input</i>
<i>O</i>	<i>Output</i>
<i>I/O</i>	<i>Input or output</i>
<i>P</i>	<i>Power</i>
<i>AI</i>	<i>Analogue input</i>
<i>AO</i>	<i>Analogue output</i>
<i>AIO</i>	<i>Analogue Input or analogue output</i>
<i>OD</i>	<i>Open Drain Signal</i>
<i>#</i>	<i>Low level active signal</i>

3.2.3.1. Lithium-ion Battery power input pin header: BAT1

EVK-STD-CARRIER uses TI BQ24770 NVDC-1 battery charge controllers. It allows the system to be regulated at battery voltage but does not drop below system minimum voltage. With this feature, the system keeps operating even when the battery is completely discharged or removed.

The following table shows the pin-out of the *BAT1* connector.

Bat1: Location on Board, B8

Lithium-ion Battery power input pin header					Edge Finger	Type
WAFER 8P 2.54mm 180D(M) DIP A2543WV2-8P						
Header	Pin	Signal Name	Function	Pin#		
	1	+VDD_BAT	Battery Supply Voltage	-		P
	2	+VDD_BAT	Battery Supply Voltage	-		P
	3	I2C_PM_DAT_3V3	Power management I2C bus data	P122		IO OD
	4	I2C_PM_CLK_3V3	Power management I2C bus clock	P121		IO OD
	5	BAT_ID	Battery Presence Detection	-		O
	6	BAT_THRM#	Battery Presence Detection			O
	7	GND	Ground	-		P
	8	GND	Ground	-		P

Note:

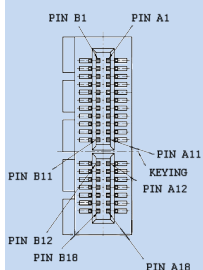
The I2C address for TI BQ24770 smart charger IC is 0x09 and connects to I2C_PM bus from SMARC module.

3.2.3.2. PCIe x1 Card Slot: PCIE0

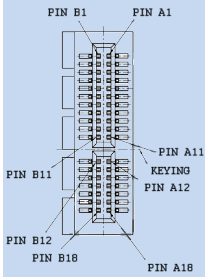
The signals of PCIe x1 card slot are originated from PCIE_A of SMRAC card. The following table shows the pin-out of the PCIE0 connector.

PCIE0: Location on Board, G7

PCIe x1 Card Slot				Edge Finger	Type
PCIEXPRESS 36P 180D(F) DIP 2EG01817-D2D-DF					
Header	Pin	Signal Name	Function	Pin#	
Side A Connector					
	A1	PCIE_A_PRSENT1#	Hot plug presence detect	P74	I
	A2	+12V	+12V Power	-	P
	A3	+12V	+12V Power	-	P
	A4	GND	Ground	-	P
	A5	PCIEA_JTAG2	TCK	-	I
	A6	PCIEA_JTAG3	TDI	-	I
	A7	PCIEA_JTAG4	TDO	-	O
	A8	PCIEA_JTAG5	TMS	-	I
	A9	+3.3V	+3.3V Power	-	P
	A10	+3.3V	+3.3V Power	-	P
	A11	PWRGD	Power Good	-	O
Mechanical Key					
	A12	GND	Ground	-	P
	A13	PCIE_A_REFCK+	Reference Clock Differential	P83	O
	A14	PCIE_A_REFCK-	Pair	P84	O
	A15	GND	Ground	-	P
	A16	PCIE_A_RX+	Receiver Lane 0, Differential Pair	P86	I
	A17	PCIE_A_RX-		P87	I
	A18	GND	Ground	-	P

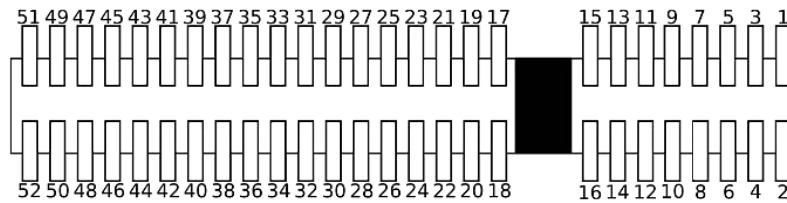


PCIe x1 Card Slot				Edge Finger	Type
PCIEXPRESS 36P 180D(F) DIP 2EG01817-D2D-DF					
Header	Pin	Signal Name	Function	Pin#	
Side B Connector					
	B1	+12V	+12V Power	-	P
	B2	+12V	+12V Power	-	P
	B3	RSVD	Reserved	-	-
	B4	GND	Ground	-	P
	B5	I2C_PM_CK_3V3	I2C Clock	P121	IO OD
	B6	I2C_PM_DAT_3V3	I2C Data	P122	IO OD
	B7	GND	Ground	-	P
	B8	+3.3V	+3.3V Power	-	P
	B9	PCIEA_JTAG1	+TRST#		I
	B10	+3.3V	+3.3V Power	-	P
	B11	PCIE_A_WAKE#	Link Reactivation	S146	I
Mechanical Key					
	B12	RSVD	Reserved	-	-
	B13	GND	Ground	-	P
	B14	PCIE_A_TX+	Transmitter Lane 0, Differential Pair	P89	O
	B15	PCIE_A_TX-		P90	O
	B16	GND	Ground	-	P
	B17	PCIE_A_PRSENT2#	Hot plug presence detect	P74	I
	B18	GND	Ground	-	P



3.2.3.3. mini-PCIE Card Slot: mini-PCIE1

The signals of *mini-PCIE1* card slot are originated from *PCIE_B* of *SMRAC* card. The 3rd set of USB signals are also connected to this connector. The following table shows the pin-out of the *mini-PCIE1* connector.



Mini-PCIE1: Location on Board, E8/F8

Mini-PCIE Card Slot						
0.80mm Pitch, 5.20mm Height, PCI Express* Mini Card, 52 Circuit, Right Angle, Surface Mount, 0.25µm Gold (Au) Plating						
Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	Top Side			Bottom Side		
	1	PCIE_B_WAKE#	Link Reactivation	2	+3.3V	+3.3V Power
	3	RSVD	Reserved	4	GND	Ground
	5	RSVD	Reserved	6	1.5V	+1.5V Power
	7	PCIE_B_CKREQ#	Request running clock	8	UIM_PWR	Sim card VDC power supply
	9	GND	Ground	10	UIM_DATA	Sim card serial data
	11	PCIE_B_REFCK+	Reference Clock Differential Pair	12	UIM_CLK	Sim card clock signal
	13	PCIE_B_REFCK-		14	UIM_RESET	Sim card reset signal
	15	GND	Ground	16	UIM_VPP	Programing voltage input

Mini-PCIE Card Slot							
0.80mm Pitch, 5.20mm Height, PCI Express* Mini Card, 52 Circuit, Right Angle, Surface Mount, 0.25µm Gold (Au) Plating							
Header	Pin	Signal Name	Function	Pin	Signal Name	Function	
	Top Side			Bottom Side			
	Mechanical Key						
		17	UIM_C8	Optionally used for USB interfaces and other uses.	18	GND	Ground
		19	UIM_C4	Optionally used for USB interfaces and other uses.	20	+3.3V	+3.3V Power
		21	GND	Ground	22	PCIE_B_PERST#	PCIe Fundamental Reset output
		23	PCIE_B_RX-	Receiver, Differential Pair	24	+3.3Vaux	+3.3V Power
		25	PCIE_B_RX+		26	GND	Ground
		27	GND	Ground	28	+1.5V	+1.5V Power
		29	GND	Ground	30	I2C_PM_CK_3V3	I2C Clock
		31	PCIE_B_TX-	Transmitter, Differential Pair	32	I2C_PM_DAT_3V3	I2C Data
		33	PCIE_B_TX+		34	GND	Ground
		35	GND	Ground	36	USB_PCIE_B_D-	Universal serial bus port 3 (-)
		37	RSVD	Reserved	38	USB_PCIE_B_D+	Universal serial bus port 3 (+)
		39	RSVD	Reserved	40	GND	Ground

Mini-PCIE Card Slot						
0.80mm Pitch, 5.20mm Height, PCI Express* Mini Card, 52 Circuit, Right Angle, Surface Mount, 0.25µm Gold (Au) Plating						
Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	<i>Top Side</i>			<i>Bottom Side</i>		
	41	RSVD	Reserved	42	LED_WWAN#	Wireless Card Status Indicator
	43	RSVD	Reserved	44	LED_WLAN#	
	45	RSVD	Reserved	46	LED_WPAN	
	47	RSVD	Reserved	48	+1.5V	+1.5V Power
	49	RSVD	Reserved	50	GND	Ground
	51	RSVD	Reserved	52	+3.3V	+3.3V Power

3.2.3.4. mini-PCIE Card Slot: mini-PCIE2

The signals of *mini-PCIE2* card slot are originated from *PCIE_C* of *SMRAC* card. The 4th set of *USB* signals are also connected to this connector. The following table shows the pin-out of the *mini-PCIE2* connector.



Mini-PCIE2: Location on Board, E6/F6

Mini-PCIE Card Slot						
0.80mm Pitch, 5.20mm Height, PCI Express* Mini Card, 52 Circuit, Right Angle, Surface Mount, 0.25µm Gold (Au) Plating						
Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	Top Side			Bottom Side		
	1	PCIE_C_WAKE#	Link Reactivation	2	+3.3V	+3.3V Power
	3	RSVD	Reserved	4	GND	Ground
	5	RSVD	Reserved	6	1.5V	+1.5V Power
	7	PCIE_C_CKREQ#	Request running clock	8	UIM_PWR	Sim card VDC power supply
	9	GND	Ground	10	UIM_DATA	Sim card serial data
	11	PCIE_C_REFCK+	Reference Clock Differential Pair	12	UIM_CLK	Sim card clock signal
	13	PCIE_C_REFCK-		14	UIM_RESET	Sim card reset signal
	15	GND	Ground	16	UIM_VPP	Programing voltage input

Mini-PCIE Card Slot							
0.80mm Pitch, 5.20mm Height, PCI Express* Mini Card, 52 Circuit, Right Angle, Surface Mount, 0.25µm Gold (Au) Plating							
Header	Pin	Signal Name	Function	Pin	Signal Name	Function	
	Top Side			Bottom Side			
	Mechanical Key						
		17	UIM_C8	Optionally used for USB interfaces and other uses.	18	GND	Ground
		19	UIM_C4	Optionally used for USB interfaces and other uses.	20	+3.3V	+3.3V Power
		21	GND	Ground	22	PCIE_C_PERST#	PCIe Fundamental Reset output
		23	PCIE_C_RX-	Receiver, Differential Pair	24	+3.3Vaux	+3.3V Power
		25	PCIE_C_RX+		26	GND	Ground
		27	GND	Ground	28	+1.5V	+1.5V Power
		29	GND	Ground	30	I2C_PM_CK_3V3	I2C Clock
		31	PCIE_C_TX-	Transmitter, Differential Pair	32	I2C_PM_DAT_3V3	I2C Data
		33	PCIE_C_TX+		34	GND	Ground
		35	GND	Ground	36	USB_PCIE_C_D-	Universal serial bus port 4 (-)
	37	RSVD	Reserved	38	USB_PCIE_C_D+	Universal serial bus port 4 (+)	
	39	RSVD	Reserved	40	GND	Ground	

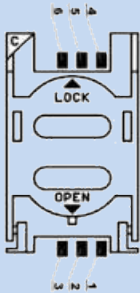
Mini-PCIE Card Slot						
0.80mm Pitch, 5.20mm Height, PCI Express* Mini Card, 52 Circuit, Right Angle, Surface Mount, 0.25µm Gold (Au) Plating						
Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	<i>Top Side</i>			<i>Bottom Side</i>		
	41	RSVD	Reserved	42	LED_WWAN#	Wireless Card Status Indicator
	43	RSVD	Reserved	44	LED_WLAN#	
	45	RSVD	Reserved	46	LED_WPAN	
	47	RSVD	Reserved	48	+1.5V	+1.5V Power
	49	RSVD	Reserved	50	GND	Ground
	51	RSVD	Reserved	52	+3.3V	+3.3V Power

3.2.3.5. SIM Card Holder: SIM_SLOT

A SIM card holder is present on EVK-STD-CARRIER for 3G/HSPA mini-PCIE module. The signals of the SIM card holder are connected to mini-PCIE1 connector.

The following table shows the pin-out of SIM_SLOT connector.

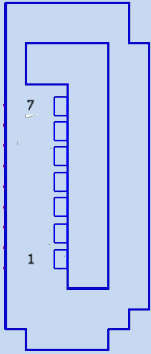
SIM_SLOT: Location on Board, E7/F7

SIM Card Holder					Edge Finger	Type	
WAFER 8P 2.54mm 180D(M) DIP A2543WV2-8P							
Header	Pin	Signal Name	Function	Pin#			
	1	UIM_PWR	Power Supply Input	-	P		
	2	UIM_RESET	Reset signal, used to reset the card's communications.	-	O		
	3	UIM_CLK	Provides the card with a clock signal, from which data communications timing is derived	-	O		
	4	UIM_C4	AUX1, optionally used for USB interfaces and other uses.	-	-		
	5	GND	Ground	-	P		
	6	UIM_VPP	Programing voltage input			P	
	7	UIM_DATA	Serial Data	-	IO		
	8	UIM_C8	AUX2, optionally used for USB interfaces and other uses.	-	-		

3.2.3.6. SATA Connector: SATA

The following table shows the pin-out of SATA connector.

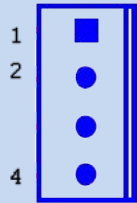
SATA: Location on Board, B3

SATA Connector					Edge Finger	Type
Serial ATA 7P 1.27mm 180D(M) DIP WATM-07DBN4A3B8						
Header	Pin	Signal Name	Function	Pin#		
	1	GND	Ground	-		P
	2	SATA_TX+	Transmit Output differential pair.	P48		
	3	SATA_TX-	Transmit Output differential pair.	P49		
	4	GND	Ground	-		P
	5	SATA_RX-	Receive Input differential pair	P52		I
	6	SATA_RX+	Receive Input differential pair	P51		I
	7	SATADOM	Sata Dom Pin 7 Power			

3.2.3.7. SATA Power Connector: SATA_PWR

The following table shows the pin-out of SATA Power connector.

SATA_PWR: Location on Board, A3

SATA Power Connector					Edge Finger	Type
WAFER 4P 2.5mm 180D(M) DIP 24W1161-04S10-01T						
Header	Pin	Signal Name	Function	Pin#		
	1	+5V	+5V Power	-		P
	2	GND	Ground	-		P
	3	GND	Ground	-		P
	4	GND	Ground	-		P
	5	+12V	+12V Power	+12V Power	-	

Note:

SATA Power cable is available from *Embedian* and come with *EVK-STD-CARRIER*. The part number from *Embedian* is *MKSA-041522-F35C-LF*.

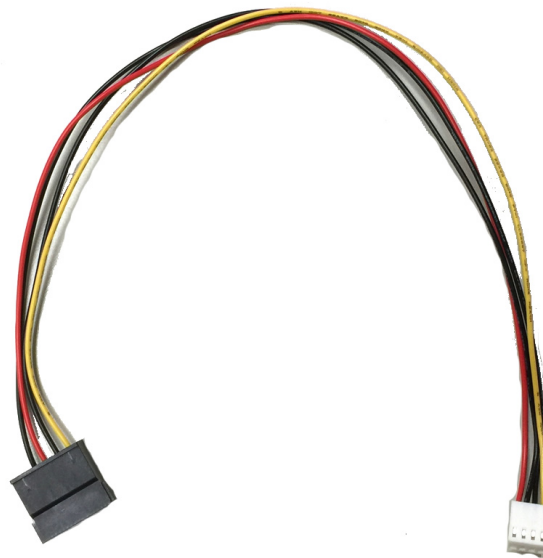


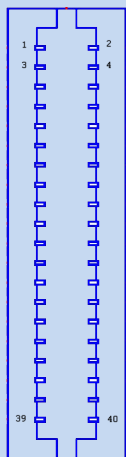
Figure 10: SATA Power Cable

3.2.3.8. 2-LANE and 4-LANE CAMERA Connector: CAMERA

The following table shows the pin-out of CAMERA connector.

CAMERA: Location on Board, C8/D8

2-LANE and 4-LANE CAMERA Connector						
B/B CONN. 2x20P 0.5mm 180D(M) SMD DF12(3.0)-30D						
Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	Odd Side			Even Side		
	1	GND	Ground	2	GND	Ground
	3	CSI1_CK+	CSI1 differential clock inputs	4	CSI0_CK+	CSI0 differential clock inputs
	5	CSI1_CK-	CSI1 differential clock inputs	6	CSI0_CK-	CSI0 differential clock inputs
	7	GND	Ground	8	GND	Ground
	9	CSI1_D0+	CSI1 differential data inputs 0	10	CSI0_D0+	CSI0 differential data inputs 0
	11	CSI1_D0-	CSI1 differential data inputs 0	12	CSI0_D0-	CSI0 differential data inputs 0
	13	GND	Ground	14	GND	Ground
	15	CSI1_D1+	CSI1 differential data inputs 1	16	CSI0_D1+	CSI0 differential data inputs 1
	17	CSI1_D1-	CSI1 differential data inputs 1	18	CSI0_D1-	CSI0 differential data inputs 1
	19	GND	Ground	20	GND	Ground



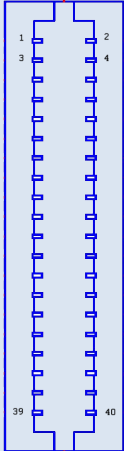
2-LANE and 4-LANE CAMERA Connector						
B/B CONN. 2x20P 0.5mm 180D(M) SMD DF12(3.0)-30D						
Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	Odd Side			Even Side		
	21	CSI1_D2+	CSI1 differential data inputs 2	22	I2C_CAM_CK	Camera I2C bus clock
	23	CSI1_D2-	CSI1 differential data inputs 2	24	I2C_CAM_DAT	Camera I2C bus data
	25	GND	Ground	26	CAM0_PWR#	Camera 0 Power Enable, active low output
	27	CSI1_D3+	CSI1 differential data inputs 3	28	CAM0_RST#	Camera 0 Reset, active low output
	29	CSI1_D3-	CSI1 differential data inputs 3	30	I2C_CAM_CK	Camera I2C bus clock
	31	GND	Ground	32	I2C_CAM_DAT	Camera I2C bus data
	33	CAM_MCK	Master clock output for CSI1 camera support	34	CAM1_PWR#	Camera 1 Power Enable, active low output
	35	GND	Ground	36	CAM1_RST#	Camera 1 Reset, active low output
	37	+3.3V	+3.3V Power	38	+1.8V	+1.8V Power
	39	+3.3V	+3.3V Power	40	+1.8V	+1.8V Power

3.2.3.9. LVDS Connector: LVDS

The following table shows the pin-out of LVDS connector.

LVDS: Location on Board, D3

LVDS Connector						
B/B Conn. 40P 1.25mm 90D SMD DF13-40DP-1.25V(91)						
Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	Odd Side (Channel 0)			Even Side (Channel 1)		
	1	VDD_LCD	LVDS panel VDD	2	VDD_LCD	LVDS panel VDD
	3	VDD_LCD	LVDS panel VDD	4	VDD_LCD	LVDS panel VDD
	5	GND	Ground	6	GND	Ground
	7	LVDS0_D0-	LVDS0 LCD data channel differential pairs 1	8	LVDS1_D0-	LVDS1 LCD data channel differential pairs 1
	9	LVDS0_D0+		10	LVDS1_D0+	
	11	GND	Ground	12	GND	Ground
	13	LVDS0_D1-	LVDS0 LCD data channel differential pairs 2	14	LVDS1_D1-	LVDS1 LCD data channel differential pairs 2
	15	LVDS0_D1+		16	LVDS1_D1+	
	17	GND	Ground	18	GND	Ground
	19	LVDS0_D2-	LVDS0 LCD data channel differential pairs 3	20	LVDS1_D2-	LVDS1 LCD data channel differential pairs 3
	21	LVDS0_D2+		22	LVDS1_D2+	

LVDS Connector						
B/B Conn. 40P 1.25mm 90D SMD DF13-40DP-1.25V(91)						
Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	Odd Side (Channel 0)			Even Side (Channel 1)		
	23	GND	Ground	24	GND	Ground
	25	LVDS0_CK-	LVDS0 LCD differential clock pairs	26	LVDS1_CK-	LVDS1 LCD differential clock pairs
	27	LVDS0_CK+		28	LVDS1_CK+	
	29	GND	Ground	30	GND	Ground
	31	LVDS0_D3-	LVDS0 LCD data channel differential pairs 4	32	LVDS1_D3-	LVDS1 LCD data channel differential pairs 4
	33	LVDS0_D3+		34	LVDS1_D3+	
	35	GND	Ground	36	GND	Ground
	37	I2C_LCD_CK	I2C_LCD bus clock	38	I2C_LCD_DAT	I2C_LCD bus data
	39	EDP_HPD	Future use for eDP HDP	40	NC	Not Connected

Note:

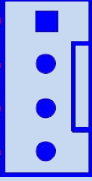
1. EVK-STD-CARRIER supports dual-channel LVDS (LVDS0 and LVDS1). LVDS0 signals are connected from LVDS0 of SMARC module. LVDS1 signals are connected from AFB_DIFF0-3 of SMARC module.
2. LVDS cables support the following panels.
 AUO G240HW01 V0 24 inch-wide 1920 (H) x 1080 (V) TFT color LCD
 or
 AUO G185XW01 V2 18.5 inch-wide WXGA 1366 (H) x 768 (V) TFT color LCD
 or
 AUO G070VW01 V0 7 inch WVGA 800 (H) x 480 (V) TFT color LCD

For detail part number, please see the following section.

3.2.3.10. LVDS Backlight Power Connector: LVDS_BKLT

The following table shows the pin-out of LVDS Backlight Power connector.

LVDS_BKLT: Location on Board, D2

LVDS Backlight Connector					Edge Finger	Type
WAFER BOX 2.0mm 4P 180D(M) DIP WO/Pb JIH VEI						
Header	Pin	Signal Name	Function	Pin#		
	1	VDD_BKLT	Backlight Power	-		P
	2	LCD_BKLT_EN	High enables panel backlight	S127		O
	3	LCD_BKLT_PWM	Display backlight PWM control	S141		O
	4	GND	Ground	-		P

Note:

The following table shows the part number of LVDS cables and LVDS backlight cables for supported panel. These cables are available from Embedian.

<i>Supported Panel</i>	<i>P/N (LVDS Cable + LVDS Backlight Cable)</i>
<i>AUO G240HW01 V0 (1080p dual channel)</i>	<i>DF13FIXL-B203028-A55CB-LF</i>
<i>AUO G185XW01 V2 (1366x768 single channel)</i>	<i>DF13FIXL-B203028-A45CA-LF</i>
<i>AUO G070VW01 V0 (800x480 single channel)</i>	<i>DF13DF19-B202028-F30CA-LF</i>

The default packing list comes with *DF13DF19-B202028-F30CA-LF* unless specified.

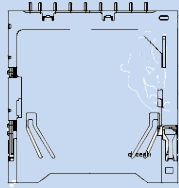


Figure 11: LVDS Cable and LVDS Backlight Cable

3.2.3.11. SD/SDHC Card Connector: SD

The following table shows the pin-out of SD connector.

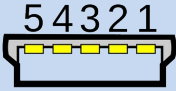
SD: Location on Board, B2/C2/B3/C3

SD/SDHC Card Connector					Edge Finger	Type
Right Angle, SMT, 2.75mm height, Push Push Normal Type With Detect Switch						
Header	Pin	Signal Name	Function	Pin#		
	1	SDIO_D3	SD receive/transmit data	P42		IO
	2	SDIO_CMD	SD receive response/transmit command	P34		IO
	3	VSS1	Ground	-		P
	4	VDD_SD0	Power	-		P
	5	SDIO_CK	SD Clock	P36		O
	6	VSS2	Ground	-		P
	7	SDIO_D0	SD receive/transmit data	P39		IO
	8	SDIO_D1	SD receive/transmit data	P40		IO
	9	SDIO_D2	SD receive/transmit data	P41		IO
	10	SDIO_CD#	SD Insert Detect	P35		I
	11	SDIO_WP	SD Write Protect	P33		I

3.2.3.12. USB OTG Connector: USBOTG

The following table shows the pin-out of USB OTG connector.

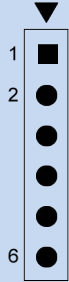
USBOTG: Location on Board, G2

SD/SDHC Card Connector				Edge Finger	Type
USB OTG mini Type B Connector					
Header	Pin	Signal Name	Function	Pin#	
	1	USB0_VBus	Power Supply	-	P
	2	USB0-	Data-	P61	IO
	3	USB0+	Data+	P60	IO
	4	USB0_OTG_ID	Host cable identification	P64	IO
	5	GND	Ground	-	P

3.2.3.13. SPI0 CS0 Pin Header: SPI0_0

The following table shows the pin-out of SPI0 CS0 pin header.

SPI0_0: Location on Board, G5

SPI0 CS0 Pin Header				Edge Finger	Type
PIN HEADER 1x6P 2.00mm 180D(M) SMD					
Header	Pin	Signal Name	Function	Pin#	
	1	+3.3V	+3.3V Power	-	P
	2	SPI00_SCLK	SPI0 Master Clock output	P44	O
	3	SPI00_MOSI	SPI0 Master Data output	P46	O
	4	SPI00_MISO	SPI0 Master Data input	P45	I
	5	SPI00_CS#	SPI0 Master Chip Select 0 output	P43	O
	6	GND	Ground	-	P

3.2.3.14. SPI0 CS1 Pin Header: SPI0_1

The following table shows the pin-out of SPI0 CS1 pin header.


SPI0_1: Location on Board, G5

SPI0 CS1 Pin Header					<i>Edge Finger</i>	<i>Type</i>
PIN HEADER 1x6P 2.00mm 180D(M) SMD						
<i>Header</i>	<i>Pin</i>	<i>Signal Name</i>	<i>Function</i>	<i>Pin#</i>		
	1	+3.3V	+3.3V Power	-		P
	2	SPI01_SCLK	SPI0 Master Clock output	P44		O
	3	SPI01_MOSI	SPI0 Master Data output	P46		O
	4	SPI01_MISO	SPI0 Master Data input	P45		I
	5	SPI01_CS#	SPI0 Master Chip Select 1 output	P31		O
	6	GND	Ground	-		P

3.2.3.15. SPI1 CS0 Pin Header: SPI1_0

The following table shows the pin-out of SPI1 CS0 pin header.


SPI1_0: Location on Board, G6

SPI1 CS0 Pin Header					Edge Finger	Type
PIN HEADER 1x6P 2.00mm 180D(M) SMD						
Header	Pin	Signal Name	Function	Pin#		
	1	+3.3V	+3.3V Power	-		P
	2	SPI10_SCLK	SPI1 Master Clock output	P56		O
	3	SPI10_MOSI	SPI1 Master Data output	P58		O
	4	SPI10_MISO	SPI1 Master Data input	P57		I
	5	SPI10_CS#	SPI1 Master Chip Select 0 output	P54		O
	6	GND	Ground	-		P

3.2.3.16. SPI1 CS1 Pin Header: SPI1_1

The following table shows the pin-out of SPI1 CS1 pin header.

SPI1_1: Location on Board, G6

SPI1 CS1 Pin Header					Edge Finger	Type
PIN HEADER 1x6P 2.00mm 180D(M) SMD						
Header	Pin	Signal Name	Function	Pin#		
	1	+3.3V	+3.3V Power	-		P
	2	SPI11_SCLK	SPI1 Master Clock output	P56		O
	3	SPI11_MOSI	SPI1 Master Data output	P58		O
	4	SPI11_MISO	SPI1 Master Data input	P57		I
	5	SPI11_CS#	SPI1 Master Chip Select 1 output	P55		O
	6	GND	Ground	-		P

3.2.3.17. I2S1 and I2S2 Pin Header: I2S

The I2S0 signals from SMARC module connect to a SGTL5000 audio codec. I2S1 and I2S2 signals from SMARC module leave as a 2x7 2.0mm pin header. The following table shows the pin-out of I2S1 and I2S2 pin header.


I2S: Location on Board, G6

<i>I2S1 and I2S2 Pin Header</i>						
<i>PIN HEADER 2x7P 2.00mm 180D(M) SMD</i>						
<i>Header</i>	<i>Pin</i>	<i>Signal Name</i>	<i>Function</i>	<i>Pin</i>	<i>Signal Name</i>	<i>Function</i>
	<i>I2S1</i>			<i>I2S2</i>		
	1	+3.3V	+3.3V Power	2	+3.3V	+3.3V Power
	3	I2S1_LRCK	Left& Right audio synchronization clock	4	I2S2_LRCK	Left& Right audio synchronization clock
	5	I2S1_CK	Digital audio clock	6	I2S2_CK	Digital audio clock
	7	I2S1_SDOUT	Digital audio Output	8	I2S2_SDOUT	Digital audio Output
	9	I2S1_SDIN	Digital audio Input	10	I2S2_SDIN	Digital audio Input
	11	GND	Ground	12	GND	Ground
	13	AUDIO_MCK	Master clock output to Audio codecs	14	GND	Ground

3.2.3.18. SPDIF Pin Header: SPDIF

The following table shows the pin-out of SPDIF pin header.

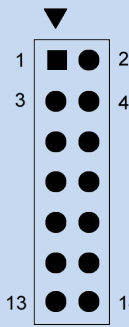
SPDIF: Location on Board, F7

<i>SPDIF Pin Header</i>					<i>Edge Finger</i>	<i>Type</i>
<i>PIN HEADER 1x4P 2.00mm 180D(M) SMD</i>						
<i>Header</i>	<i>Pin</i>	<i>Signal Name</i>	<i>Function</i>	<i>Pin#</i>		
	1	SPDIF_OUT_3V3	Digital Audio Output	S59		O
	2	NC	Not Connected	-		-
	3	GND	Ground	-		P
	4	SPDIF_IN_3V3	Digital Audio Input	S60		I

3.2.3.19. GPIO Pin Header: GPIO

The following table shows the pin-out of *GPIO* pin header.

GPIO: Location on Board, F2

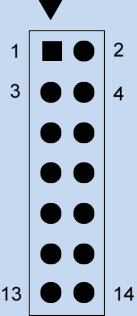
GPIO Pin Header					Edge Finger	Type
PIN HEADER 2x7P 2.00mm 180D(M) SMD						
Header	Pin	Signal Name	Function	Pin#		
	1	+3.3V	+3.3V Power	-		P
	2	GND	Ground	-		P
	3	GPIO0	Camera 0 Power Enable	P108		IO
	4	GPIO6	Tachometer input	P114		IO
	5	GPIO1	Camera 1 Power Enable	P109		IO
	6	GPIO7	PCAM_FLD signal input	P115		IO
	7	GPIO2	Camera 0 Reset	P110		IO
	8	GPIO8	CAN0 Error signal,	P116		IO
	9	GPIO3	Camera 1 Reset	P111		IO
	10	GPIO9	CAN1 Error signal, active Low input	P117		IO
	11	GPIO4	HD Audio Reset	P112		IO
	12	GPIO10		P118		IO
	13	GPIO5	PWM output	P113		IO
	14	GPIO11		P119		IO

3.2.3.20. MISC. Signals Pin Header: MISC

The following table shows the pin-out of misc. signals pin header.

MISC: Location on Board, G3

<i>MISC Signals Pin Header</i>					<i>Edge Finger</i>	<i>Type</i>
<i>PIN HEADER 2x7P 2.54mm 180D(M) SMD</i>						
<i>Header</i>	<i>Pin</i>	<i>Signal Name</i>	<i>Function</i>	<i>Pin#</i>		
	1	POWER_BTN#	Power-button input from Carrier board	P128		I
	2	GND	Ground	-		P
	3	SLEEP#	Sleep indicator from Carrier board	S149		I
	4	GND	Ground	-		P
	5	LID#	Lid open/close indication to Module	S148		I
	6	GND	Ground	-		P
	7	FORCE_RECOV#	Force Recovery	S155		I
	8	GND	Ground	-		P
	9	TEST#	Test Pin	S158		I
	10	GND	Ground	-		P
	11	WDI_Z	Watchdog input transition	-		I
	12	WDI	Wdatchdog input	-		I
	13	RESET_IN#	Reset input from Carrier board	P127		I
	14	GND	Ground	-		P



Note:

1. When pin 11 and pin 12 are shunt, *WDT_TIME_OUT#* will be high and reset will be triggered after 200ms.

3.2.3.21. AFB Signals Pin Header: AFB

The following table shows the pin-out of AFB signals pin header.

AFB: Location on Board, E2

AFB Signals Pin Header					Edge Finger	Type
PIN HEADER 2x7P 2.00mm 180D(M) SMD						
Header	Pin	Signal Name	Function	Pin#		
	1	+3.3V	+3.3V Power	-	P	
	2	GND	Ground	-	P	
	3	AFB0_OUT	Alternate Function Block	S17	O	
	4	AFB5_IN (*)	Alternate Function Block	S22	I	
	5	AFB1_OUT (*)	Alternate Function Block	S18	O	
	6	AFB6_PTIO	Alternate Function Block	S23	IO	
	7	AFB2_OUT (*)	Alternate Function Block	S19	O	
	8	AFB7_PTIO	Alternate Function Block	S24	IO	
	9	AFB3_IN	Alternate Function Block	S20	I	
	10	AFB8_PTIO	Alternate Function Block	S55	IO	
	11	AFB4_IN (*)	Alternate Function Block	S21	I	
	12	AFB9_PTIO	Alternate Function Block	S56	IO	
	13	NC	Not Connected	-	-	
	14	NC	Not Connected	-	-	

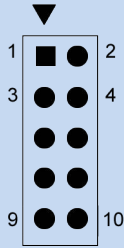
Note:

AFB1_OUT, AFB2_OUT, AFB4_IN and AFB5_IN signals share with 4-wire touch signals. The default hardware configuration is AFB.

3.2.3.22. CAN0 Bus Pin Header: CAN0

The following table shows the pin-out of CAN0 bus pin header.

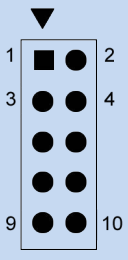
CAN0: Location on Board, D1

CAN0 Bus Pin Header					Edge Finger	Type
PIN HEADER 2x5P 2.00mm 180D(M) SMD						
Header	Pin	Signal Name	Function	Pin#		
	1	NC	Not Connected	-	-	
	2	NC	Not Connected	-	-	
	3	CAN0L	CAN Signal Low	P144	I	
	4	CAN0H	CAN Signal High	P143	O	
	5	NC	Not Connected	-	-	
	6	NC	Not Connected	-	-	
	7	NC	Not Connected	-	-	
	8	NC	Not Connected	-	-	
	9	GND	Ground	-	P	
	10	NC	Not Connected	-	-	

3.2.3.23. CAN1 Bus Pin Header: CAN1

The following table shows the pin-out of CAN1 bus pin header.

CAN1: Location on Board, D1/E1

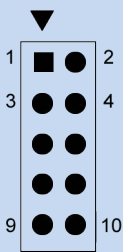
CAN1 Bus Pin Header					<i>Edge Finger</i>	<i>Type</i>
PIN HEADER 2x5P 2.00mm 180D(M) SMD						
<i>Header</i>	<i>Pin</i>	<i>Signal Name</i>	<i>Function</i>	<i>Pin#</i>		
	1	NC	Not Connected	-	-	
	2	NC	Not Connected	-	-	
	3	CAN1L	CAN Signal Low	P146	I	
	4	CAN1H	CAN Signal High	P145	O	
	5	NC	Not Connected	-	-	
	6	NC	Not Connected	-	-	
	7	NC	Not Connected	-	-	
	8	NC	Not Connected	-	-	
	9	GND	Ground	-	P	
	10	NC	Not Connected	-	-	

3.2.3.24. SER1 RS232 (2 wires) Pin Header: COM1

The following table shows the pin-out of COM1 pin header.

COM1: Location on Board, E1

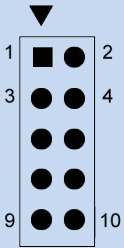
<i>COM1 Pin Header</i>					<i>Edge Finger</i>	<i>Type</i>
<i>PIN HEADER 2x5P 2.00mm 180D(M) SMD</i>						
<i>Header</i>	<i>Pin</i>	<i>Signal Name</i>	<i>Function</i>	<i>Pin#</i>		
	1	NC	Not Connected	-	-	
	2	NC	Not Connected	-	-	
	3	COM1_RXD	Receive Data	P135	I	
	4	NC	Not Connected	-	-	
	5	COM1_TXD	Transmit Data	P134	O	
	6	NC	Not Connected	-	-	
	7	NC	Not Connected	-	-	
	8	NC	Not Connected	-	-	
	9	GND	Ground	-	P	
	10	NC	Not Connected	-	-	



3.2.3.25. SER3 RS232 (2 wires) Pin Header: COM3

The following table shows the pin-out of COM3 pin header.

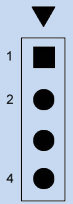
COM3: Location on Board, F1

<i>COM3 Pin Header</i>					<i>Edge Finger</i>	<i>Type</i>
<i>PIN HEADER 2x5P 2.00mm 180D(M) SMD</i>						
<i>Header</i>	<i>Pin</i>	<i>Signal Name</i>	<i>Function</i>	<i>Pin#</i>		
	1	NC	Not Connected	-	-	
	2	NC	Not Connected	-	-	
	3	COM3_RXD	Receive Data	P141	I	
	4	NC	Not Connected	-	-	
	5	COM3_TXD	Transmit Data	P140	O	
	6	NC	Not Connected	-	-	
	7	NC	Not Connected	-	-	
	8	NC	Not Connected	-	-	
	9	GND	Ground	-	P	
	10	NC	Not Connected	-	-	

3.2.3.26. I2C_GP Pin Header: I2C0

The following table shows the pin-out of I2C_GP pin header.

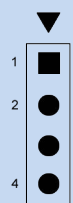
I2C0: Location on Board, B6

<i>I2C_GP Pin Header</i>					<i>Edge Finger</i>	<i>Type</i>
<i>PIN HEADER 1x4P 2.00mm 180D(M) SMD</i>						
<i>Header</i>	<i>Pin</i>	<i>Signal Name</i>	<i>Function</i>	<i>Pin#</i>		
	1	+3.3V	+3.3V Power	-		P
	2	I2C_GP_CK_3V3	General purpose I2C bus clock	S48		O OD
	3	I2C_GP_DAT_3V3	General purpose I2C bus data	S49		IO OD
	4	GND	Ground	-		P

3.2.3.27. I2C_CAM Pin Header: I2C1

The following table shows the pin-out of I2C_CAM pin header.


I2C1: Location on Board, B7

<i>I2C_CAM Pin Header</i>					<i>Edge Finger</i>	<i>Type</i>
<i>PIN HEADER 1x4P 2.00mm 180D(M) SMD</i>						
<i>Header</i>	<i>Pin</i>	<i>Signal Name</i>	<i>Function</i>	<i>Pin#</i>		
	1	+3.3V	+3.3V Power	-		P
	2	I2C_CAM_CK_3V3	Serial Camera Support Link - I2C bus clock	S5		O OD
	3	I2C_CAM_DAT_3V3	Serial Camera Support Link - I2C bus data	S7		IO OD
	4	GND	Ground	-		P

3.2.3.28. Buzzer: Buzzer

The buzzer on *EVK-STD_CARRIER* is controlled by *PWM (GPIO5)*. The rated frequency is 2731 + 200Hz.

Buzzer: Location on Board, A2


Buzzer Connector					Edge Finger	Type
ELECTRO MAGNETIC BUZZER						
Header	Pin	Signal Name	Function	Pin#		
	1	+5V	+5V Power	-		P
	2	GPIO5	PWM Out	P113		O

3.2.3.29. 4-wire Resistive Touch Connector: Touchscreen

EVK-STD-CARRIER provides with a 4-wire FPC connector for legacy touch panel. The controller is from ADC of the processor and from AFB of SMARC connector.

The following table shows the pin-out of the Touchscreen 4-wire resistive connector.

Touchscreen: Location on Board, C7/C8

I2C_CAM Pin Header				Edge Finger	Type
PIN HEADER 1x4P 2.00mm 180D(M) SMD					
Header	Pin	Signal Name	Function	Pin#	
	1	XNUR	Left	S21	AI
	2	YPLL	Bottom	S19	AI
	3	XPUL	Right	S18	AI
	4	YNLR	Top	S22	AI

Note:

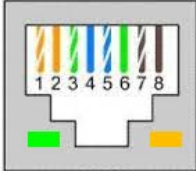
2. The length of touch FPC cable should not be keeping too long.
3. The connector is not populated at factory default unless user specified.

3.2.3.30. LAN2 (2nd LAN) RJ45 Connector: LAN2

EVK-STD-CARRIER provides with the 2nd RJ45 GigaLAN connector from AFB of SMARC connector.

The following table shows the pin-out of the LAN2 RJ45 connector.

LAN2: Location on Board, C7/C8

LAN2 RJ45 Connector					Edge Finger	Type	
RJ45 1x1 Tab down Through Hole Gold Flash 10/100/1000 Base=T LED:L-Y;R-O/G							
Header	Pin	Signal Name	Function	Pin#			
	1	GBE1_MDI0+	Transmit Data+	S62		AO	
	2	GBE1_MDI0-	Transmit Data-	S63		AO	
	3	GBE1_MDI1+	Receive Data+	S65		AI	
	4	GBE1_MDI2+	Transmit Data+	S66		AO	
	5	GBE1_MDI2-	Transmit Data-	S68		AO	
	6	GBE1_MDI1-	Receive Data-	S69		AI	
	7	GBE1_MDI3+	Receive Data+	S71		AO	
	8	GBE1_MDI3-	Receive Data-	S72		AO	
	L	Left LED	Duplex	S23/S24			Yellow
	R	Right LED	Link and Ack	S55			Green

Note:

1. The connector is not populated at factory default unless user specified.
2. The GBE1 shares the same signals as LVDS1. The hardware configuration is set as LVDS1 at factory default.

3.2.3.31. MXM3.0 Connector: SMARC

The following table shows the pin-out of MXM 3.0 pin header.

SMARC: Location on Board, D3/D4/D5/D6/D7

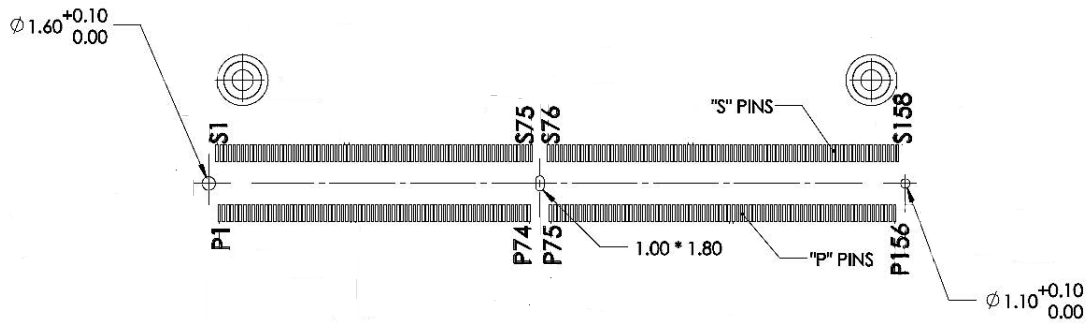


Figure 12: MXM3.0 Connector Pin Layout

MXM 3.0 Connector			
MXM 3.0 SOCKET,314POTS,7.8MM HEIGHT			
<i>Pin</i>	<i>Signal Name</i>	<i>Pin</i>	<i>Signal Name</i>
P1	PCAM_PXL_CK1	S1	PCAM_VSYNC
P2	GND	S2	PCAM_HSYNC
P3	CSI1_CK+ / PCAM_D0	S3	GND
P4	CSI1_CK- / PCAM_D1	S4	PCAM_PXL_CK0
P5	PCAM_DE	S5	I2C_CAM_CK
P6	PCAM_MCK	S6	CAM_MCK
P7	CSI1_D0+ / PCAM_D2	S7	I2C_CAM_DAT
P8	CSI1_D0- / PCAM_D3	S8	CSI0_CK+ / PCAM_D10
P9	GND	S9	CSI0_CK- / PCAM_D11
P10	CSI1_D1+ / PCAM_D4	S10	GND
P11	CSI1_D1- / PCAM_D5	S11	CSI0_D0+ / PCAM_D12
P12	GND	S12	CSI0_D0- / PCAM_D13
P13	CSI1_D2+ / PCAM_D6	S13	GND
P14	CSI1_D2- / PCAM_D7	S14	CSI0_D1+ / PCAM_D14
P15	GND	S15	CSI0_D1- / PCAM_D15
P16	CSI1_D3+ / PCAM_D8	S16	GND
P17	CSI1_D3- / PCAM_D9	S17	AFB0_OUT
P18	GND	S18	AFB1_OUT
P19	GbE_MDI3-	S19	AFB2_OUT
P20	GbE_MDI3+	S20	AFB3_IN
P21	GbE_LINK100#	S21	AFB4_IN
P22	GbE_LINK1000#	S22	AFB5_IN
P23	GbE_MDI2-	S23	AFB6_PTIO

MXM 3.0 Connector			
MXM 3.0 SOCKET,314POTS,7.8MM HEIGHT			
<i>Pin</i>	<i>Signal Name</i>	<i>Pin</i>	<i>Signal Name</i>
P24	GbE_MDI2+	S24	AFB7_PTIO
P25	GbE_LINK_ACT#	S25	GND
P26	GbE_MDI1-	S26	SDMMC_D0
P27	GbE_MDI1+	S27	SDMMC_D1
P28	GbE_CTREF	S28	SDMMC_D2
P29	GbE_MDI0-	S29	SDMMC_D3
P30	GbE_MDI0+	S30	SDMMC_D4
P31	SPI0_CS1#	S31	SDMMC_D5
P32	GND	S32	SDMMC_D6
P33	SDIO_WP	S33	SDMMC_D7
P34	SDIO_CMD	S34	GND
P35	SDIO_CD#	S35	SDMMC_CK
P36	SDIO_CK	S36	SDMMC_CMD
P37	SDIO_PWR_EN	S37	SDMMC_RST#
P38	GND	S38	AUDIO_MCK
P39	SDIO_D0	S39	I2S0_LRCK
P40	SDIO_D1	S40	I2S0_SDOUT
P41	SDIO_D2	S41	I2S0_SDIN
P42	SDIO_D3	S42	I2S0_CK
P43	SPI0_CS0#	S43	I2S1_LRCK
P44	SPI0_CK	S44	I2S1_SDOUT
P45	SPI0_DIN	S45	I2S1_SDIN
P46	SPI0_DO	S46	I2S1_CK

MXM 3.0 Connector			
MXM 3.0 SOCKET,314POTS,7.8MM HEIGHT			
<i>Pin</i>	<i>Signal Name</i>	<i>Pin</i>	<i>Signal Name</i>
P47	GND	S47	GND
P48	SATA_TX+	S48	I2C_GP_CK
P49	SATA_TX-	S49	I2C_GP_DAT
P50	GND	S50	I2S2_LRCK
P51	SATA_RX+	S51	I2S2_SDOUT
P52	SATA_RX-	S52	I2S2_SDIN
P53	GND	S53	I2S2_CK
P54	SPI1_CS0#	S54	SATA_ACT#
P55	SPI1_CS1#	S55	AFB8_PTIO
P56	SPI1_CK	S56	AFB9_PTIO
P57	SPI1_DIN	S57	PCAM_ON_CSI0#
P58	SPI1_DO	S58	PCAM_ON_CSI1#
P59	GND	S59	SPDIF_OUT
P60	USB0+	S60	SPDIF_IN
P61	USB0-	S61	GND
P62	USB0_EN_OC#	S62	AFB_DIFF0+
P63	USB0_VBUS_DET	S63	AFB_DIFF0-
P64	USB0_OTG_ID	SS64	GND
P65	USB1+	S65	AFB_DIFF1+
P66	USB1-	S66	AFB_DIFF1-
P67	USB1_EN_OC#	S67	GND
P68	GND	S68	AFB_DIFF2+
P69	USB2+	S69	AFB_DIFF2-

MXM 3.0 Connector			
MXM 3.0 SOCKET,314POTS,7.8MM HEIGHT			
<i>Pin</i>	<i>Signal Name</i>	<i>Pin</i>	<i>Signal Name</i>
P70	USB2-	S70	GND
P71	USB2_EN_OC#	S71	AFB_DIFF3+
P72	PCIE_C_PRSENT#	S72	AFB_DIFF3-
P73	PCIE_B_PRSENT#	S73	GND
P74	PCIE_A_PRSENT#	S74	AFB_DIFF4+
P75	PCIE_A_RST#	S75	AFB_DIFF4-
P76	PCIE_C_CKREQ#	S76	PCIE_B_RST#
P77	PCIE_B_CKREQ#	S77	PCIE_C_RST#
P78	PCIE_A_CKREQ#	S78	PCIE_C_RX+
P79	GND	S79	PCIE_C_RX-
P80	PCIE_C_REFCK+	S80	GND
P81	PCIE_C_REFCK-	S81	PCIE_C_TX+
P82	GND	S82	PCIE_C_TX-
P83	PCIE_A_REFCK+	S83	GND
P84	PCIE_A_REFCK-	S84	PCIE_B_REFCK+
P85	GND	S85	PCIE_B_REFCK-
P86	PCIE_A_RX+	S86	GND
P87	PCIE_A_RX-	S87	PCIE_B_RX+
P88	GND	S88	PCIE_B_RX-
P89	PCIE_A_TX+	S89	GND
P90	PCIE_A_TX-	S90	PCIE_B_TX+
P91	GND	S91	PCIE_B_TX-
P92	HDMI_D2+	S92	GND

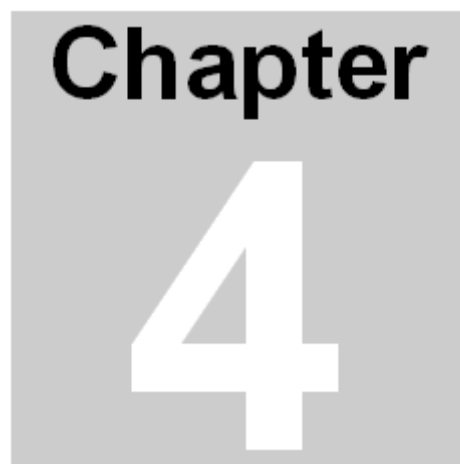
MXM 3.0 Connector			
MXM 3.0 SOCKET,314POTS,7.8MM HEIGHT			
<i>Pin</i>	<i>Signal Name</i>	<i>Pin</i>	<i>Signal Name</i>
P93	HDMI_D2-	S93	LCD_D0
P94	GND	S94	LCD_D1
P95	HDMI_D1+	S95	LCD_D2
P96	HDMI_D1-	S96	LCD_D3
P97	GND	S97	LCD_D4
P98	HDMI_D0+	S98	LCD_D5
P99	HDMI_D0-	S99	LCD_D6
P100	GND	S100	LCD_D7
P101	HDMI_CK+	S101	GND
P102	HDMI_CK-	S102	LCD_D8
P103	GND	S103	LCD_D9
P104	HDMI_HPD	S104	LCD_D10
P105	HDMI_CTRL_CK	S105	LCD_D11
P106	HDMI_CTRL_DAT	S106	LCD_D12
P107	HDMI_CEC	S107	LCD_D13
P108	GPI00 / CAM0_PWR#	S108	LCD_D14
P109	GPI01 / CAM1_PWR#	S109	LCD_D15
P110	GPI02 / CAM0_RST#	S110	GND
P111	GPI03 / CAM1_RST#	S111	LCD_D16
P112	GPI04 / HDA_RST#	S112	LCD_D17
P113	GPI05 / PWM_OUT	S113	LCD_D18
P114	GPI06 / TACHIN	S114	LCD_D19
P115	GPI07 / PCAM_FLD	S115	LCD_D20

MXM 3.0 Connector			
MXM 3.0 SOCKET,314POTS,7.8MM HEIGHT			
<i>Pin</i>	<i>Signal Name</i>	<i>Pin</i>	<i>Signal Name</i>
P116	GPI08 / CAN0_ERR#	S116	LCD_D21
P117	GPI09 / CAN1_ERR#	S117	LCD_D22
P118	GPI010	S118	LCD_D23
P119	GPI011	S119	GND
P120	GND	S120	LCD_DE
P121	I2C_PM_CK	S121	LCD_VS
P122	I2C_PM_DAT	S122	LCD_HS
P123	BOOT_SEL0#	S123	LCD_PCK
P124	BOOT_SEL1#	S124	GND
P125	BOOT_SEL2#	S125	LVDS0+
P126	RESET_OUT#	S126	LVDS0-
P127	RESET_IN#	S127	LCD_BKLT_EN
P128	POWER_BTN#	S128	LVDS1+
P129	SER0_TX	S129	LVDS1-
P130	SER0_RX	S130	GND
P131	SER0_RTS#	S131	LVDS2+
P132	SER0_CTS#	S132	LVDS2-
P133	GND	S133	LCD_VDD_EN
P134	SER1_TX	S134	LVDS_CK+
P135	SER1_RX	S135	LVDS_CK-
P136	SER2_TX	S136	GND
P137	SER2_RX	S137	LVDS3+
P138	SER2_RTS#	S138	LVDS3-

MXM 3.0 Connector

MXM 3.0 SOCKET,314POTS,7.8MM HEIGHT

<i>Pin</i>	<i>Signal Name</i>	<i>Pin</i>	<i>Signal Name</i>
P139	SER2_CTS#	S139	I2C_LCD_CK
P140	SER3_TX	S140	I2C_LCD_DAT
P141	SER3_RX	S141	LCD_BKLT_PWM
P142	GND	S142	LCD_DUAL_PCK
P143	CAN0_TX	S143	GND
P144	CAN0_RX	S144	RSVD / EDP_HPD
P145	CAN1_TX	S145	WDT_TIME_OUT#
P146	CAN1_RX	S146	PCIE_WAKE#
P147	VDD_IN	S147	VDD_RTC
P148	VDD_IN	S148	LID#
P149	VDD_IN	S149	SLEEP#
P150	VDD_IN	S150	VIN_PWR_BAD#
P151	VDD_IN	S151	CHARGING#
P152	VDD_IN	S152	CHARGER_PRSNT#
P153	VDD_IN	S153	CARRIER_STBY#
P154	VDD_IN	S154	CARRIER_PWR_ON
P155	VDD_IN	S155	FORCE_RECOV#
P156	VDD_IN	S156	BATLOW#
		S157	TEST#
		S158	VDD_IO_SEL#

A gray square graphic containing the word "Chapter" in a bold, black, sans-serif font at the top, and a large, white, sans-serif number "4" centered below it.

Quick Hardware Installation Guide

The purpose of this chapter is to provide a quick hardware installation guide so that developers can easily get the board up and running in few minutes.

Chapter 4 Quick Hardware Installation Guide

The quick hardware installation guides are intended to provide developers with simple instructions on how to install *EVK-STD-CARRIER* evaluation kit from very beginning and have it monitoring your local device in few minutes. No advanced installation options are discussed here - just the basics that will work for 95% of users who want to get started. This guide will lead you through the process of configuring, installing, and developing SMARC module. This guide was written to be as clear as possible and to provide only the details necessary to get you up and running. For more in-depth information, links to other chapters will be located where appropriate.

Step1. Insert SMARC CPU module

Install SMARC CPU module to *EVK-STD-CARRIER* SMARC connector at 30 degree angle.

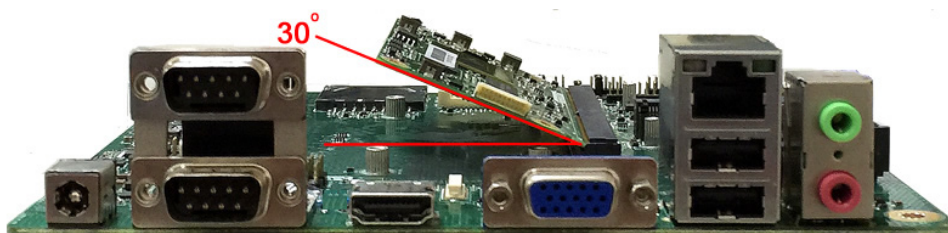


Figure 13: Insert SMARC Module

Step2. Fasten SMARC Module

Press down SMARC CPU module and fasten it by M2.5x 5mm screws.

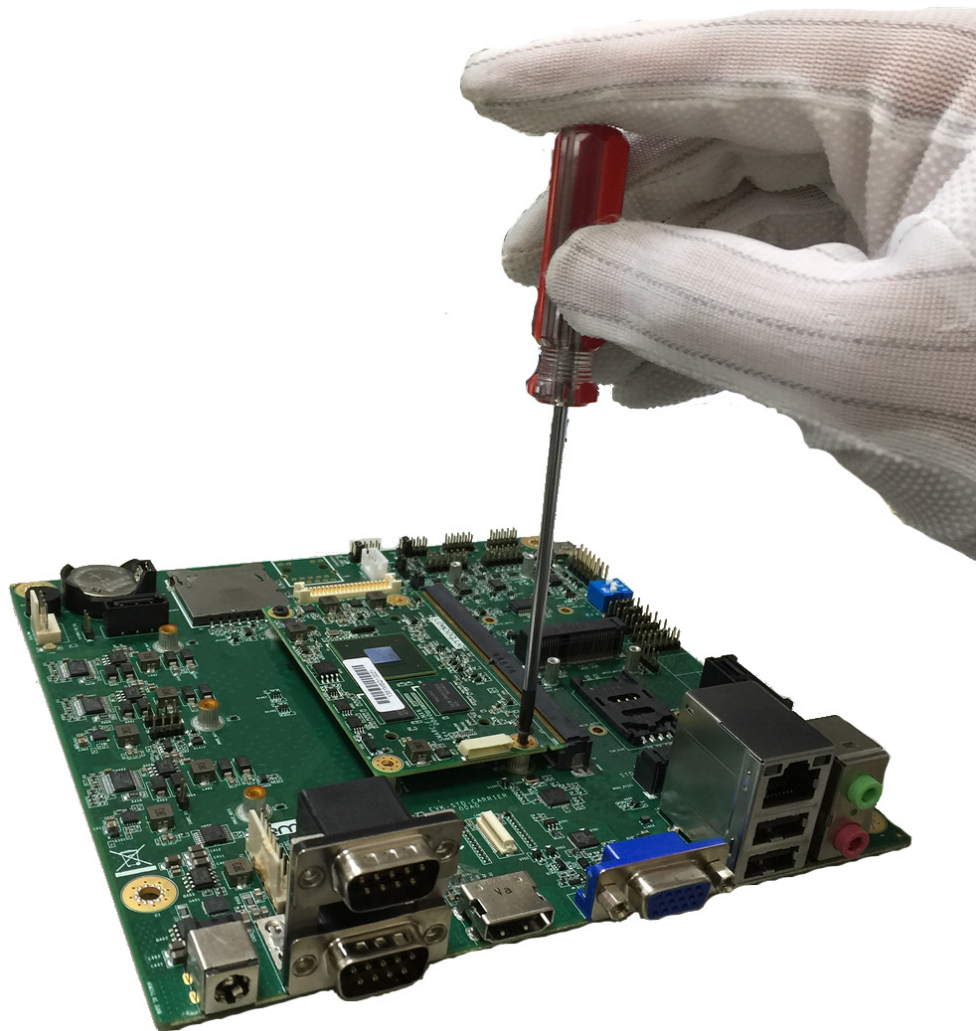


Figure 14: Fasten SMARC Module

Step3. Check Jumper Settings

Before power on, it is very important to check if the jumper is set properly. Below picture shows those need to be cared at power up.

1. **SMARC_SEL:**

Open: if your SMARC module uses 3.3V VDDIO.
Shunt: if your SMARC module uses 1.8V VDDIO.

2. **SER0_RX_SEL:**

Shunt 1-2: If your debug port is set to *SER0*.

If you need to connect to an LCD, you will also need to check the *LCD_VDD_SEL* and *LCD_BKLT_SEL*.

3. **LCD_BKLT_SEL:**

Shunt 1-2: 5V
Shunt 2-3: 12V

4. **LCD_VDD_SEL:**

Shunt 1-2: 3.3V
Shunt 2-3: 5V

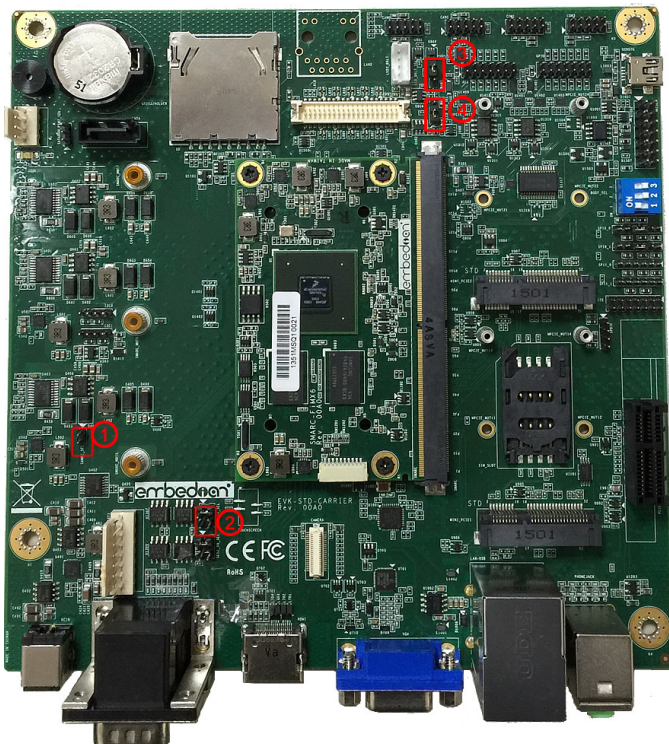


Figure 15: Check Jumper Settings

Step4. Check Switch Settings and Insert Bootable SD card

If *TEST#* pin is shunt crossed, the *SMARC* module will always boot up from SD card. If *TEST#* pin is open, the *SMARC* module will always boot up from on-module SPI NOR flash. Once the bootloader (u-boot) is up, it will read the *BOOT_SEL* setting and decides where to load kernel.

Usually, it first boot up is from SD card. Please insert the bootable SD card and set the *BOOT_SEL* switch to *ON OFF OFF* as shown in the following picture.

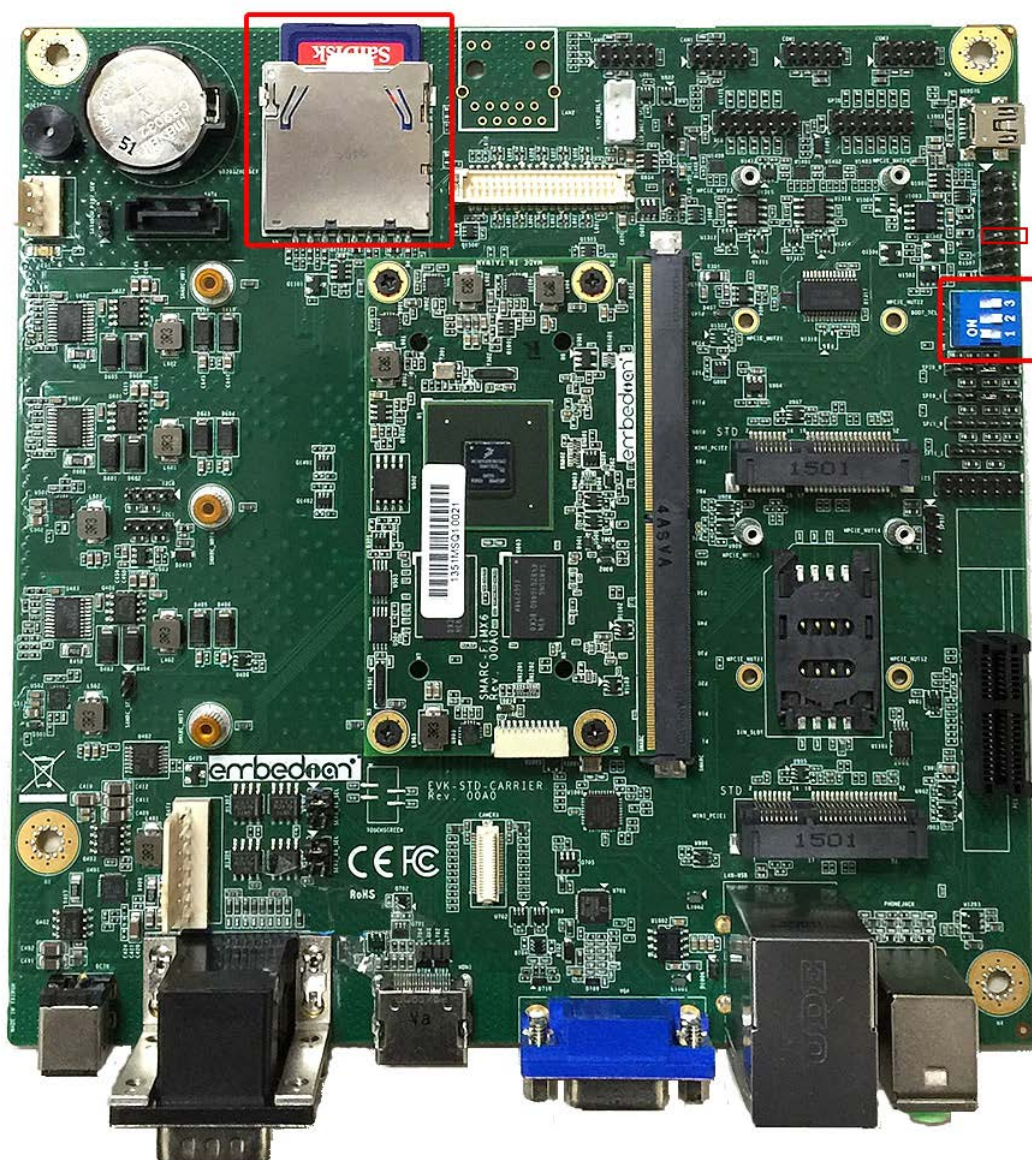


Figure 16: Check Switch Settings and Insert Bootable SD Card

Step5. Connect Debug Cable, Ethernet Cable and LCD Cable (if necessary) and Apply Power

Step 1~3 assumes that your debug port is set to *SER3*. If you use *SER0* as your debug port, neglect step 1 below.

1. Connect *COM3* header of *EVK-STD-CARRIER* to the 2x5 box header to DB9 cable.
2. Connect the 2x5 box header to a null modem cable (tx/rx crossed).
3. Connect the null modem cable to the *RS232* port of your host PC. Set the baud rate of the serial port as *115200, 8n1*.
4. Connect Ethernet cable to the RJ45 connector of *EVK-STD-CARRIER*.

If *LCD* is required in your application, follow step 5 and step 6 below.

5. Connect *LVDS* cable to *LVDS* connector.
6. Connect *LCD* backlight cable to *LVDS_BKLT* connector.

Bring up the board.

7. Apply 12V~ 24V (~36W power adaptor) DC power to *EVK-STD-CARRIER*, you should be able to see debug message from your putty or serial terminal of your host PC. No root password needed for Yocto rootfs. The default root password for Ubuntu 14.04 is *root*, and default *ubuntu* user is *temppwd*.

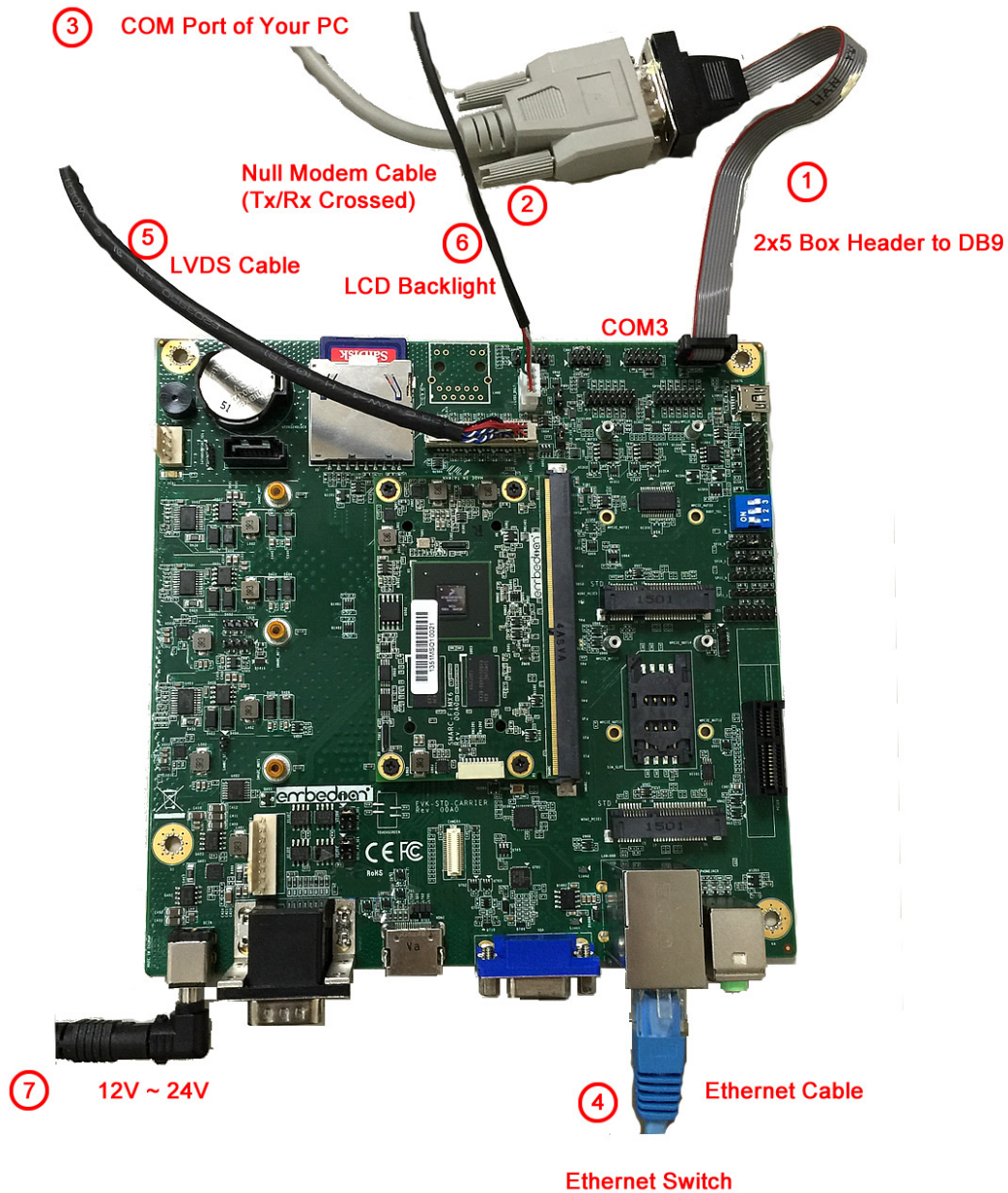


Figure 17: Wiring Diagram