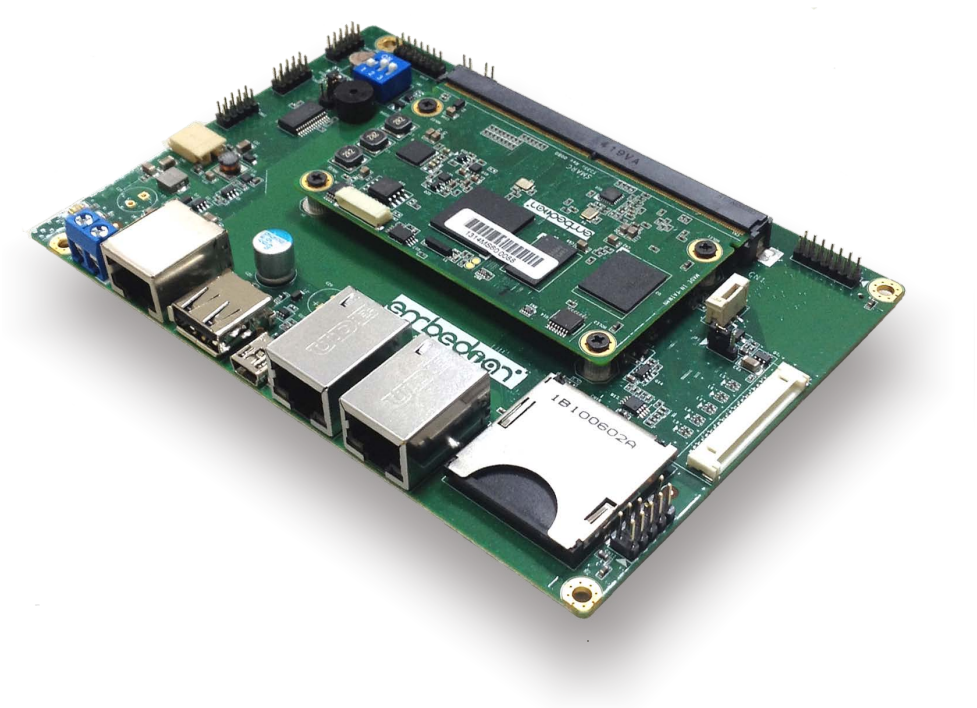
User's Manual

SMART Serier Single Board Computer



SBC-SMART-BEE

Revision History

Revision	Date	Changes from Previous Revision
1.0	2013/6/21	Initial Release
1.1	2014/4/17	Update to SMARC T335X Hardware Revision 00B0 1. SPI_D0 and SPI_D1 interchanged 2. LCD_BKLT_PWM and GPIO1 interchanged 3. Change Baseboard name from SMARTBASE-T3 to SBC-SMART-BEE
1.2	2014/05/09	1. Correct RS422 TX Polarity of CN12 2. Add Mounting Hole Mechanical Drawing Information
2.0	2014//11/05	1. Carrier Board H/W Revision 00A0 to 00B0 2. Add Buzzer 3. Change 18-bit Parallel RGB Interface to 18-bit LVDS Interface
2.1	2014/12/19	Correct the boot selection mode for SD bootup and eMMC bootup on page 26
2.2	2017/02/13	Correct document error in CN14

USER INFORMATION

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Table of Contents

Using this Manual

This guide provides information about the Embedian SBC-SMART-BEE Single Board Computer based on TI Sitara AM335x ARM-Cortex-A8 processor.

Conventions used in this guide

This table describes the typographic conventions used in this guide:

This Convention	Is used for
Italic type	Emphasis, new terms, variables, and document titles.
`monospaced type`	Filenames, pathnames, and code examples.

Embedian Information

Document Updates

Please always check the product specific section on the Embedian support website at www.embedian.com/ for the most current revision of this document.

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Additional Resources

Please also refer to the most recent SMARC T335x User's Manual and TI AM335x processor reference manual and related documentation for additional information.

Introduction

This Chapter gives background information on the SBC-SMART-BEE Single Board Computer
Section include：

- SBC-SMART-BEE single board computer Goals
- Feature Set Overview
- Block Diagram
- Peripheral Overview
- Layout Diagram
- Document and Standard References

Chapter 1 Introduction

This document serves as a user manual and technical reference for the EMBEDIAN SBC-SMART-BEE single board computer. The manual is intended for use by engineering personnel working with SBC-SMART-BEE systems. It will be very helpful if developers can refer together with the carrier board schematics.

1.1 SBC-SMART-BEE Single Board Computer Goals

EMBEDIAN SBC-SMART-BEE single board computer is equipped with all mechanical and electrical components necessary for the rapid start-up of the SMARC T335X computer on module. The SBC-SMART-BEE is designed as an “application ready” 3.5-inch single board computer.

The SBC-SMART-BEE single board computer is intended to serve multiple needs and summarized as followed:

- SMARC T335X Module bring-up platform for hardware and software development.
- Module validation platform.
- Customer evaluation platform.
- Customer design reference.
- Manufacturing test platform.
- Flexible prototyping vehicle (facilitated by multiple mezzanines).
- An “application ready” single board computer. (together with SMARC T335X module)

1.2 Feature Set Overview

The SBC-SMART-BEE has the following features:

- SMARC-T335X computer on module as the core.
- Length x Width: 102mm x 145mm (4.0" x 5.7"), 3.5-inch form factor
- Accepts 82mm x 50mm SMARC Modules.
- Accepts 3.3V SMARC VDD_IO only.
- Buzzer

- 24-bit color packing, single channel LVDS port.
- 18-bit color packing, single channel LVDS port
- 3.3V or 5V LCD signaling option
- Reset Jumper
- 5V LED Backlight support
- USB OTG mini AB connector – direct from SMARC.
- USB R/A Type A connector – direct from SMARC. SMARC compliant in an 82mm x 50mm form factor.
- 2 x Fast Ethernet (10/100Mbps) ports with integrated magnetics.
- On-board I2S Audio Codec.
- RS232 support for 3 SMARC serial ports (one can be configured as RS422/RS485).
- CAN Bus support (1).
- SPI (2) and I2C (2) Header
- Boot Option Switch
- SD Card slot.
- GPIO Header
- 4-wire Touch Connector
- RTC backup power sources – Lithium coin cell onboard.
- 5V input voltage terminal block with +/-28V over voltage and mis-wiring protection
- External WDT option
- A single 4KB EEPROM is provided on I2C0 that holds the board information. This information includes board name, part number, serial number, and revision information.

1.3 Block Diagram

An overall system block diagram for the SBC-SMART-BEE single board computer is shown on the following page. The following color coding is used on the block diagram:

- Industry standard wired I/O connectors are shown in orange.
- Embedian defined wired I/O connectors and headers are shown in red.
- Industry standard mezzanine and slot format connectors are shown in blue.
- ICs on the board are shown in pale yellow.
- Miscellaneous features (jumpers, switches) are shown in drab green.

Much may be gleaned from this diagram:

- How SMARC resources are used on the Evaluation Carrier.
- What the major Evaluation Carrier Features are.
- An indication of the power supply architecture.

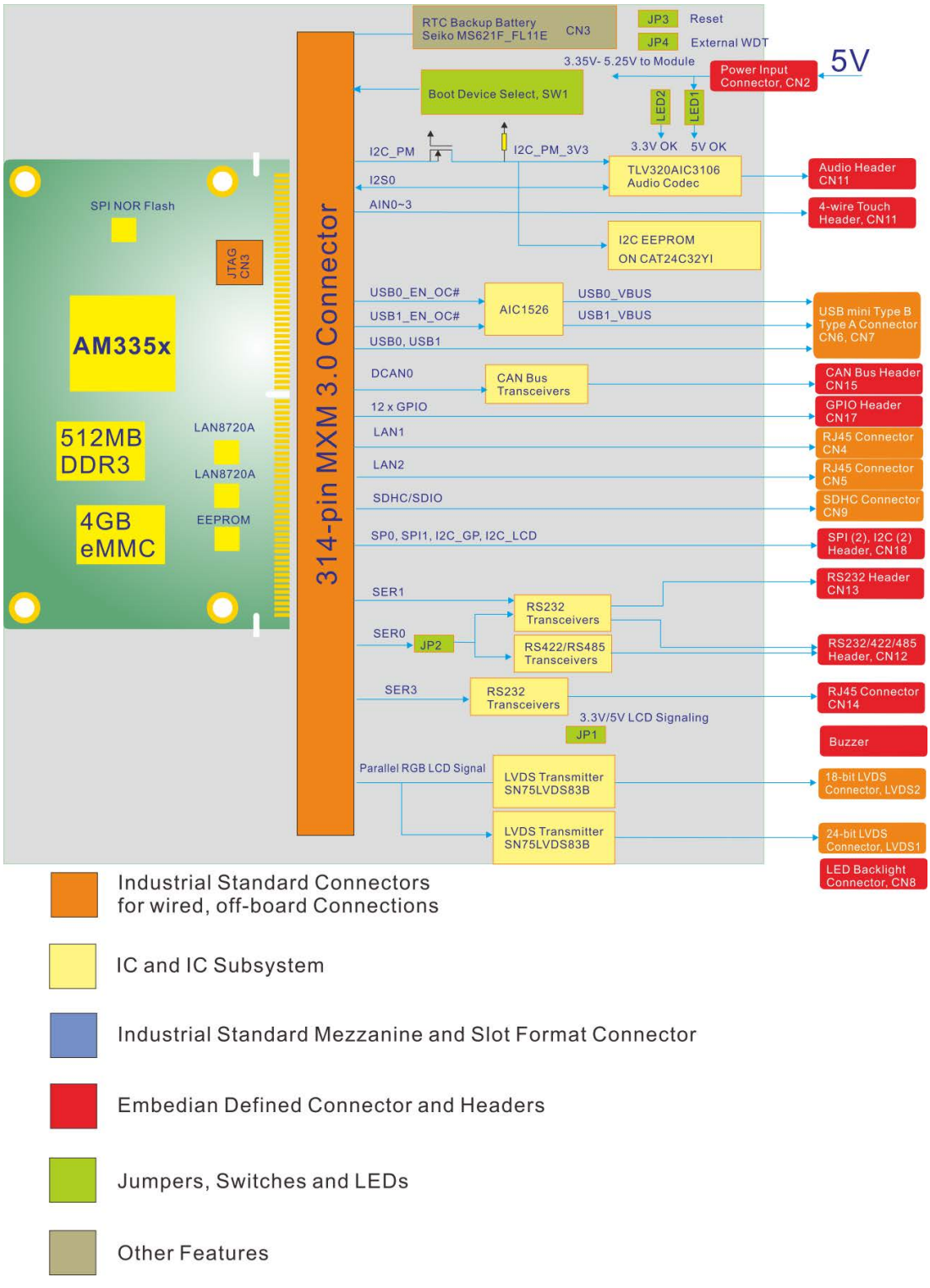


Figure 1: SBC-SMART-BEE Single Board Computer Block Diagram

Details for this diagram will be explained in the following chapters.

1.4 Peripheral Overview

The following diagram shows the function of all peripherals including of connectors, headers, configuration jumpers and other important features on the SBC-SMART-BEE single board computer.

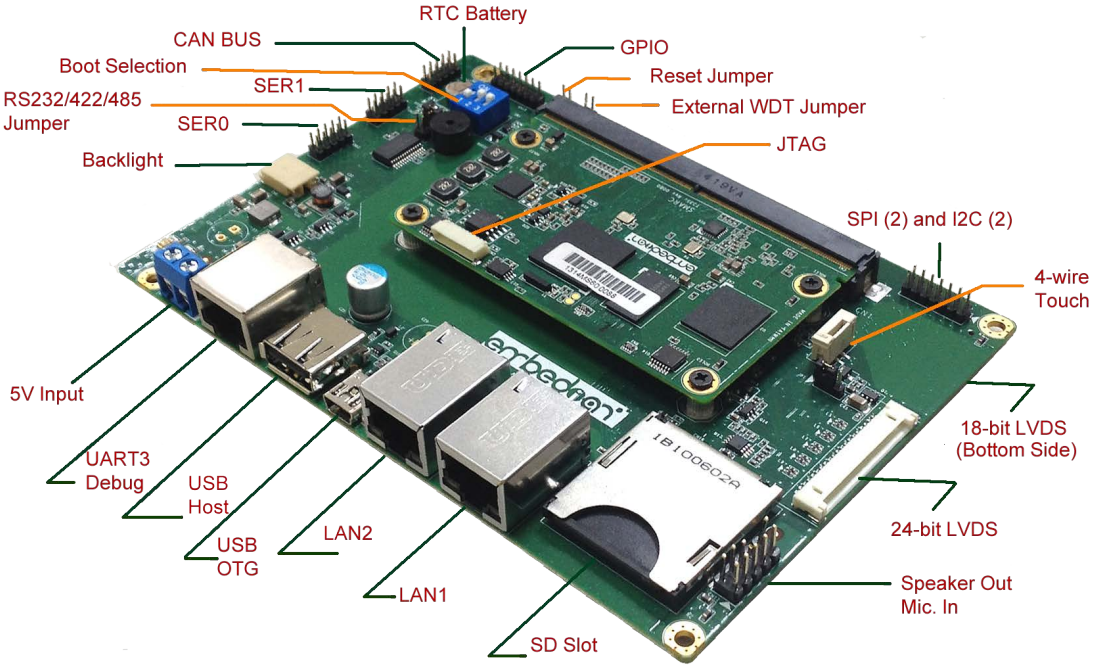


Figure 2: SBC-SMART-BEE Peripheral Diagram

1.5 Layout Diagram

The following section shows the physical location and reference designator of connectors, configuration jumpers and other important features on the SBC-SMART-BEE single board computer.

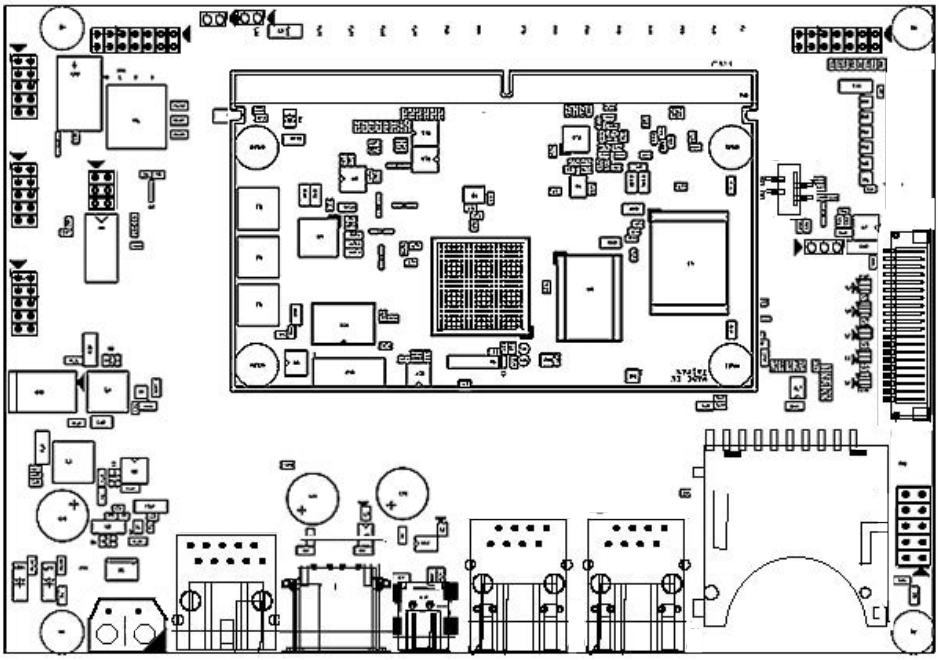


Figure 3-1: SBC-SMART-BEE Connectors, Headers and Jumpers (Top Side)

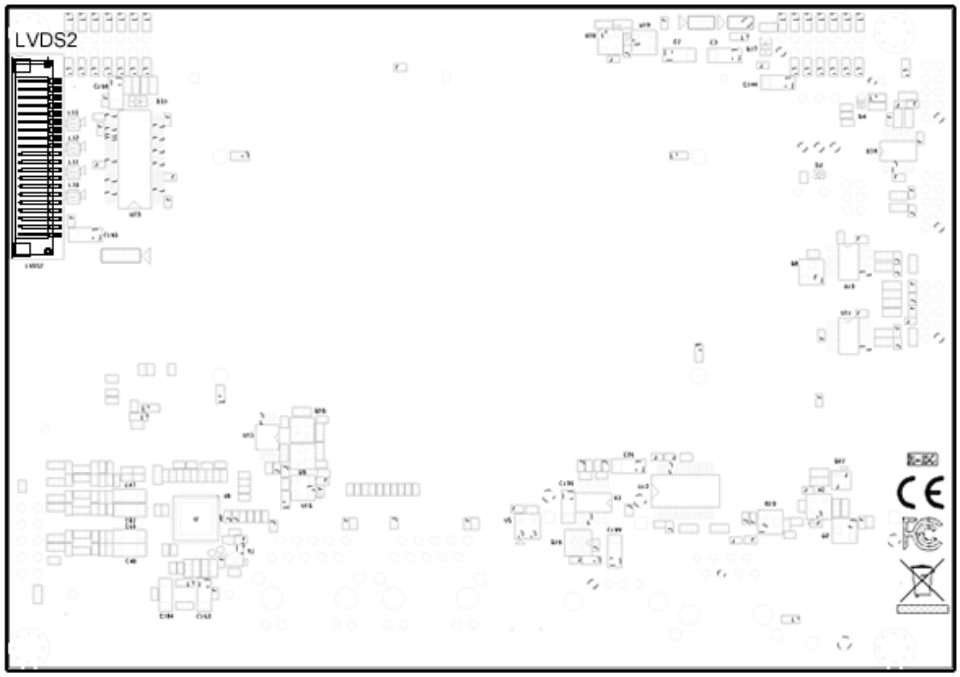


Figure 3-2: SBC-SMART-BEE Connectors, Headers and Jumpers (Bottom Side)

1.6 Mounting Holes Mechanical Drawing

Figure 4 shows the mounting holes information of *SBC-SMART-BEE*. The diameter of mounting hole is 3.2mm and the diameter of the ring is 6mm.

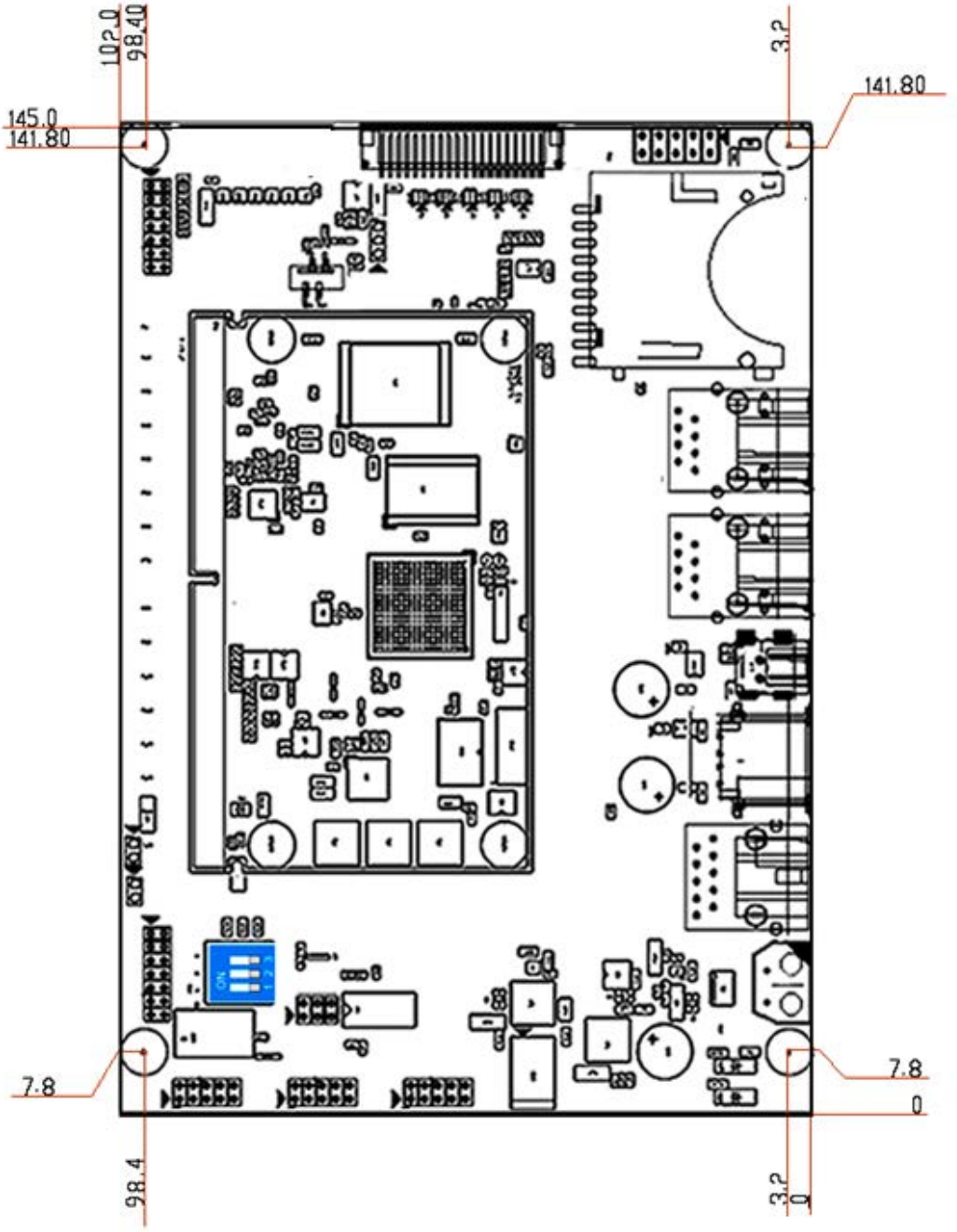


Figure 4: SBC-SMART-BEE Mounting Holes Mechanical Drawing Information

1.7 Document and Standard References

1.7.1. External Industry Standard Documents

- ***eMMC (Embedded Multi-Media Card)*** the eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (www.jedec.org).
- ***The I2C Specification,*** Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com).
- ***I2S Bus Specification,*** Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com).
- ***JTAG (Joint Test Action Group*** defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (www.ieee.org).
- ***MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification,*** Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (www.mxm-sig.org).
- ***PICMG® EEEP Embedded EEPROM Specification,*** Rev. 1.0, August 2010 (www.picmg.org).
- ***SD Specifications Part 1 Physical Layer Simplified Specification,*** Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (www.sdcard.org).
- ***SPI Bus –*** "Serial Peripheral Interface" - de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus).
- ***USB Specifications*** (www.usb.org).

1.7.2. SGET Documents

- ***SMARC_Hardware_Specification_V1p0***, version 1.0, December 20, 2012.

1.7.3. Embedian Documents

The following documents are listed for reference. The Module schematic is not usually available outside of Embedian, without special permission. The other schematics may be available, under NDA or otherwise. Contact your Embedian representative for more information. The SMARC T335x Evaluation Carrier Board Schematic is particularly useful as an example of the implementation of various interfaces on a Carrier board.

- ***SMARC_T335x Evaluation Carrier Board Schematic***, PDF and OrCAD format
- ***SMARC_T335x Evaluation Carrier Board User's Manual***
- ***SMARC_T335x Carrier Board Hardware Design Guide***
- ***SMARC_T335x Carrier Board Hardware Layout Guide***
- ***SMARC_T335x User's Manual***
- ***SMARC_T335X Schematic Checklist***

1.7.4. TI Documents

- ***AM335x ARM Cortex-A8 Microprocessors (MPUs),*** April 15 2013 (rev. F)
- ***AM335x Schematic Checklist***, Oct 31 2011
- ***AM335x ARM Cortex-A8 Microprocessors (MPUs) Technical References Manual***, April 15 2013 (rev. H)
- ***AM335x Power Consumption Summary***, Oct 31 2011

1.7.5. TI Development Tools

- ***Pin Mux Utility for ARM® Microprocessors***
- ***Power Estimation Tool (PET)***

1.7.6. TI Software Documents

- ***LINUXEZSDK-AM335x***
- ***ANDROIDDEVKIT-JB-AM335x***

1.7.7. Embedian Software Documents

- ***Embedian Linux BSP for SMARC T335X Module***
- ***Embedian Android BSP for SMARC T335X Module***
- ***Embedian Linux BSP User's Guide***
- ***Embedian Android BSP User's Guide***

1.7.8. TI Design Network

- ***Beaglebone***
- ***Beaglebone Blask***

Embedian, Inc.

- ***Adeneo Embedded (Windows Embedded Compact 7)***
- ***Nucleus***
- ***QNX***

Jumpers, Switches and LEDs

This Chapter provides SBC-SMART-BEE jumpers, switches and LEDs information.

Section include：

- Jumpers
- Switches
- LEDs

Chapter 2 Jumpers, Switches and LEDs

This chapter gives detail information of the jumpers, switches and LEDs.

2.1 Jumpers

The SBC-SMART-BEE has a number of jumpers that allow you to configure your system to suit your application. All use 2mm shorting blocks (shunts) to select settings. Turn off power to the SBC-SMART-BEE before changing the position of a shunt.

2.1.1. Jumper Location

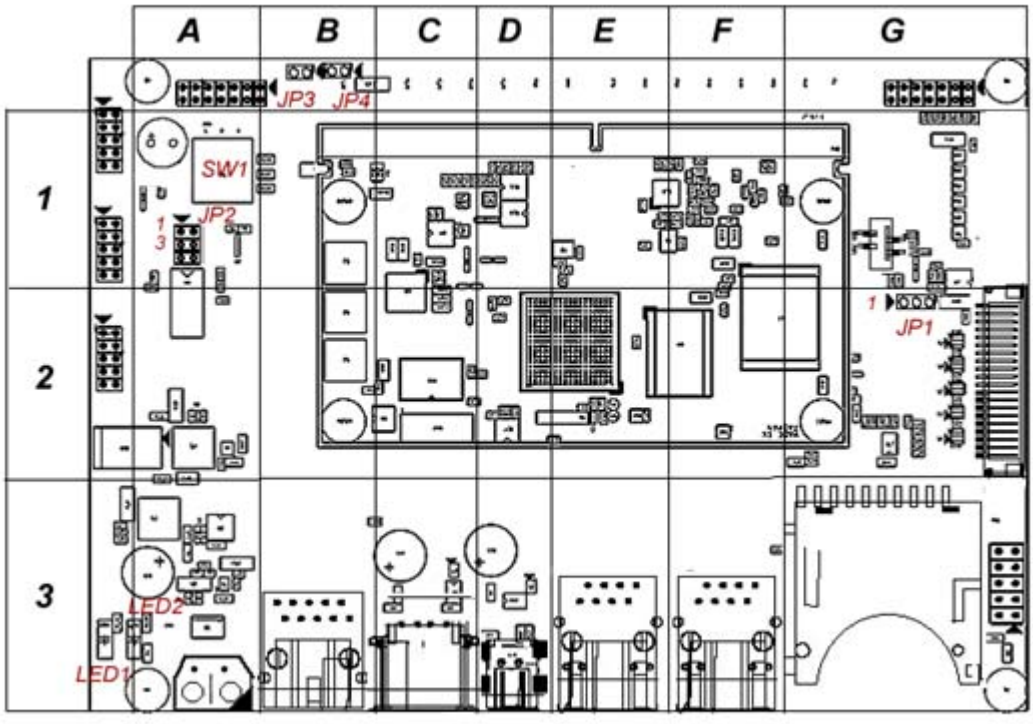


Figure 5: Jumper Locations

2.1.2. List of Jumpers

The table below lists the function of various jumpers.

Label	Function
JP1	*3.3V/5V LCD Signaling Voltage*
JP2	*RS232/RS422/RS485 Setting for SER0 (UART0)*
JP3	*Hardware Reset*
JP4	*External WatchDog Timer*

2.1.3. Jumper Settings

The following tables describe how the jumper shunts to various configurations.

JP1: *Location on Board, G2*

JP1	3.3V/5V LCD Signaling Voltage	
	Setting	**Function**
	JP1 (1-2)	*3.3V*
	JP1 (2-3)	*5V*

JP2: *Location on Board, A1*

JP2	RS232/RS422/RS485 Settings	
	Setting	**Function**
	JP2 (1-2)	*RS232*
	JP2 (3-4)	*RS422/RS485 half duplex*
	JP2 (5-6)	*RS422/RS485 full duplex*

JP3: *Location on Board, B1*

JP3	Hardware Reset	
	Setting	**Function**
	Shunt JP3 and Release Immediately	*Hardware Reset*

JP4: *Location on Board, B1*

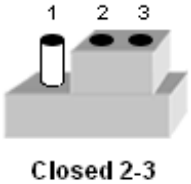
JP4	External Watchdog Timer	
	Setting	**Function**
	JP4 Open	*Disable External WDT*
	JP4 Closed	*Enable External WDT*

2.1.4. Setting Jumpers

You configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip.
To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2 or 2 and 3.


Open


Closed

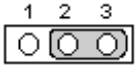


Closed 2-3

The jumper settings are schematically depicted in this manual as follows.


Open


Closed



Closed 2-3

A pair of needle-nose pliers may be helpful when working with jumpers. If you have any doubts about the best hardware configuration for your application, contact your sales representative before you make any change.

2.2 Switches

The *SBC-SMART-BEE* has one switch (SW1) that could determine the boot devices.

2.2.1. Switch Location

The SW1 switch for boot configuration is located at *A1* as shown in the following figure.

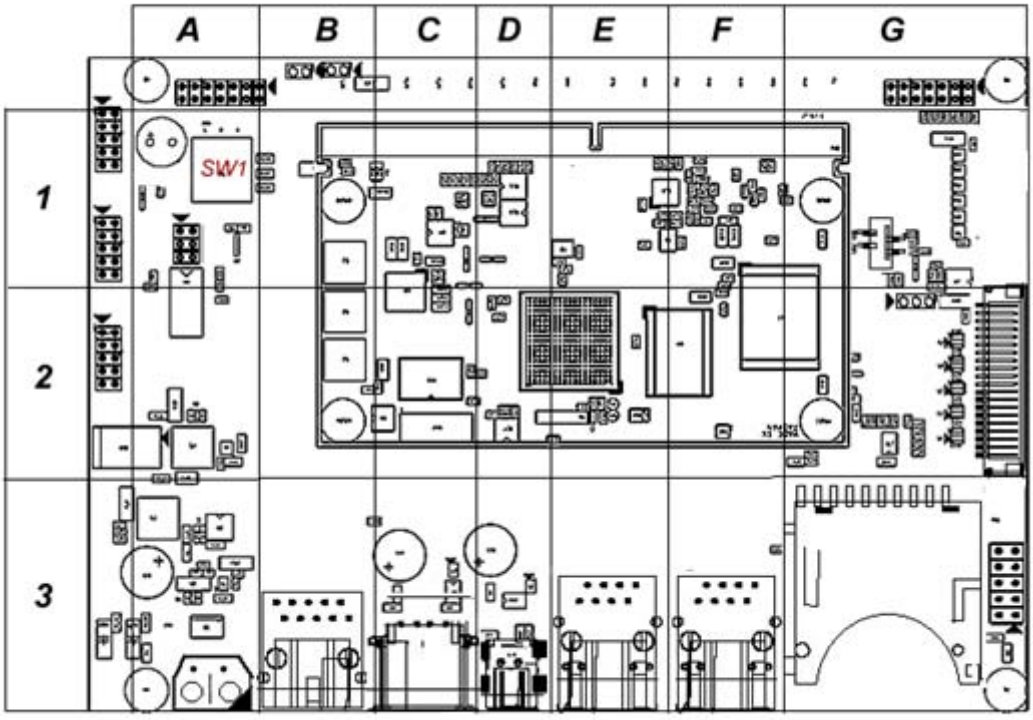


Figure 6: Switch Locations

2.2.2. List of Booting Device Configuration

The table below lists the booting device configuration setting by SW1.

SW1			Function
1	2	3	Boot Configuration
ON	OFF	OFF	Carrier SD Card (CN16)
OFF	ON	ON	Module eMMC Flash M

2.3 LEDs

The *SBC-SMART-BEE* has two LEDs to indicate the 5V and 3.3V power status. When power is fine, the LED will light on.

2.3.1. LEDs Location

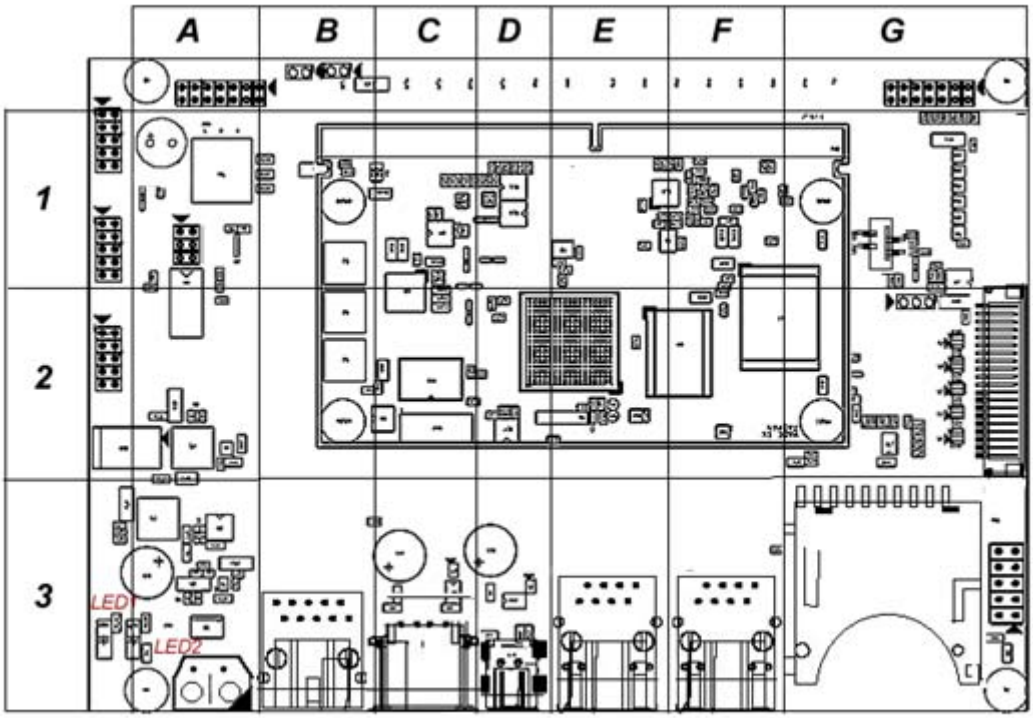


Figure 7: LED Locations

2.3.2. List of LEDs

The table below lists the function of LEDs.

Label	Function
LED1	*ON, if 5V is fine*
LED2	*ON, if 3.3V is fine*

Connectors and Headers

This Chapter gives SBC-SMART-BEE connectors and headers detail information.

Section include：

- Connectors
- Headers

Chapter 3 Headers and Connectors

This section gives SBC-SMART-BEE connectors and headers detail information.

3.1 Connectors

Wired connections to the *SBC-SMART-BEE* single board computer are described in this section.

3.1.1. Connector Location

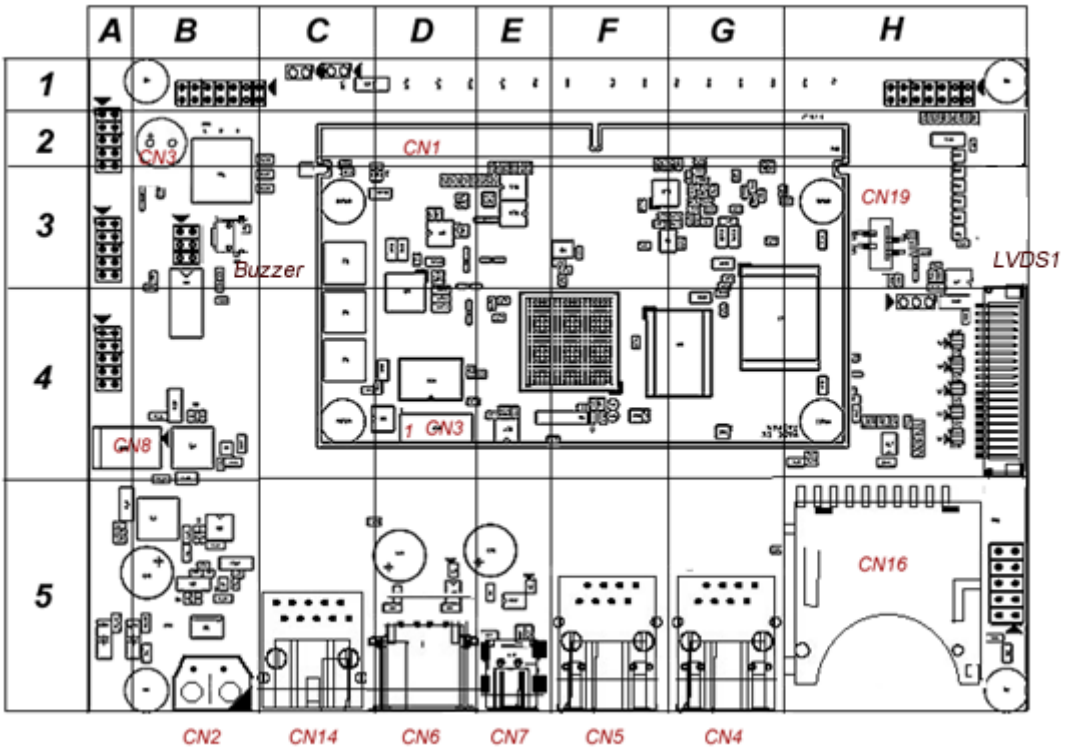


Figure 8-1: Connector Locations (Top)

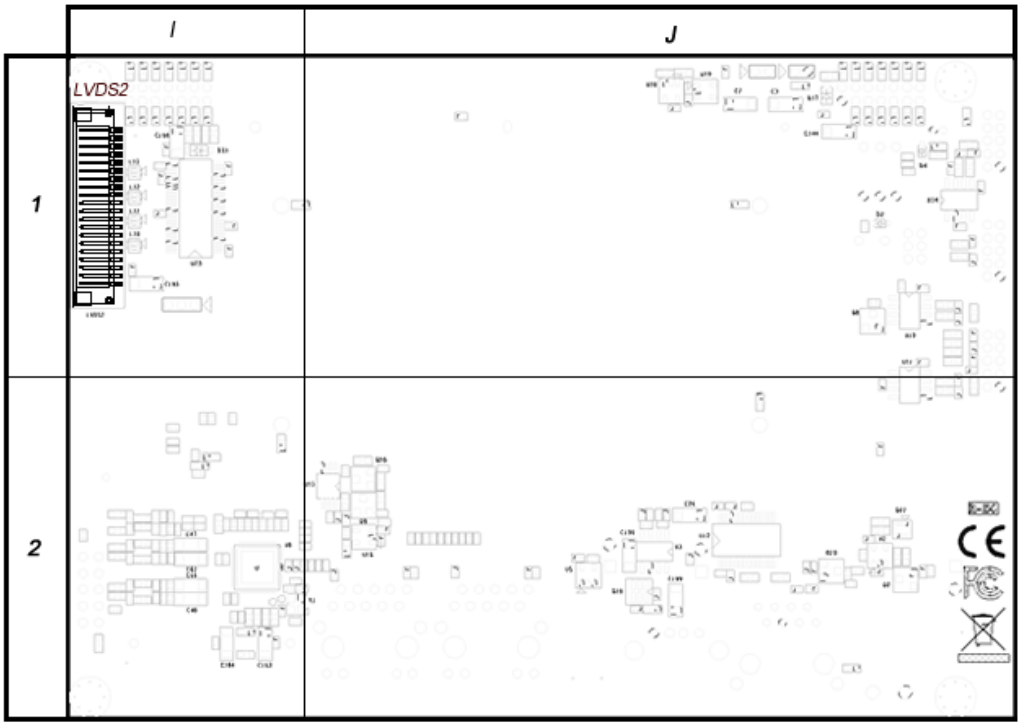


Figure 8-2: Connector Locations (Bottom)

3.1.2. List of Connectors

The table below lists the function of various connectors.

Label	Function
CN1	*314-pin MXM3.0 SMARC Module Connector*
CN2	*Power Input 2-pin Terminal Block*
CN3	*RTC Backup Battery*
CN4	*LAN1 RJ45 Jack with Integrated Magnetic*
CN5	*LAN2 RJ45 Jack with Integrated Magnetic*
CN6	*USB Host Type A Connector*
CN7	*USB OTG mini Type B Connector*
CN8	*LCD LED Backlight Connector*
LVDS1	*24-bit Single Channel LVDS Connector*
LVDS2	*18-bit Single Channel LVDS Connector*
CN14	*Serial Console RJ45 Connector (SER3/UART3)*
CN16	*SD/SDHC Connector*
CN19	*4-wire Touch Connector*
CN3 (on Module)	*JTAG Connector*
Buzzer	

3.1.3. Connector Pin Assignments

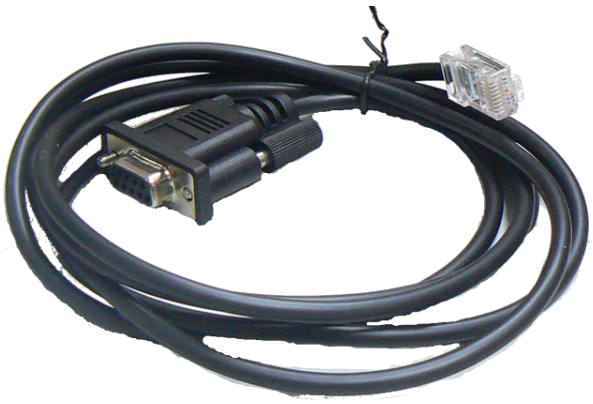
The following tables describe the electrical signals available on the connectors of the SBC-SMART-BEE. Each section provides relevant details about the connector including part numbers, mating connectors, signal descriptions and references to related chapters.

Pinout Legend

I	*Input*
O	*Output*
I/O	*Input or output*
P	*Power*
AI	*Analogue input*
AO	*Analogue output*
AIO	*Analogue Input or analogue output*
OD	*Open Drain Signal*
#	*Low level active signal*

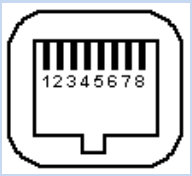
3.1.3.1. Serial Console Debug Connector: CN14

SBC-SMART-BEE provides with one serial console port that using RJ45 as the connector. The serial console port is available through a RJ-45 connector (CN14). A RJ45 to DB9 cable with 1m long comes with the evaluation kit and is shown as follows.



The following table shows the pin-out of the CN14 serial console connector.

CN14: *Location on Board, C5*

	8-pin RJ45 Connector			Edge Finger	Sitara AM335x CPU			Type
Header	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
	1	NC	Not Connected					
	2	SER3_TX	Transmit Data	P140	L16	1	UART3_TXD	O
	3	SER3_RX	Receive Data	P141	L17	1	UART3_RXD	I
	4	NC	Not Connected					
	5	GND	Ground					P
	6	NC	Not Connected					
	7	NC	Not Connected					
	8	NC	Not Connected					

3.1.3.2. USB Host Type A Connector: CN6

SBC-SMART-BEE provides with one USB 2.0 host type A connector (CN6).

The following table shows the pin-out of the CN6 USB host connector.

CN6: *Location on Board, D5*

	USB Type A Connector			Edge Finger	Sitara AM335x CPU			Type
Header	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
	1	USB1_VBus	USB1 -supply (max. 500mA)					P
	2	USB1-	Universal serial bus port 1 (-)	P66	R17	0	USB1_DM	IO
	3	USB1+	Universal serial bus port 0 (+)	P65	R18	0	USB1_DP	IO
	4	USB_GND	USB Ground					P

Note:

To protect the external power lines of peripheral devices, make sure that:
-- The wires have the right diameter to withstand the maximum available current.
-- The enclosure of the peripheral device fulfills the fire-protecting requirements of IEC/EN 60950.
The USB power lines are protected with a resetable fuse and are limited to 500mA.
If the USB device is powered from the *SBC-SMART-BEE* directly, not from the external power, make sure that the total power consumption does not exceed the DC power budget.

3.1.3.3. USB OTG Mini Type B Connector: CN7

SBC-SMART-BEE provides with one USB 2.0 OTG mini type B connector (CN7).

The following table shows the pin-out of the CN7 USB OTG connector.

CN7: *Location on Board, E5*

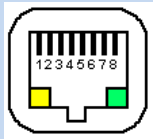
	USB OTG Mini Type B Connector			Edge Finger	Sitara AM335x CPU			Type
Header	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
	1	USB0_VBus	Power Supply					P
	2	USB0-	Data-	P61	N18	0	USB0_DM	IO
	3	USB0+	Data+	P60	N17	0	USB0_DP	IO
	4	USB0_OTG_ID	Host cable identification	P64	P16	0	USB0_ID	IO
	5	GND	Ground					P

3.1.3.4. Gigabit LAN RJ45 Connector: CN4 and CN5

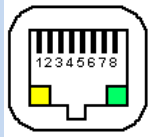
SBC-SMART-BEE provides with two Gigabit LAN RJ45 connectors (CN4 and CN5).

The following table shows the pin-out of the CN4 (LAN1) and CN5 (LAN2) connectors.

CN4 (LAN1): *Location on Board, G5*

	Gigabit RJ45 Connector			Edge Finger	Sitara AM335x CPU			Type
Header	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
	1	GBE_MDI0+	Transmit Data+	P30	From SMSC LAN8720A			AO
	2	GBE_MDI0-	Transmit Data-	P29				AO
	3	GBE_MDI1+	Receive Data+	P27				AI
	4	GBE_MDI2+	Transmit Data+	P26				NC
	5	GBE_MDI2-	Transmit Data-	P24				NC
	6	GBE_MDI1-	Receive Data-	P23				AI
	7	GBE_MDI3+	Receive Data+	P20				NC
	8	GBE_MDI3-	Receive Data-	P19				NC
	L	Left LED	Duplex	P21/ P22				Yellow
	R	Right LED	Link and Ack	P25				Green

CN5 (LAN2): *Location on Board, F5*

	Gigabit RJ45 Connector			Edge Finger	Sitara CPU		AM335x	Type
Header	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
	1	GBE1_MDI0+	Transmit Data+	S62	From SMSC LAN8720A			AO
	2	GBE1_MDI0-	Transmit Data-	S63				AO
	3	GBE1_MDI1+	Receive Data+	S65				AI
	4	GBE1_MDI2+	Transmit Data+	S66				NC
	5	GBE1_MDI2-	Transmit Data-	S68				NC
	6	GBE1_MDI1-	Receive Data-	S69				AI
	7	GBE1_MDI3+	Receive Data+	S71				NC
	8	GBE1_MDI3-	Receive Data-	S72				NC
	L	Left LED	Duplex	S23/ S24				Yellow
	R	Right LED	Link and Ack	S55				Green

Note:

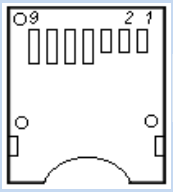
SBC-SMART-BEE supports two fast LANs (10/100Mbps). SBC-SMART-BEE uses RJ45 connectors with integrated Gigabit Magnetic. The reason for that is because SBC-SMART-BEE could be used to support other 3.3V SMARC module from other vendors.

3.1.3.5. SD/SDHC Connector: CN16

SBC-SMART-BEE provides with one SD/SDHC connector (CN16). The SD slot could be used as a boot device or as a standard storage.

The following table shows the pin-out of the CN16 SD/SDHC connector.

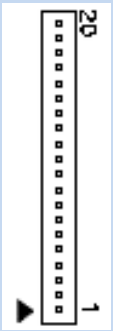
CN16: *Location on Board, H5*

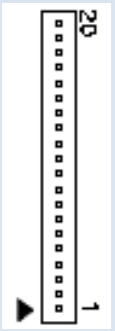
	SD/SDHC Connector			Edge Finger	Sitara AM335x CPU			Type
Header	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
	1	SDIO_CD# /SDIO_D3	SD Insert Detect/ SD receive/transmit data	P35/ P42	U14/ F17	7/0	GPIO1 [18]/ MMC0_ DAT3	I/IO
	2	SDIO_CMD	SD receive response/ transmit command	P34	G18	0	MMC0_ CMD	O
	3	GND	Ground					P
	4	VDD_SD0	Power					P
	5	SDIO_CK	SD Clock	P36	G17	0	MMC0 _CLK	I
	6	GND	Ground					P
	7	SDIO_D0	SD receive/transmit data	P39	G16	0	MMC0_ DAT0	O
	8	SDIO_D1	SD receive/transmit data	P40	G15	0	MMC0_ DAT1	O
	9	SDIO_D2	SD receive/transmit data	P41	F18	0	MMC0_ DAT2	O
	10	SDIO_WP	SD Write Protect	P33	V14	7	GPIO1 [17]	I

3.1.3.6. 18-bit LVDS Connector: LVDS2

SBC-SMART-BEE provides with one LCD 18-bit LVDS connector (LVDS2) and one 24-bit LVDS connector (LVDS1). LVDS2 (bottom side) supports 18-bit color depths.
The following table shows the pin-out of the LVDS2 LVDS LCD connector.

LVDS2: *Location on Board, I1 (Bottom Side)*

	LVDS Connector: *CONN. DF14-20P-1.25H			***Edge Finger***	***Sitara AM335x CPU***			***Type***
Header	*Pin*	*Signal Name*	*Function*	*Pin#*	*Ball*	*Mode*	*Signal Name*	
	1	*1*	*GND*					*P*
	2	*2*	*GND*					*P*
	3	*3*	*NC*					*NC*
	4	*4*	*NC*					*NC*
	5	*5*	*GND*					*P*
	*6*	*6*	*CLKP*					*O*
	7	*7*	*CLKM*					*O*
	8	*8*	*GND*					*P*
	9	*9*	*A2P*					*O*
	10	*10*	*A2M*					*O*
	11	*11*	*GND*					*P*
	12	*12*	*A1P*					*O*
	13	*13*	*A1M*					*O*
	14	*14*	*GND*					*P*
	15	*15*	*A0P*					*O*
	16	*16*	*A0M*					*O*
	17	*17*	*GND*					*P*

	LVDS Connector: *CONN. DF14-20P-1.25H			Edge Finger	Sitara AM335x CPU			Type
Header	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
	18	18	GND					P
	19	19	VCC (3.3V or 5V)					P
	20	20	VCC (3.3V or 5V)					P

Note:

LVDS2 18-bit LVDS signal from CPU LCD controller. In the 18-bit single pixel mode, the RGB and control inputs shall be transmitted as shown in Figure 9. Outputs A3 through A7 and CLK2 shall be inactive in this mode and fixed at a single value.

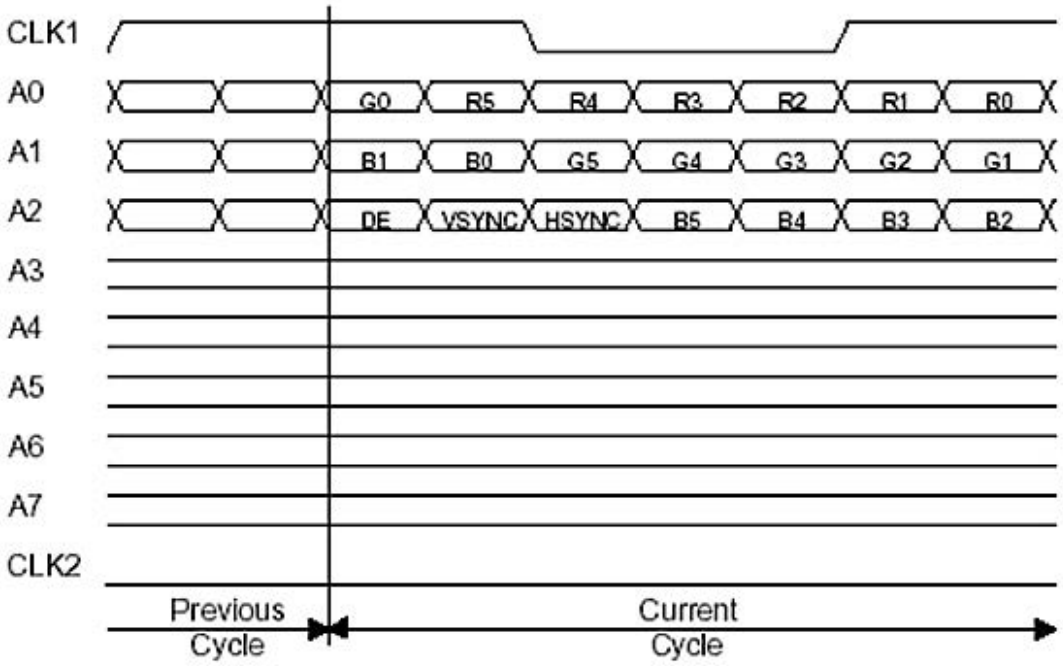
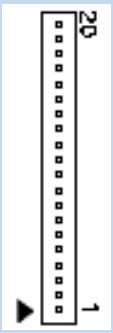


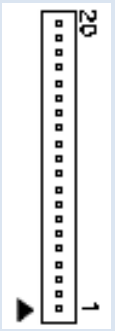
Figure 9: 18-bit Single Pixel Transmission, Unbalanced

3.1.3.7. 24-bit LVDS Connector: LVDS1

SBC-SMART-BEE provides with one LCD LVDS connector (LVDS1). It supports 24-bit color depths. The LVDS signal is implemented from parallel RGB LCD signals via a TI SN75LVDS83B interface IC on carrier board.
The following table shows the pin-out of the LVDS1 LCD LVDS connector.

LVDS1: *Location on Board, H4*

	LVDS Connector: *CONN. DF14-20P-1.25H			Edge Finger	Sitara AM335x CPU			Type
Header	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
	1	1	GND					P
	2	2	GND					P
	3	3	A3P					O
	4	4	A3M					O
	5	5	GND					P
	6	6	CLKP					O
	7	7	CLKM					O
	8	8	GND					P
	9	9	A2P					O
	10	10	A2M					O
	11	11	GND					P
	12	12	A1P					O
	13	13	A1M					O
	14	14	GND					P
	15	15	A0P					O
	16	16	A0M					O
	17	17	GND					P

	LVDS Connector: *CONN. DF14-20P-1.25H			Edge Finger	Sitara AM335x CPU			Type
Header	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
	18	18	GND					P
	19	19	VCC (3.3V or 5V)					P
	20	20	VCC (3.3V or 5V)					P

Note:

LVDS1 is a 24-bit color depth LVDS signal. In the 24-bit single pixel mode, the RGB and control inputs shall be transmitted as shown in the following figure. Outputs A4 through A7 and CLK2 shall be inactive in this mode and fixed at a single value. Bits marked RES are reserved for future use and may take any value.

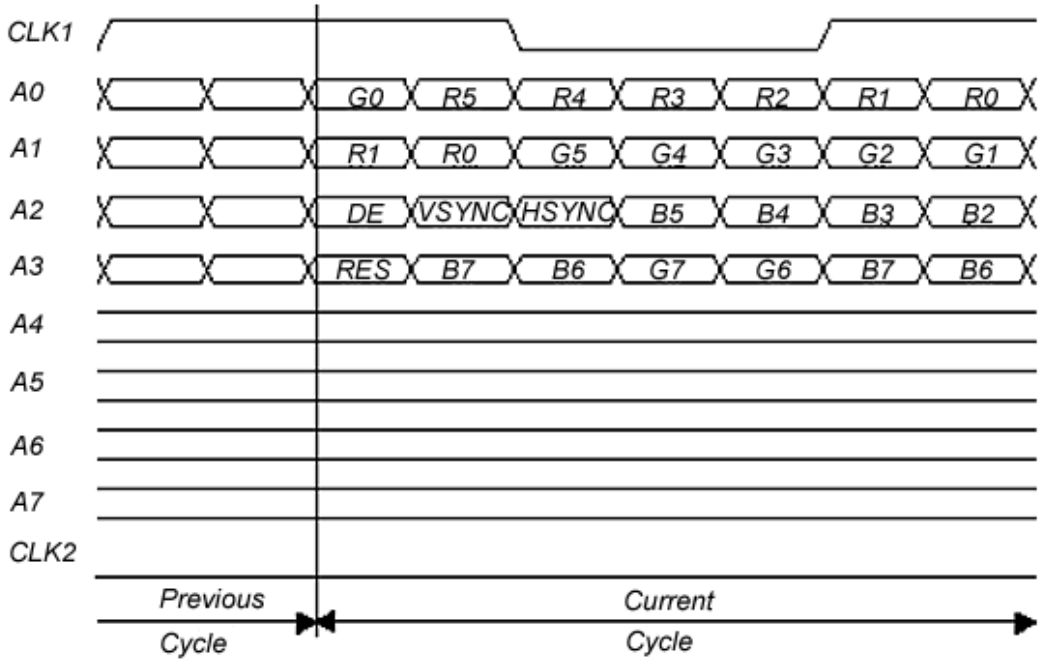
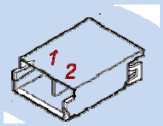


Figure 10: 24-bit Single Pixel Transmission, Unbalanced

3.1.3.8. LCD LED Backlight Connector: CN8

SBC-SMART-BEE provides with one LCD LED backlight connector (CN8) that can drive up to 10 LEDs in series. The driver IC is TI *TPS61165*.
The following table shows the pin-out of the CN8 LED backlight connector.

CN8: *Location on Board, A4/B4*

	LED Backlight Connector: ***JST SM02B-BHSS-1-TB or compatible***			***Edge Finger***	***Sitara AM335x CPU***			***Type***
Header	*Pin*	*Signal Name*	*Function*	*Pin#*	*Ball*	*Mode*	*Signal Name*	
	*1*	*BLH*	*Backlight Drive (Anode Side)*		*From TPS61165*			*P*
	2	*BLL*	*Backlight Drive (Cathode Side)*		*From TPS61165*			*P*

Note:

The mating connector is JST *BHSR-02VS-1* or compatible. The backlight control pin is *ecap0_in_pwm0_out.gpio0_7*.

3.1.3.9. Power Input Terminal Block Connector: CN2

The power input connector of *SBC-SMART-BEE* is using a 2-pin 5mm terminal block and located at CN2. The input power should be 5V. There are +28V over voltage and -28V miswiring protection.

The following table shows the pin-out of the CN2 power input terminal block connector.

CN2: *Location on Board, B5*

	Power Input Connector: 2-pin screw type terminal block			Edge Finger	Sitara AM335x CPU			Type
Header	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
	1	5V	5V Input					P
	2	GND	Ground Power					P

3.1.3.10. SMARC Module Connector: CN1

The SMARC Module is supported on CN1. This is a 314 pin MXM3 style connector. The CN1 pin-out conforms to the SMARC Module specification. Only 3.3V Module I/O can be supported on the SMARC T335X Evaluation Carrier.

The MXM3 style connector used on the *SBC-SMART-BEE* carrier board is with a board-to-board spacing of 5mm. Other stack height options are available, including 1.8MM, 2.7mm and 8mm.

The carrier board has captive M2.5 threaded standoffs in the SMARC mounting hole positions. The standoffs accept M2.5 screws, inserted from above, through the Module holes.

Only 82mm x 50mm format SMARC Modules may be used with the SBC-SMART-BEE carrier board. The carrier board PCB has a cut-out allowing access to the back side of the SMARC Module for test and debug.

3.1.3.11. RTC Backup Battery: CN3

A 6.8mm diameter 3V lithium coin cell battery is available on the Evaluation Carrier in position CN3. The part number of coin cell battery on CN3 is *Seiko MS621F_FL11E*.

The battery '+' terminal is protected against charging (as required by safety regulations) by a Schottky diode and a 49.9 Ohm resistor (R10). The 49.9 resistor feeds the SMARC VDD_RTC pin (SMARC pin S147).

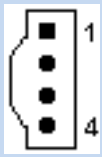
CN3: *Location on Board, B2*

3.1.3.12. 4-wire Touch Connector: CN19

SBC-SMART-BEE provides with a 4-wire FPC connector for touch panel. The controller is from ADC of the processor.

The following table shows the pin-out of the CN19 4-wire resistive connector.

CN19: *Location on Board, H3*

	4-wire Touch Connector: 1.0 ZIF FPC SMT V/T			Edge Finger	Sitara AM335x CPU			Type
Header	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
	1	XNUR	Left	S21	C7		AIN1	AI
	2	YPLL	Bottom	S19	B7		AIN2	AI
	3	XPUL	Right	S18	B6		AIN0	AI
	4	YNLR	Top	S22	A7		AIN3	AI

Note:

The length of touch FPC cable should not be keeping too long.

3.1.3.13. JTAG Connector: CN3 on Module

JTAG functions for CPU debug and test are implemented on separate small form factor connector (CN3: *JST SM10B-SRSS-TB*, 1mm pitch R/A SMD Header) on SMARC module. The JTAG pins are used to allow test equipment and circuit emulators to have access to the Module CPU. The pin-outs shown below are used:

The following table shows the pin-out of the CN3 (on module) JTAG connector.

CN3: *Location on Board, D4*

	JTAG Connector: ***JST SM10B-SRSS-TB, 1mm pitch R/A SMD Header***			***Edge Finger***	***Sitara AM335x CPU***			***Type***
Header	*Pin*	*Signal Name*	*Function*	*Pin#*	*Ball*	*Mode*	*Signal Name*	
	*1*	*VDD_33A*	*JTAG I/O Voltage (sourced by Module)*					*P*
	2	*nTRST*	*JTAG Reset, active low*	*B10*		*nTRST*	*B10*	*I*
	3	*TMS*	*JTAG mode select*	*C11*		*TMS*	*C11*	*I*
	4	*TDO*	*JTAG data out*	*A11*		*TDO*	*A11*	*O*
	5	*TDI*	*JTAG data in*	*B11*		*TDI*	*B11*	*I*
	6	*TCK*	*JTAG clock*	*A12*		*TCK*	*A12*	*I*
	7	*RTCK*	*JTAG return clock*					*I*
	8	*GND*	*Ground*					*P*
	9	*MFG_Mode #*	*Pulled low to allow in-circuit SPI ROM update*					*I*
	10	*GND*	*Ground*					*P*

Note:

The mating connector part number is JST 10SR-3S.

3.1.3.14. Buzzer

Buzzer is controlled by GPIO10 from the SMARC module. User can use this GPIO and generate a square wave to control the buzzer.

The following table shows the pin-out of the GPIO10.

Buzzer: *Location on Board, B3*

Buzzer				Edge Finger	Sitara AM335x CPU			Type
Header	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
		GPIO10		P118	C14	7	GPIO3[7]	I/O

3.2 Headers

This section details the header information of *SBC-SMART-BEE* single board computer.

3.2.1. Header Location

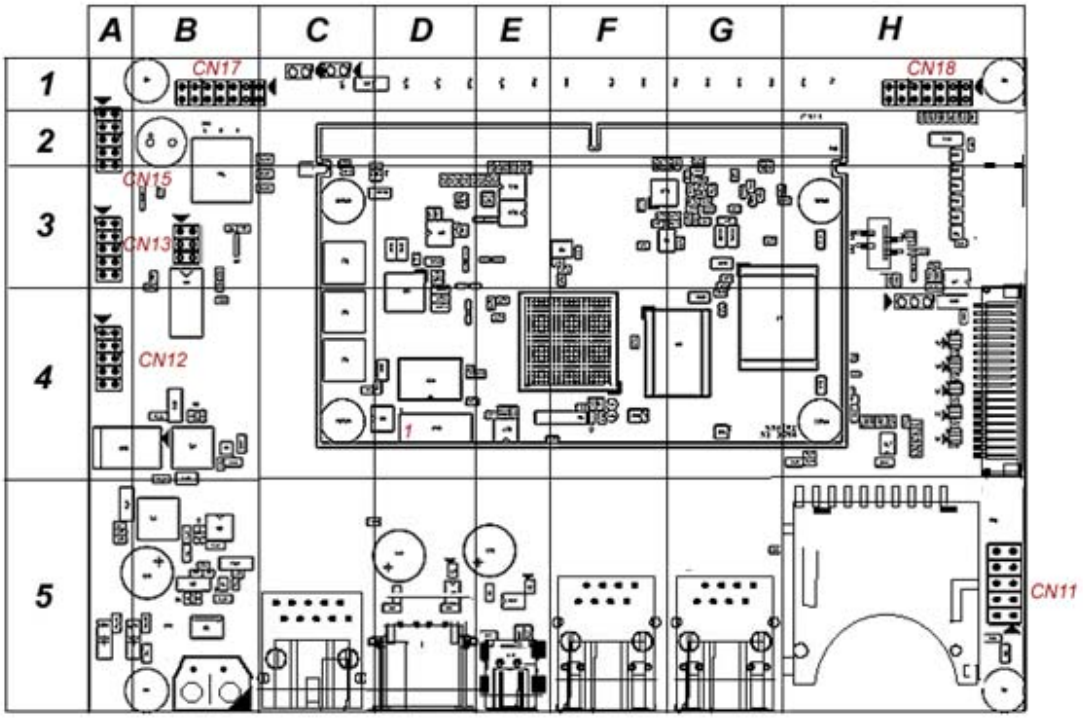


Figure 11: Header Locations

3.2.2. List of Headers

The table below lists the function of various headers.

Label	Function
CN12	*RS232/RS422/RS485 port (SER0/UART0) with hardware handshaking*
CN13	*RS232 port (SER1/UART1)*
CN15	*CAN Bus Header*
CN17	*GPIO Header*
CN18	*I2C (2) and SPI (2) Header*
CN11	*Mic, In and Speaker Out Audio Header*

3.2.3. Header Pin Assignments

The following tables describe the electrical signals available on the connectors of the SBC-SMART-BEE. Each section provides relevant details about the connector including part numbers, mating connectors, signal descriptions and references to related chapters.

Pinout Legend

I	*Input*
O	*Output*
I/O	*Input or output*
P	*Power*
AI	*Analogue input*
AO	*Analogue output*
AIO	*Analogue Input or analogue output*
OD	*Open Drain Signal*
#	*Low level active signal*

3.2.3.1. Asynchronous Serial Ports Header: CN12 and CN13

The SMARC T335X Evaluation Carrier supports three serial ports defined in the SMARC specification. They are SER0, SER1 and SER3. SER3 is also used as a serial debug port that is described in section 3.1.3.1. The Evaluation Carrier has EIA RS232/RS422/RS485 compliant signal levels and polarities. Per the SMARC specification, one of the three ports (SER0) have RTS/CTS handshaking, and two (SER1 and SER3) have TX and RX data only, without handshaking.
The Evaluation Carrier runs SER0 and SER1 through one transceiver and SER3 through a 2nd transceiver. The Evaluation Carrier could also runs SER0 via JP2 setting through a SN75HVD11D transceiver to become a RS422 or RS485 signals.

A 10-way box header to DB9 cable with 20cm long comes with the evaluation kit for users easily testing the functions and is shown as follows.

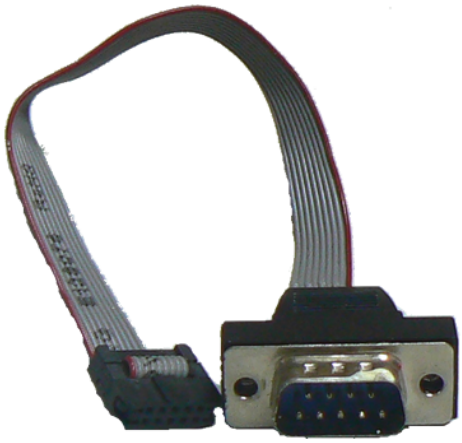
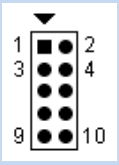


Figure 12: 10-way box header to DB9 cable

The red line on the cable should align to pin 1 of the header.

The following table shows the pin-out of the CN12 and CN13 asynchronous serial port header.

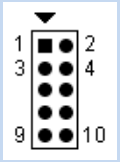
CN12: Location on Board, A4

Header	RS232/RS422/RS485 Header: HEADER DIP 10*2P 180D MALE 2.0mm			Edge Finger	Sitara AM335x CPU			Type
	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
	1	422_TX-/ 485_RX-						
	2	422_TX+/ 485_RX+						
	3	SER0_RX	Receive Data	P130	E15	0	UART0_RXD	I
	4	SER0_RTS	Ready to Send	P131	E17	0	UART0_RTSN	O
	5	SER0_TX	Transmit Data	P129	E16	0	UART0_TXD	O
	6	SER0_CTS	Clear To Send	P132	E18	0	UART0_CTSN	I
	7	422_RX+						
	8	422_RX-						
	9	GND						P
	10	NC						

Note:

The ones marked as blue are RS232 signals. When using RS232 as function, please shunt pin 1-2 of JP2.

CN13: *Location on Board, A3*

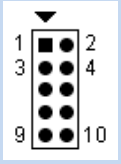
	RS232 Header: HEADER DIP 10*2P 180D MALE 2.0mm			***Edge Finger***	***Sitara AM335x CPU***			***Type***
Header	*Pin*	*Signal Name*	*Function*	*Pin#*	*Ball*	*Mode*	*Signal Name*	
	*1*	*NC*						
	2	*NC*						
	3	*SER1_RX*	*Receive Data*	*P135*	*K18*	*1*	*UART2_RXD*	*I*
	4	*NC*						
	5	*SER1_TX*	*Transmit Data*	*P134*	*L18*	*1*	*UART2_TXD*	*O*
	6	*NC*						
	7	*NC*						
	8	*NC*						
	9	*GND*						*P*
	10	*NC*						

3.2.3.2. CAN Bus Header: CN15

The SBC-SMART-BEE supports one CAN bus port and locates at CN15. It runs CAN0 through SN65HVD251D transceiver.

The following table shows the pin-out of the CN15 CAN Bus header.

CN15: *Location on Board, A2*

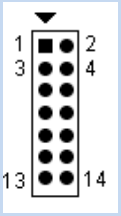
	CAN Bus Header: HEADER DIP 10*2P 180D MALE 2.0mm			Edge Finger	Sitara AM335x CPU			Type
Header	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
	1	NC						
	2	NC						
	3	CAN0L	CAN Signal Low	P144	K15	1	DCAN0_RX	I
	4	CAN0H	CAN Signal High	P143	J18	1	DCAN0_TX	O
	5	NC						
	6	NC						
	7	NC						
	8	NC						
	9	GND						P
	10	NC						

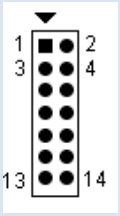
3.2.3.3. GPIO Header: CN17

The SBC-SMART-BEE single board computer supports 12 GPIO ports defined in the SMARC specification. The GPIO header locates at CN17.

The following table shows the pin-out of the CN17 GPIO header.

CN17: *Location on Board, B1*

	GPIO Header: HEADER DIP 14*2P 180D MALE 2.0mm			Edge Finger	Sitara AM335x CPU			Type
Header	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
	1	VDD_ GPIO						P
	2	GND						P
	3	GPIO0	Camera 0 Power Enable	P108	J17	7	GPIO3[4]	I/O
	4	GPIO6	Tachometer input	P114	U18	7	GPIO1[28]	I/O
	5	GPIO1	Camera 1 Power Enable	P109	T6	7	GPIO2[5]	I/O
	6	GPIO7	PCAM_FLD signal input	P115	V6	7	GPIO1[29]	I/O
	7	GPIO2	Camera 0 Reset	P110	U16	7	GPIO1[25]	I/O
	8	GPIO8	CAN0 Error signal,	P116	T13	7	GPIO2[0]	I/O
	9	GPIO3	Camera 1 Reset	P111	V16	7	GPIO1[24]	I/O

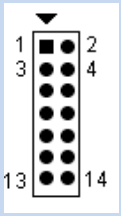
	GPIO Header: HEADER DIP 14*2P 180D MALE 2.0mm			Edge Finger	Sitara AM335x CPU			Type
Header	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
	10	GPIO9	CAN1 Error signal, active low input	P117	V12	7	GPIO2[1]	I/O
	11	GPIO4	HD Audio Reset	P112	U6	7	GPIO2[4]	I/O
	12	GPIO10		P118	C14	7	GPIO3[7]	I/O
	13	GPIO5	PWM output	P113	T7	7	GPIO2[3]	I/O
	14	GPIO11		P119	B14	7	GPIO3[8]	I/O

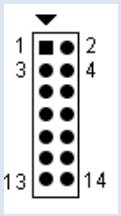
3.2.3.4. SPI and I2C Header: CN18

Two sets of SPI bus and I2C bus are presented in CN18.

The following table shows the pin-out of the CN18 SPI and I2C header.

CN18: *Location on Board, H1*

	SPI/I2C Header: HEADER DIP 14*2P 180D MALE 2.0mm			Edge Finger	Sitara AM335x CPU			Type
Header	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
	1	Reserved						
	2	SPI1_CS0#	SPI1 Master Chip Select 0 output	P54	C12	3	SPI1_CS0	O
	3	SPI0_CS1#	SPI0 Master Chip Select 1 output	P31	C15	0	SPI0_CS1	O
	4	SPI1_CS1#	SPI1 Master Chip Select 1 output	P55	A15	4	SPI1_CS1	O
	5	SPI0_SCLK	SPI0 Master Clock output	P44	A17	0	SPIO_SCLK	O
	6	SPI1_SCLK	SPI1 Master Clock output	P56	A13	3	SPI1_SCLK	O
	7	SPI0_MOSI	SPI0 Master Data output (output from CPU, input to SPI device)	P46	B16	0	SPI0_D1	O
	8	SPI1_MOSI	SPI1 Master Data output (output from CPU, input to SPI device)	P58	D12	3	SPI1_D1	O

	SPI/I2C Header: HEADER DIP 14*2P 180D MALE 2.0mm			Edge Finger	Sitara AM335x CPU			Type
Header	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
	9	SPI0_ MISO	SPI0 Master Data input (input to CPU, output from SPI device)	P45	B17	0	SPI0_D0	I
	10	SPI1_ MISO	SPI1 Master Data input (input to CPU, output from SPI device)	P57	B13	3	SPI1_D0	I
	11	I2C_GP_ CK	General purpose I2C bus clock	S48	D15	3	I2C1_SCL	OD
	12	I2C_LCD _GK	LCD display I2C bus clock	S139	D17	3	I2C2_SCL	OD
	13	I2C_GP_ DAT	General purpose I2C bus data	S49	D16	3	I2C1_SDA	OD
	14	I2C_LCD _DAT	LCD display I2C bus data	S140	D18	3	I2C2_SDA	OD

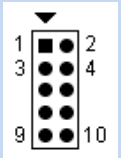
3.2.3.5. I2S Device Header: CN11

The I2S0 channel on the SBC-SMART-BEE is run through a TLV320AIC3106 audio codec allowing I2S0 to/from Evaluation Carrier Audio CODEC. I2C0 bus is also connected to TLV320AIC3106 to send command to audio codec and read codec register information at address 0x1B.

The audio mic. In and headset speaker out header is located at CN11.

The following table shows the pin-out of the CN11.

CN11: *Location on Board, H5*

	Audio Header: HEADER DIP 10*2P 180D MALE 2.54mm			**Edge Finger**	**Sitara AM335x CPU**			**Type**
Header	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
	1	MIC_L	Left channel of microphone input	From TLV320AIC3016 Audio Codec				AI
	2	AGND	Analog Ground					P
	3	MIC_R	Right channel of microphone input					AI
	4	AUD_33	Analogue VDD_IO					P
	5	HP_OUT_R	Right channel of headset speaker					AO
	6	HP_OUT_RR	HPRCOM Signal of AIC3106					AO
	7	MICDEC	Microphone detect					
	8	NC						

	Audio Header: HEADER DIP 10*2P 180D MALE 2.54mm			Edge Finger	Sitara AM335x CPU			Type
Header	Pin	Signal Name	Function	Pin#	Ball	Mode	Signal Name	
	9	HP_OUT_L	Left channel of headset speaker out	From TLV320AIC3016 Audio Codec				
	10	HP_OUT_LR	HPLCOM Signal of AIC3106					

The following diagram shows the AIC3106 block diagram from digital end to analog end.

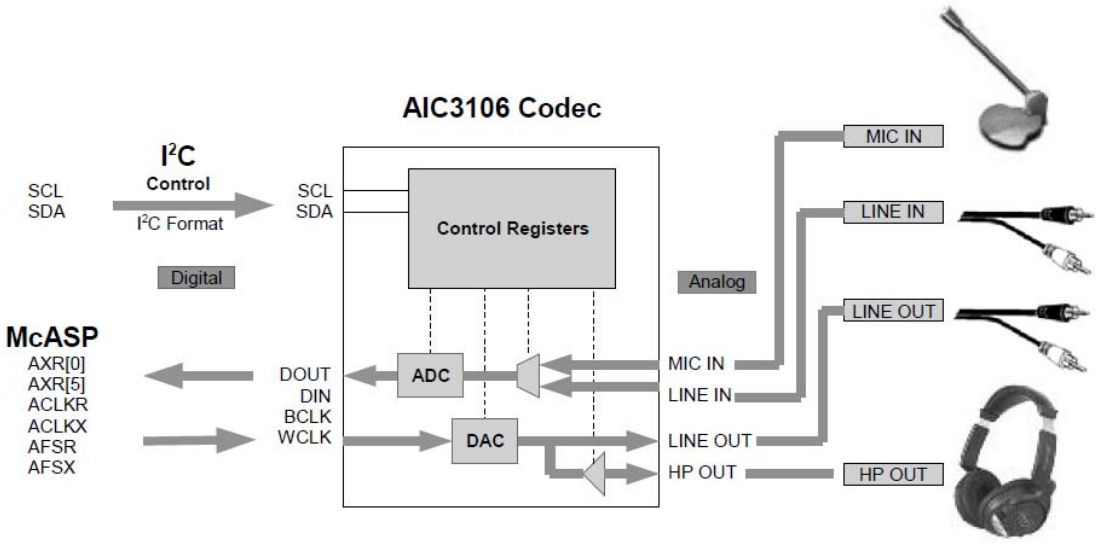


Figure 13: AIC3106 Block Diagram

I2C0 Devices and Carrier EEPROM Format

This Chapter points out the I2C0 device information.
Section include：

- I2C Devices on Carrier
- Carrier EEPROM Format

Chapter 4 I2C0 Devices and Carrier EEPROM Format

This chapter introduces I2C0 devices on SBC-SMART-BEE. Also, EEPROM format on carrier board will also be introduced.

4.1 I2C0 Devices

There are two I2C devices on the SBC-SMART-BEE Carrier and are all on the *I2C_PM* (*I2C0*) bus and are operated at 3.3V. Those devices and their address details are listed in the following table:

#	Device	Description	Address (7-bit)	Address (8-bit)		Notes
				Read	Write	
I2C_PM Bus						
1	TI TLV320AIC3106	Audio Codec	0x1B	0x37	0x36	General purpose usage address
2	On Semiconductor CAT64C32	EEPROM	0x57	0xAF	0xAE	General purpose parameter EEPROM, Serial number, etc in PICMG EEEP format

Note:

The I2C0 bus on SMARC module is operated at 1.8V. It has been level shifted to 3.3V on carrier board.

4.2 Carrier EEPROM Format

The SBC-SMART-BEE module includes an I2C serial EEPROM available on the I2C_PM bus. An On Semiconductor 24C32 or equivalent EEPROM is used in the Carrier. The device operates at 3.3V. The Module serial EEPROM is placed at I2C slave addresses A2 A1 A0 set to 1 (I2C slave address 57 hex, 7 bit address format or A0 / A1 hex, 8 bit format) (for I2C EEPROMs, address bits A6 A5 A4 A3 are set to binary 0101 convention).

The Carrier serial EEPROM is intended to retain carrier parameter information, including serial number. The carrier serial EEPROM data structure conforms to the PICMG® EEEP Embedded EEPROM Specification.

If developers have more than one carrier boards all using SMARC T335X as the core module, it is recommended to have an EEPROM on carrier. The advantage for that is the module will read the Carrier EEPROM information and load the specific hardware configurations. It will be secure and easy to maintain software.

Note:

The EEPROM ID memory layout is now follow the mainline and as follows.

Name	Offset	Size (bytes)	Contents
Header	0	4	0xAA, 0×55, 0×33, 0xEE
EEPROM Format Revision	4	2	Revision number of the overall format of this EEPROM in ASCII =A0
Board Name	6	32	Name of board in ASCII
Version	38	4	Hardware version code for board in ASCII
Manufacturer	42	16	ASCII name of the manufacturer
Part Number	58	16	ASCII Characters for the part number
Number of Pins	74	2	Number of pins used by the daughter board

Name	Offset	Size (bytes)	Contents
Serial Number	76	12	Serial number of the board. This is a 12 character string which is: MSCEWWYYnnnn Where: WW = 2 digit week of the year of production YY = 2 digit year of production nnnn = incrementing board number
Pin Usage	88	148	Two bytes for each configurable 74 pins on the expansion connectors Bit 15: Pin is used or not; 0=Unused by Cape 1=Used by Cape Bit 14-13: Pin Direction; 1 0=Output 01=Input 11=BDIR Bits 12-7: Reserved Bit 6: Slew Rate; 0=Fast 1=Slow Bit 5: Rx Enable; 0=Disabled 1=Enabled Bit 4: Pull Up/Dn Select; 0=Pulldown 1=PullUp Bit 3: Pull Up/DN enabled; 0=Enabled 1=Disabled Bits 2-0: Mux Mode Selection; Mode 0-7
VDD_3V3EXP Current	236	2	Maximum current in milliamps
VDD_5V Current	238	2	Maximum current in milliamps
SYS_5V Current	240	2	Maximum current in milliamps
DC Supplied	242	2	Indicates whether or not the board is supplying voltage on the VDD_5V rail and the current rating 000=No 1-0xFFFF is the current supplied
Available	244	32543	Available space for other non-volatile codes/data

Quick Start Guide

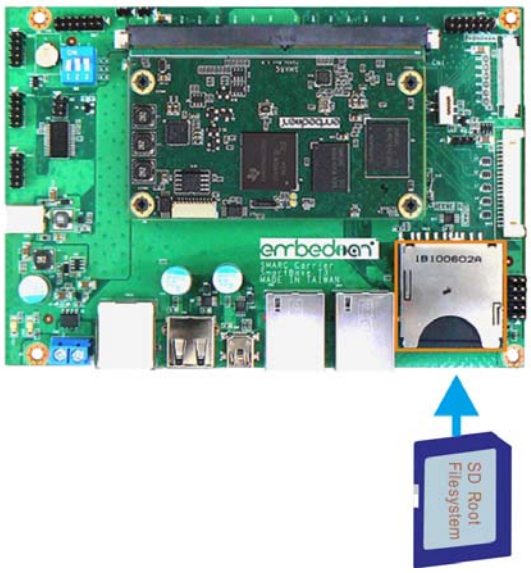
The purpose of this chapter is to provide a quick start guide so that developers can easily get the board up and running in few minutes.

Chapter 5 Quick Start Guide

These quick start guides are intended to provide developers with simple instructions on how to install *SBC-SMART-BEE* single board computer from very beginning and have it monitoring your local device in few minutes. No advanced installation options are discussed here - just the basics that will work for 95% of users who want to get started. This guide will lead you through the process of configuring, installing, and developing SBC-SMART-BEE. This guide was written to be as clear as possible and to provide only the details necessary to get you up and running. For more in-depth information, links to other chapters will be located where appropriate.

Step1. Plug a working SD card into SD slot

An image pre-installed SD card comes with the evaluation kit. Plug the SD card into SD card slot (CN 16). If developers do not have evaluation kit, please refer to Embedian “SMARC T335X Software Installation Guide” to prepare for a working SD card first.



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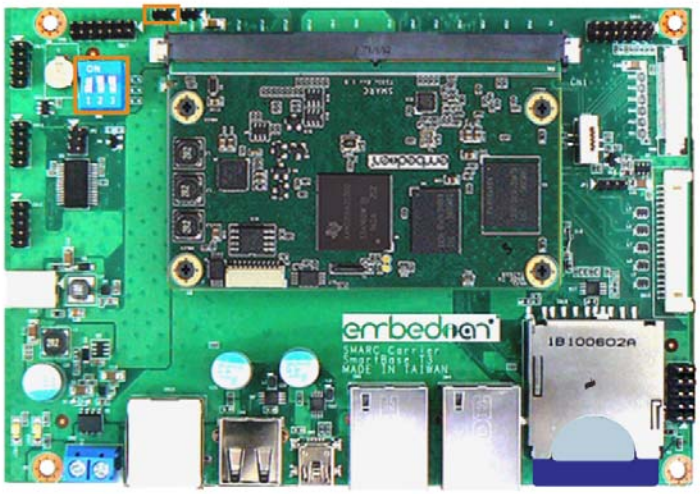
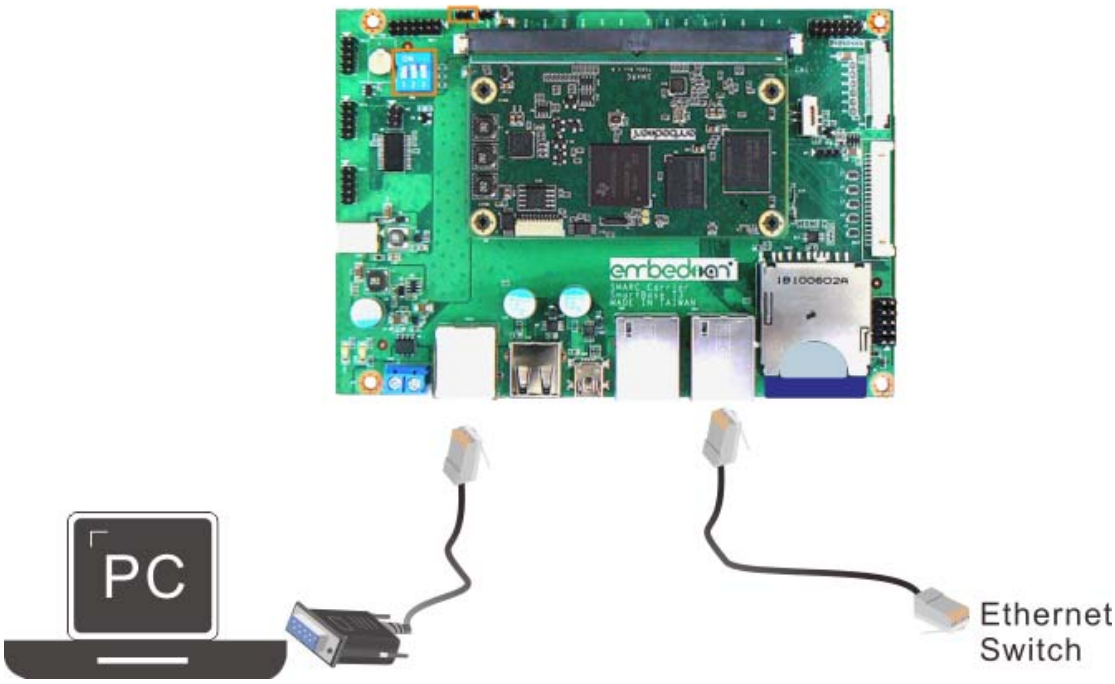
Step2. Check Jumpers and Switches

SW1 switch should be set as SD boot (ON OFF OFF) and make sure that JP3 is not shunt.



Step3. Wired the console and Ethernet cable

Connect the *DB9* to *RJ-45* console debug cable from *CN14* of the device to your PC and the Ethernet cable from *LAN1 (CN4)* of the device to an Ethernet switch.



Open a serial terminal like Putty in your PC. Set the *COM* port as *115200, 8n1.*

Step4. Power 5V to the device

Apply 5V to *CN2* connector of the device. If you see the *LED* light on, that means the wiring is correct. Do not need to worry about the mis-wiring because the device has mis-wiring protection.

You will see the Ubuntu 12.04 booting. The default root password is "*root*" (no quotation) and default Ubuntu user password is "*temppwd*". Default Ethernet is set as *DHCP*. If the root file system is Arago, there is no need for root pass.