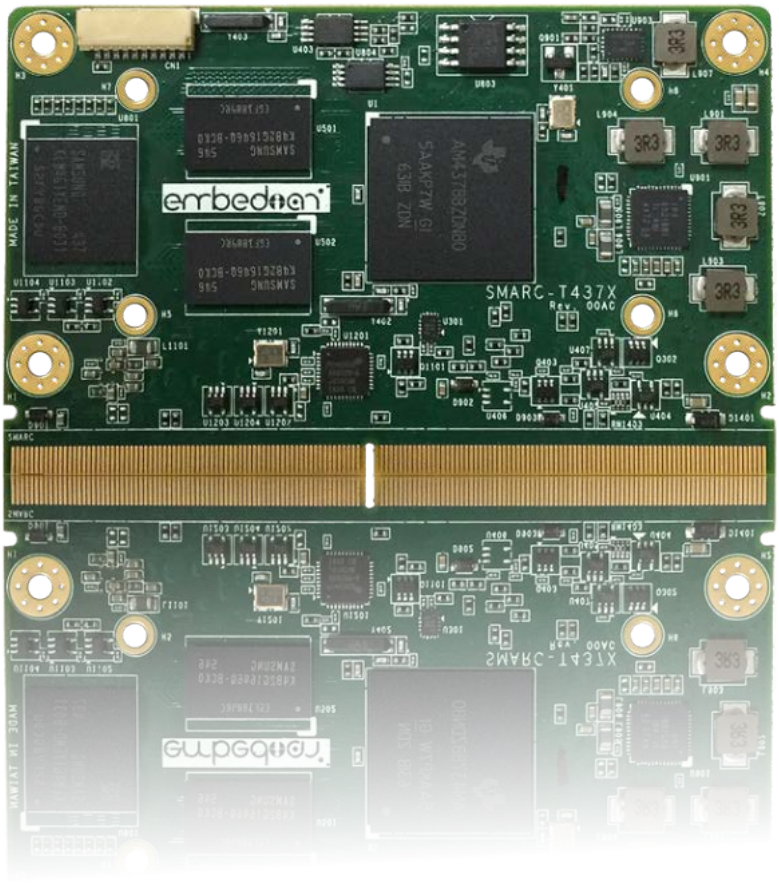
User's Manual

SMARC Computer on Module

TI Sitara AM4378 Cortex A9
24bits Parallel LCD
4 x COM Ports
2 x SDHC, 1 x eMMC
1 x USB Host 2.0, 1 x USB OTG
2 x 10/100/1000M Gigabit Ethernet
2 x CAN Bus, 2 x SPIs, 3 x I2Cs

SMARC-T4378


SMARC-T437X

Revision History

Revision	Date	Changes from Previous Revision
1.0	*2015/12/20*	*Initial Release*

USER INFORMATION

About This Manual

This document provides information about products from *EMBEDIAN, INC.* No warranty of suitability, purpose, or fitness is implied. While every attempt has been made to ensure that the information in this document is accurate, the information contained within is supplied “as-is” and is subject to change without notice.

For the circuits, descriptions and tables indicated, *EMBEDIAN* assumes no responsibility as far as patents or other rights of third parties are concerned.

Copyright Notice

Trademarks

The following lists the trademarks of components used in this board.

- ARM is a registered trademark of ARM Limited.
- Android is a registered trademark of Google
- Linux is a registered trademark of Linus Torvalds.
- WinCE is a registered trademark of Microsoft
- TI is a registered trademark of Texas Instruments
- All other products and trademarks mentioned in this manual are trademarks of their respective owners.

Standards

EMBEDIAN is *ISO 9001:2008* and *ISO14001*-certified manufacturer. *SMARC* is an *SGET* standard for *ARM* computer on module.

Warranty

This *EMBEDIAN* product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, *EMBEDIAN* will at its discretion, decide to repair or replace defective products.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product’s environmental specifications or improper installation or maintenance.

EMBEDIAN will not be responsible for any defects or damages to other products not supplied by EMBEDIAN that are caused by a faulty EMBEDIAN product.

Technical Support

Technicians and engineers from *EMBEDIAN* and/or its subsidiaries and official distributors are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Before contacting *EMBEDIAN* technical support, please consult our Web site for the latest product documentation, utilities, and drivers. If the information does not help solve the problem, contact us by e-mail or telephone.

Table of Contents

Using this Manual

This guide provides information about the Embedian *SMARC-T4378* for TI Sitara embedded *SMARC* core module family.

Conventions used in this guide

This table describes the typographic conventions used in this guide:

This Convention	Is used for
Italic type	Emphasis, new terms, variables, and document titles.
`monospaced type`	Filenames, pathnames, and code examples.

Embedian Information

Document Updates

Please always check the product specific section on the Embedian support website at www.embedian.com/ for the most current revision of this document.

Contact Information

For more information about your Embedian products, or for customer service and technical support, contact Embedian directly.

To contact Embedian by	Use
Mail	Embedian, Inc. 4F-7. 432 Keelung Rd. Sec. 1, Taipei 11051, Taiwan
World Wide Web	http://www.embedian.com/
Telephone	+ 886 2 2722 3291

Additional Resources

Please also refer to the most recent *TI T4378* processor reference manual and

related documentation for additional information.

Introduction

This Chapter gives background information on the *SMARC-T4378*
Section include：

- Features and Functionality
- Module Variants
- Block diagram
- Software Support / Hardware Abstraction
- Module Variant
- Document and Standard References

Chapter 1 Introduction

The *SMARC-T4378* is a highly integrated cost-effective System-on-Module that perfectly fits various embedded and industrial products and segment. It is based on *AM4378* 1GHz ARM® Cortex™-A9 multipurpose processor from *Texas Instruments Sitara*™ family.
The *SMARC-T4378* provides an ideal building block for simple integration with a wide range of products in target markets requiring rich connectivity in a compact, cost effective SoM with low power consumption.
The module connector has 314 edge fingers that mate with a low profile 314 pin 0.5mm pitch right angle connector (this connector is sometimes identified as an 321 pin connector, but 7 pins are lost to the key).
Featuring *Texas Instruments*' System-on-Chip, Embedian's *SMARC-T4378* offers 24-bit Parallel LCD, two Gigabit Ethernet ports, on on-board eMMC flash, two SDHC, USB 2.0, USB OTG, four UARTs support and many peripheral interfaces in a cost effective, low power, miniature package. Embedian's *SMARC-T4378* thin and robust design makes it an ideal building block for reliable system design.

The module is the ideal choice for a broad range of target markets including

- HVAC Building and Control Systems
- IOT Gateway
- Smart Grid and Smart Metering
- HMI/ In-Home Display
- Smart Toll Systems
- Connected Vending Machines
- Display Unit
- General Control System
- And more

Complete and cost-efficient Embedian evaluation kits for Yocto, Ubuntu 14.04, and Android ICS allow immediate and professional embedded product development with dramatically reduced design risk and time-to-market.

1.1 Features and Functionality

The *SMARC-T4378* module is based on the *Sitara AM4378* processor with single core Cortex-A9 from *Texas Instruments*. This processor offers a high number of interfaces. The module has the following features:

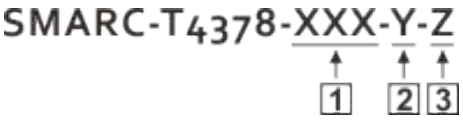
- *SMARC* 1.0 (*3.3V VDDIO*) and 1.1 (*1.8V VDDIO*) compliant in an 82mm

x 50mm form factor.

- Processor: *Texas Instruments AM4378* ARM Cortex-A9 up to 1GHz
- Memory: Onboard 4GB eMMC Flash and 4MB *SPI NOR* Flash
- Onboard 512MB (with 800Mhz CPU variance) or 1GB *DDR3L* (with 1GHz *CPU* variance), 32-bit data bus.
- Networking: 2 x 10/100/1000 Mbps Ethernet
- Display: 24-bit Parallel *LCD* (maximum 24-bit 1400×1050@60)
- Expansion: 2 x *SDHC/SDIO*, 1 x *USB 2.0* Host
- *USB*: 1 x *USB 2.0 Host*, 1 x *USB 2.0 OTG*
- A single 4KB *EEPROM* is provided on I2C0 that holds the board information. This information includes board name, serial number, and revision information.
- Additional Interface:
  - 4 x *UART*s
  - 2 x *SPI*
  - 3 x *I2C*
  - 1 x *I2S*
  - 2 x *CAN Bus*
  - 1 x *PWM*
  - 12 x *GPIOs*
  - *WDT*
- SW Support: L:inux, Yocto, Ubuntu, Android ICS, Windows Embedded Compact 7
- Power Consumption (Typcal)
  - 1.55 Watts
- Thermal:
  - Normal Temperature: 0°C ~ 60°C
  - Industrial Temperature: -40° ~85°C
- Power Supply
- 3V to 5.25V (single 5V is recommended in non-battery operation)
- 3.3V or 1.8V module IO support

1.2 Module Variants

The *SMARC-T4378* module is available with various options based on processors running speed in this family from *TI*, *DDR3L* memory configuration, voltage rail of VDDIO and operating temperature ranges.



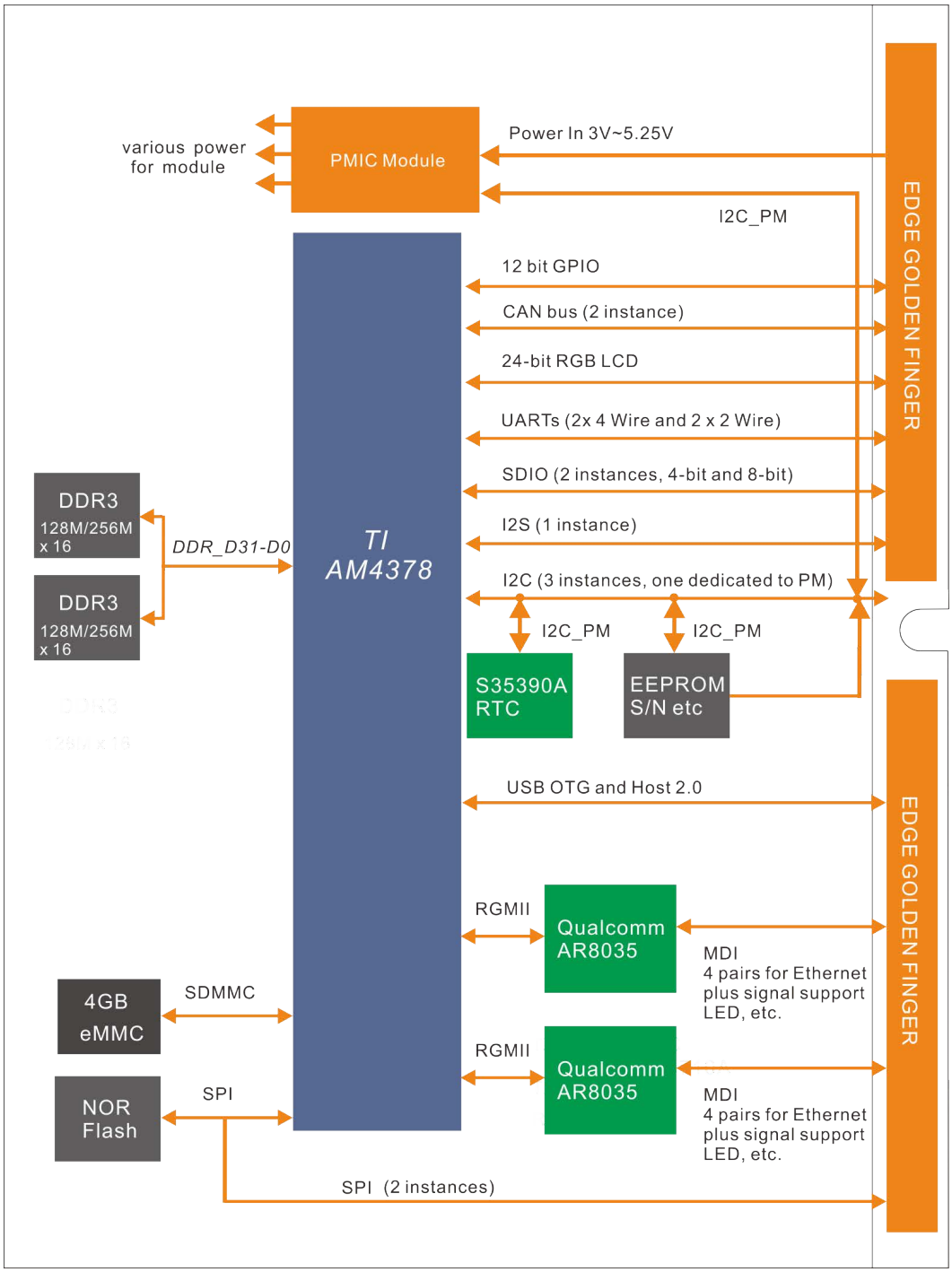
1: "*800*" (CPU running at 800Mhz and using 512MB DDR3 memory)
"*01G*" (CPU running at 1GHz and using 1GB DDR3 memory)
3. "*P*" (if 1.8V VDDIO)
Leave it Blank if 3.3V VDDIO
4. "*I*" (Industrial temperature (-40°C~85°C))
Leave it Blank if normal temperature

For example, *SMARC-T4378-800-P* stands for *SMARC-T4378* module with *Sitara AM4378* processor running at 800Mhz and uses 512MB *DDR3L* in normal temperature and 1.8V *VDDIO* (*SMARC* 1.1).

1.3 Block Diagram

The following diagram illustrates the system organization of the *SMARC-T4378*. Arrows indicate direction of control and not necessarily signal flow.

Figure 1: SMARC-T4378 Block Diagram



Details for this diagram will be explained in the following chapters.

1.4 Software Support / Hardware Abstraction

The Embedian *SMARC-T4378* Module is supported by Embedian BSPs (Board Support Package). The first *SMARC-T4378* BSP targets Linux (Ubuntu 14.04 LTS and Yocto Project) and Android support. BSPs for other operating systems are planned. Check with your Embedian contact for the latest BSPs. This manual goes into a lot of detail on I/O particulars – information is provided on exactly how the various *SMARC* edge fingers tie into the Texas Instrument AM4378 SoC and to other Module hardware. This is provided for reference and context. Almost all of the I/O particulars are covered and abstracted in the BSP and it should generally not be necessary for users to deal with I/O at the register level.

1.5 Document and Standard References

1.5.1. External Industry Standard Documents

- ***eMMC (Embedded Multi-Media Card)*** the eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 *(www.jedec.org)*.
- ***The I2C Specification,*** Version 2.1, January 2000, Philips Semiconductor (now NXP) *(www.nxp.com)*.
- ***I2S Bus Specification,*** Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (*www.nxp.com*).
- ***JTAG (Joint Test Action Group*** defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (*www.ieee.org*).
- ***MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification,*** Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (*www.mxm-sig.org*).
- ***PICMG® EEEP Embedded EEPROM Specification,*** Rev. 1.0, August 2010 (*www.picmg.org*).
- ***SD Specifications Part 1 Physical Layer Simplified Specification,*** Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (*www.sdcard.org*).
- ***SPI Bus –*** “Serial Peripheral Interface” - de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus).
- ***USB Specifications*** (*www.usb.org*).
- ***Serial ATA Revision 3.1,*** July 18, 2011, Gold Revision, © Serial ATA

International Organization *(www.sata-io.org)*

1.5.2. SGET Documents

- ***SMARC_Hardware_Specification_V1p0***, version 1.0, December 20, 2012.
- ***SMARC_Hardware_Specification_V1p1***, version 1.1, May 29, 2014.
- ***Smart Mobility Architecture Design Guide***, version 1.0, July 9, 2013
- ***Smart Mobility Architecture Design Guide***, version 1.1, May 29, 2014

1.5.3. Embedian Documents

The following documents are listed for reference. The Module schematic is not usually available outside of Embedian, without special permission. The other schematics will be available. Contact your Embedian representative for more information. The *SMARC* Evaluation Carrier Board Schematic is particularly useful as an example of the implementation of various interfaces on a Carrier board.

- ***SMARC Evaluation Carrier Board (EVK-STD-CARRIER) Schematic***, PDF and OrCAD format
- ***SMARC Evaluation Carrier Board User's Manual***
- ***SMARC-T4378 User's Manual***

1.5.4. Texas Instrument Documents

- ***AM437x ARM® Cortex™-A9 Processors Technical Reference Manual (Rev. D, SPRUHL7D),*** April 2014 – Revised August 2015
- ***AM437x Sitara™ Processors Silicon Revisions 1.1, 1.2 (Rev. B),*** 10 April 2015

1.5.5. Texas Instrument Development Tools

- ***PINMUXTOOL-V4-CLOUD,*** Browser-based tool access via TI Cloud Tools portal. Automatic solving, high-level requirements entry for configuring device mux settings
- ***PINMUXTOOL_DESKTOP_PREVIOUS,*** Standalone desktop versions of the tool. Device and OS support vary by version

1.5.6. Texas Instrument Software Documents

- ***PROCESSOR-SDK-LINUX-AM437X,*** v02.00.00.00, 07 Oct 2015, Linux v4.1.6

1.5.7. Embedian Software Documents

- ***Embedian Linux BSP for SMARC-T4378 Module***
- ***Embedian Android BSP for SMARC-T4378 Module***
- ***Embedian Linux BSP User's Guide***
- ***Embedian Android BSP User's Guide***

1.5.8. Texas Instrument Design Network

- ***AM437x Evaluation Module,*** *Part# TMDSEVM437X*
- ***AM437x Industrial Development Kit (IDK)***, *Part# TMDSIDK437X*
- ***AM437x Starter Kit,*** *Part# TMDXSK437X*
- ***Nucleus***
- ***QNX***

Specifications

This Chapter provides SMARC-T4378 specifications.
Section include：

- *SMARC-T4378* General Functions
- *SMARC-T4378* Debug
- Mechanical Specifications
- Electrical Specification
- Environment Specification

Chapter 2 Specifications

2.1 SMARC-T4378 General Functions

2.1.1. SMARC-T4378 Feature Set

This section lists the complete feature set supported by the *SMARC-T4378* module.

SMARC Feature Specification	SMARC Specification Maximum Number Possible	SMARC-T4378 Feature Support	SMARC-T4378 Feature Support Instances
LVDS Display Support	1	No	0
Parallel LCD Support	1	Yes	1 (24 bits)[Note1]
HDMI Display Support	1	No	0
CSI Camera Support (Dual and Quad lanes)	2	No	0
Serial Camera Support	2	No	0
USB Interface	3	Yes	2
PCIe Interface	3	No	0
SATA Interface	1	No	0
GbE Interface	1	Yes	2[Note2]
SDIO Interface (4bit)	1	Yes	1 (max. 25MHz)
SDMMC Interface (8bit)	1	Yes	1 (max. 25MHz)
SPI Interface	2	Yes	2
I2S Interface	3	Yes	1
I2C Interface	5	Yes	3
Serial	4	Yes	4
CAN	2	Yes	2

SMARC Feature Specification	SMARC Specification Maximum Number Possible	SMARC-T4378 Feature Support	SMARC-T4378 Feature Support Instances
AFB		Yes	Second Gigabit Ethernet and 4-bit ADC are realized[Note2]
I/O Voltage (1.8V) Level Support		Yes	
I/O Voltage (3.3V) Level Support		Yes	

Note:

1. Parallel *RGB* interface: 1 x 24 bpp (up to 100 MHz per interface e.g 1400x1050 @ 60Hz + 35% blanking)
2. The second Gigabit Ethernet is defined at *AFB* by *SMARC* recommendation.

2.1.2. Form Factor

The *SMARC-T4378* module complies with the *SMARC* General Specification module size requirements in an 82mm x 50mm form factor.

2.1.3. CPU

The SMARC-T4378 implements TI's AM4378 ARM Cortex-A9processor.

- Up to 1GHz ARM Cortex-A9 Microprocessor
- 1 Cache 32 KB Instruction cache (I-Cache) and 32 KB Data cache (D-Cache) with Single-Error Detection (parity)
- 256KB of L2 Cache with Error Correcting - Emulation and Debug Code (ECC)
- 256KB of On-Chip Boot ROM
- 64KB of Dedicated RAM
- SGX530 graphic engine
- Crypto Hardware Accelerators (AES, SHA, RNG, DES and 3DES)
- Programmable Real-Time Unit and Industrial - Dedicated Input Pin (EXT_WAKEUP) for Communication Subsystem (PRU-ICSS)
    - Supports protocols such as EtherCAT®, PROFIBUS, PROFINET, EtherNet/IP™, and more.
- 17mm x 17mm (ZDN) package size, 0.65-mm Ball Pitch
  Optional industrial temperature rage -40°C ~ 85°C

2.1.4. Module Memory

The *SMARC-T4378* module supports different configurations of *DDR3L* memory. The following table shows the available options.

SMARC Variants	*SMARC-T4378-800*	*SMARC-T4378-01G*
512MB DDR3	*Yes*	*No*
1GB DDR3	*No*	*Yes*

Check with your Embedian contact or on the Embedian web site for updated information.

2.1.5. Onboard Storage

The *SMARC-T4378* module supports a 4GB *eMMC* flash memory device, 4MB *SPI NOR* flash and a 32Kb *I2C* serial *EEPROM* on the Module *I2C_PM* (*I2C0*) bus. The device used is an On Semiconductor *24C32* equivalent. The Module serial *EEPROM* is intended to retain Module parameter information, including a module serial number. The Module serial *EEPROM* data structure conforms to the *PICMG® EEEP* Embedded *EEPROM* Specification.). The onboard *4MB SPI NOR* flash is used as *SPI* boot media. The module will always boot up from the onboard *SPI NOR* flash first. The bootloader in *NOR* flash will read the configuration from the boot selection and load kernel zImage from the devices that selected.

2.1.6. Clocks

A 32.768 KHz clock is required for the *AM4378 CPU RTC* (Real Time Clock) and external (S-35390A) RTC.
The TI *AM4378* CPU is provided with a 24 MHz clock using a crystal in normal oscillation mode (On-chip Oscillator).
The *Qualcomm AR8035 PHY* is provided with a 24 MHz clock using a crystal in normal oscillation mode.

2.1.7. Parallel LCD Interface

The Texas Instrument *AM4378* parallel 24 bit *RGB LCD* interface is brought to the Module edge connector. The interface runs at the 3.3V or 1.8V Module I/O voltage depending on the part number that users select. The *SMARC* Module parallel *LCD* pins may be used to drive a traditional parallel *LCD* interface (or they may be used to drive *LVDS* transmitters or other transmitters that accept parallel *LCD* data at the Module *VDD_IO* level).

For parallel displays with very small form factors (think cell phone and digital camera size), the data I/O level is usually 1.8V. For larger displays, the display will likely require a 3.3V data I/O level.

If the *SMARC* modules are with 3.3V *VDD_IO* and parallel displays are with 3.3 V *I/O*, the *SMARC* Parallel LCD data signals may be passed directly to the display, for short cable runs. This voltage swing may be used directly with 3.3V capable Carrier Board LVDS transmitters, such as the TI *SN75LVDS83B*. The 3.3V signaling is suitable for direct connection to a parallel flat panel in most cases. Generally speaking, larger parallel LCD panels are likely to use 3.3V or 5V signaling. If LCD panels use 5V signaling, a set of voltage translators / buffers would be needed on the Carrier.

If the *SMARC* modules are with 1.8V VDD_IO and parallel displays are with 1.8V I/O, the *SMARC* Parallel LCD data signals may be passed directly to the display, for short cable runs. For larger displays with 3.3V I/O level and the *SMARC* modules are 1.8V VDD_IO, a bus transceiver like TI *SN74AVC32T245-ZKE* is required to achieve signal buffering and voltage translation from *VDD_IO* to a 3.3V display. If there is a requirement for a display cable longer than a few inches, it may be a good idea to include the buffer even if the display accepts 1.8V I/O. The voltage swing may be used directly with 1.8V capable Carrier Board LVDS transmitters, such as TI DS90C185.

The following figure shows the parallel LCD block diagram.

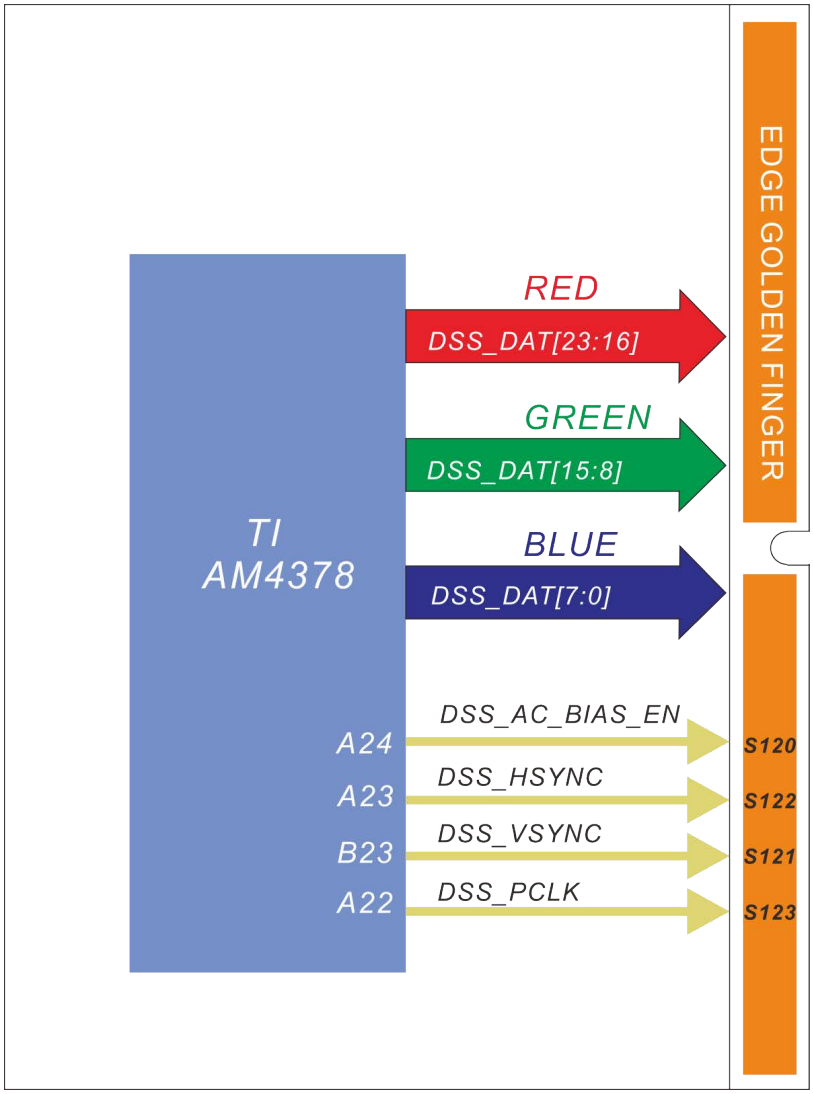


Figure 1: SMARC-T4378 Parallel LCD Diagram

The mapping of the *TI T4378* parallel LCD pins to the *SMARC* edge connector is shown in the table below. Basically, *TI AM4378* processor maps the 18 bits of *R, G, B* for 6 bit color depth to *DSS_DAT[23:18], DSS_DAT[15:10]* and *DSS_DAT[7:2]*. For *AM4378*, the extra bits used for a 24 bit color implementation come out on *TI AM4378 DSS_DAT[17:16], DISP0_DAT[9:8]* and *DISP0_DAT[1:0]*. Since 18-bit configuration and 24-bit configuration use the same MSB signals, we can say 18-bit configuration is higher bits subset 24-bit configuration from the hardware point of view. The *SMARC* golden finger connector has the same convention: Red is *LCD_D[23:16]*; Blue is *LCD_D[15:8]* and Green is *LCD_D[7:0]*. For 24 bit implementations, all bits are used. For 18 bit implementations, in *SMARC*, the least significant bits (Red *LCD_D[17:16]*, Green *LCD_D[9:8]*, Blue *LCD_D[1:0]*) are dropped.

TI AM4378 CPU			SMARC-T4378 Edge Golden Finger		Net Names (Carrier Board)	Color	24-bit Color Map
Ball	Mode	Pin Name	Pin#	Pin Name			
AE17	2	CAM0_HD__ DSS_DATA23	S118	LCD_D23 (MSB)	LCD_D23	RED	R7
AD18	2	CAM0_VD__ DSS_DATA22	S117	LCD_D22	LCD_D22		R6
AC18	2	CAM0_FIELD__ DSS_DATA21	S116	LCD_D21	LCD_D21		R5
AD17	2	CAM0_WEN__ DSS_DATA20	S115	LCD_D20	LCD_D20		R4
AC20	2	CAM0_PCLK__ DSS_DATA19	S114	LCD_D19	LCD_D19		R3
AB19	2	CAM0_DATA8__ DSS_DATA18	S113	LCD_D18	LCD_D18		R2
AA19	2	CAM0_DATA9__ DSS_DATA17	S112	LCD_D17	LCD_D17		R1
AC24	2	CAM1_DATA9__ DSS_DATA16	S111	LCD_D16 (LSB)	LCD_D16		R0
D17	0	DSS_DATA15__ DSS_DATA15	S109	LCD_D15 (MSB)	LCD_D15	GREEN	G7
C17	0	DSS_DATA14__ DSS_DATA14	S108	LCD_D14	LCD_D14		G6
D19	0	DSS_DATA13__ DSS_DATA13	S107	LCD_D13	LCD_D13		G5
C19	0	DSS_DATA12__ DSS_DATA12	S106	LCD_D12	LCD_D12		G4
B18	0	DSS_DATA11__ DSS_DATA11	S105	LCD_D11	LCD_D11		G3
A18	0	DSS_DATA10__ DSS_DATA10	S104	LCD_D10	LCD_D10		G2
B19	0	DSS_DATA9__ DSS_DATA9	S103	LCD_D9	LCD_D9		G1
A19	0	DSS_DATA8__ DSS_DATA8	S102	LCD_D8 (LSB)	LCD_D8		G0

TI AM4378 CPU			SMARC-T4378 Edge Golden Finger		Net Names (Carrier Board)	Color	24-bit Color Map
Ball	Mode	Pin Name	Pin#	Pin Name			
E19	0	DSS_DATA7__ DSS_DATA7	S100	LCD_D7 (MSB)	LCD_D7	BLUE	B7
C20	0	DSS_DATA6__ DSS_DATA6	S99	LCD_D6	LCD_D6		B6
B20	0	DSS_DATA5__ DSS_DATA5	S98	LCD_D5	LCD_D5		B5
A20	0	DSS_DATA4__ DSS_DATA4	S97	LCD_D4	LCD_D4		B4
C21	0	DSS_DATA3__ DSS_DATA3	S96	LCD_D3	LCD_D3		B3
B21	0	DSS_DATA2__ DSS_DATA2	S95	LCD_D2	LCD_D2		B2
A21	0	DSS_DATA1__ DSS_DATA1	S94	LCD_D1	LCD_D1		B1
B22	0	DSS_DATA0__ DSS_DATA0	S93	LCD_D0 (LSB)	LCD_D0		B0

TI AM4378 CPU			SMARC-T4378 Edge Golden Finger		Net Names (Carrier Board)	Color	24-bit Color Map
Ball	Mode	Pin Name	Pin#	Pin Name			
A22	0	DSS_PCLK__ DSS_PCLK	S123	LCD_PCK	LCD_PCK		
A24	0	DSS_AC_BIAS_EN__ DSS_AC_BIAS_EN	S120	LCD_DE	LCD_DE		
A23	0	DSS_HSYNC__ DSS_HSYNC	S122	LCD_HS	LCD_HS		
B23	0	DSS_VSYNC__ DSS_VSYNC	S121	LCD_VS	LCD_VS		
D10	7	GPMC_WEN__ GPIO2[4]	S127	LCD_BKLT_EN	LCD_BKLT_EN		
C10	7	GPMC_BE0N_CLE__ GPIO2[5]	S133	LCD_VDD_EN	LCD_VDD_EN		
AC23	6	GAM1_VD__ EHRPWM0B	S141	LCD_BKLT_PWN	LCD_BKLT_PWM		

To use displays which require fewer bits (e.g. 18 or 16 bit displays), simply do not connect the bottom *n LSBs* for each color, where *n* is the number of signals that are not required for a specific color. For instance, to connect an 18 bit display, *R0, R1, G0, G1, B0 and B1* will remain unused, and *R2, G2* and *B2* become the *LSBs* for this configuration.

2.1.7.1 Parallel LCD Data

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
LCD_D[16:23]	Output	CMOS VDD_IO	8 bit RED color data - 18 bit display implementations leave the two LS bits (D16, D17) not connected
LCD_D[8:15]	Output	CMOS VDD_IO	8 bit GRN color data - 18 bit display implementations leave the two LS bits (D8, D9) not connected
LCD_D[0:7]	Output	CMOS VDD_IO	8 bit BLU color data - 18 bit display implementations leave the two LS bits (D0, D1) not connected
LCD_PCK	Output	CMOS VDD_IO	Pixel clock – display data transitions on the positive clock edge
LCD_DE	Output	CMOS VDD_IO	Display Enable – signal is high during the active display line; low otherwise
LCD_HS	Output	CMOS VDD_IO	Horizontal Sync – high pulse indicates the start of a new horizontal display line
LCD_VS	Output	CMOS VDD_IO	Vertical Synch – high pulse indicates the start of a new display frame

2.1.7.2 Parallel LCD Display Support Signals

The signals in the table below support the Parallel *LCD* interfaces.

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
LCD_VDD_EN	*Output*	*CMOS VDD_IO*	*High enables panel VDD*
LCD_BKLT_EN	*Output*	*CMOS VDD_IO*	*High enables panel backlight*
LCD_BKLT_PWM	*Output*	*CMOS VDD_IO*	*Display backlight PWM control*
I2C_LCD_DAT	*Bi-Dir OD*	*CMOS VDD_IO*	*I2C data – to read LCD display EDID EEPROMs*
I2C_LCD_CK	*Output*	*CMOS VDD_IO*	*I2C clock – to read LCD display EDID EEPROMs*

2.1.8 USB Interface

The Embedian *SMARC-T4378* module supports two *USB* ports (*USB 0:1*). Per the *SMARC* specification, the module supports a *USB* "On-The-Go" (*OTG*) port capable of functioning either as a client or host device, on the *SMARC USB0* port. The *SMARC-T4378* module also supports one additional *USB2.0* host ports, on *SMARC USB1*.

The following figure shows the *USB0* and *USB1* block diagram.

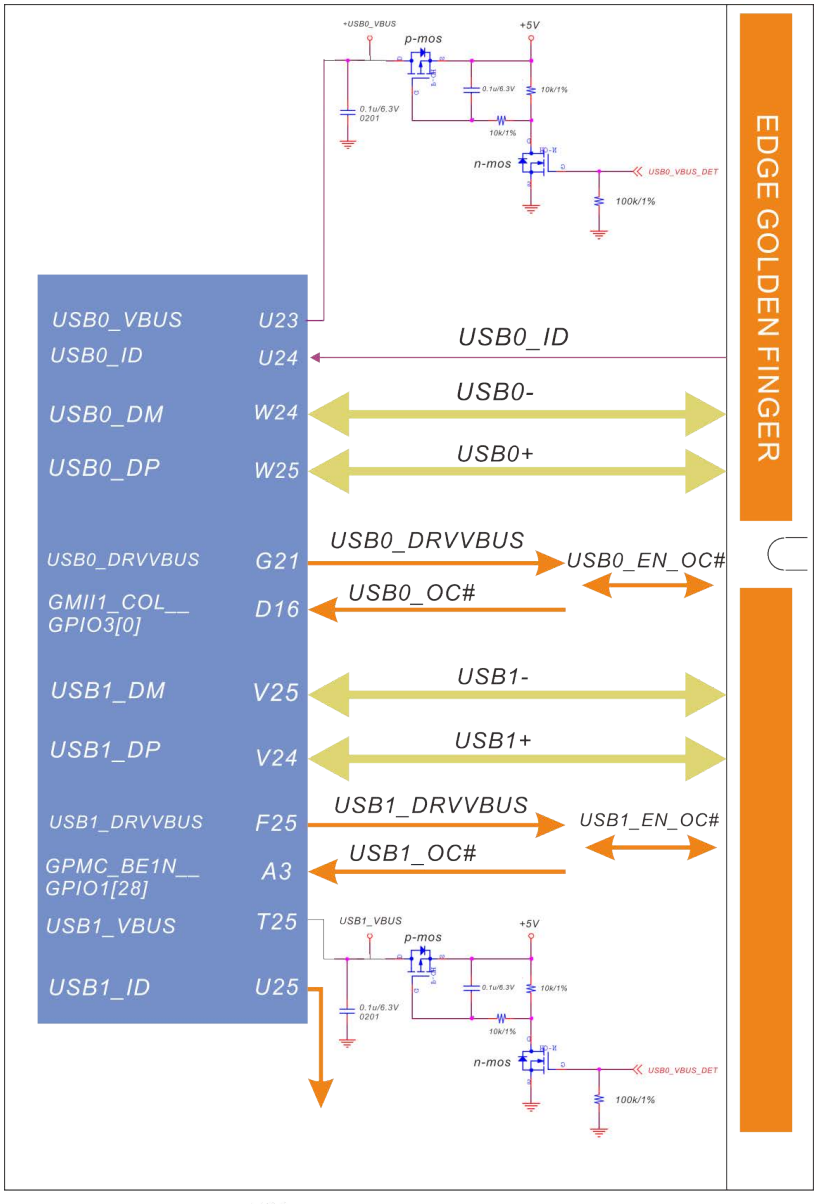


Figure 2. USB0 and USB1 Block Diagram

USB interface signals are exposed on the *SMARC-T4378* edge connector as shown below:

TI AM4378 CPU			SMARC-T4378 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin #	Pin Name		
USB0 Port (OTG)						
W25		USB0_DP	P60	USB0+	USB0+	USB0 port data pair
W24		USB0_DM	P61	USB0-	USB0-	
G21	0	USB0_DRVVBUS__ USB0_DRVVBUS	P62	USB0_EN_OC#	USB0_EN_OC#	USB Port0 power enable/over current indication signal
D16	9	GMII1_COL__ GPIO0[0]				
U23		Turn on USB0_VBUS	P63	USB0_VBUS_DET	USB0_VBUS_DET	USB host power detection, when this port is used as a device.
U24	0	USB0_ID__ USB0_ID	P64	USB0_OTG_ID	USB0_OTG_ID	USB OTG ID input, active high
USB1 Port (Host 2.0)						
V24		USB1_DP	P65	USB1+	USB1+	USB1 port data pair
V25		USB1_DM	P66	USB1-	USB1-	
F25	0	USB1_DRVVBUS__ USB1_DRVVBUS	P67	USB1_EN_OC#	USB1_EN_OC#	USB Port0 power enable/over current indication signal
A3	7	GPMC_BE1N__ GPIO1[28]				

2.1.8.1 USB0 Signals

The table below shows the *USB0* related signals.

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
USB0+ *USB0-*	*Bi-Dir*	*USB*	*Differential USB0 Data Pair*
USB0_EN_OC#	*Bi-Dir* *OD*	*CMOS* *3.3V*	*Pulled low by Module OD driver to disable USB0 power.* *Pulled low by Carrier OD driver to indicate over-current situation.* *A 10k pull-up is present on the Module to a 3.3V rail. The pull-up rail may be switched off to conserve power if the USB port is not in use. Further details may be found in Section 2.1.12.3 USBx_EN_OC# Discussion below.*
USB0_VBUS_DET	*Input*	*USB VBUS 5V*	*USB host power detection, when this port is used as a device.*
USB0_OTG_ID	*Input*	*CMOS* *3.3V*	*USB OTG ID input, active high.*

2.1.8.2 USB1 Signals

USB1 port is a *USB 2.0* host port. The table below shows the USB1 related signals.

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
USB1+ *USB1-*	*Bi-Dir*	*USB*	*Differential USB1 Data Pair*
USB1_EN_OC#	*Bi-Dir* *OD*	*CMOS* *3.3V*	*Pulled low by Module OD driver to disable USB0 power.* *Pulled low by Carrier OD driver to indicate over-current situation.* *A 10k pull-up is present on the Module to a 3.3V rail. The pull-up rail may be switched off to conserve power if the USB port is not in use. Further details may be found in Section 2.1.12.3 USBx_EN_OC# Discussion below.*

2.1.8.3 USBx_EN_OC# Discussion

The Module *USBx_EN_OC#* pins (where '*x*' is *0* or *1* for use with *USB0* or *USB1*) are multi-function Module pins, with a 10k pull-up to a 3.3V rail on the Module, an *OD* driver on the Module, and, if the *OC#* (over-current) monitoring function is implemented on the Carrier, an OD driver on the Carrier. The use is as follows:

1) On the Carrier board, for external plug-in *USB* peripherals (*USB* memory sticks, cameras, keyboards, mice, etc.) *USB* power distribution is typically handled by *USB* power switches such as the Texas Instruments *TPS2052B* or the *Micrel MIC2026-1* or similar devices. The Carrier implementation is more straightforward if the Carrier USB power switches have active-high power enables and active low open drain *OC#* outputs (as the TI and Micrel devices referenced do). The USB power switch Enable and OC# pins for a given USB channel are tied together on the Carrier. The USB power switch enable pin must function with a low input current. The TI and Micrel devices referenced above require 1 microampere or less, at a 3.3V enable voltage level.
2) The Module drives *USBx_EN_OC#* low to disable the power delivery to the *USBx* device.
3) The Module floats *USBx_EN_OC#* to enable power delivery. The line is

pulled to 3.3V by the Module pull-up, enabling the Carrier board *USB* power switch.

4) If there is a USB over-current condition, the Carrier board *USB* power switch drives the *USBx_EN_OC#* line low. This removes the over-current condition (by disabling the USB switch enable input), and allows Module software to detect the over-current condition.
5) The Module software should look for a falling edge interrupt on *USBx_EN_OC#*, while the port is enabled, to detect the *OC#* condition. The *OC#* condition will not last long, as the USB power switch is disabled when the switch IC detects the OC# condition.
6) If the USB power to the port is disabled (*USBx_EN_OC#* is driven low by the Module) then the Module software is aware that the port is disabled, and the low input value on the port does not indicate an over-current condition (because the port power is disabled).

Carrier Board USB peripherals that are not removable often do not make use of *USB* power switches with current limiting and over-current detection. It is usually deemed un-necessary for non-removable devices. In these cases, the *USBx_EN_OC#* pins may be left unused, or they may be used as *USBx* power enables, without making use of the over-current detect Module input feature.

The *SMARC-T4378* Module *USB* power enable and over current indication logic implementation is shown in the following block diagram. There are 10k pull-up resistors on the Module on the *SMARC USBx_EN_OC#* lines. Outputs driving the *USBx_EN_OC#* lines are open-drain. The Carrier board USB power switch, if present, is enabled by *USBx_EN_OC#* after a device connection is detected on the DP/DM lines.

The Enable pin on the Carrier board *USB* power switch must be active – high and the Over-Current pin (*OC#*) must be open drain, active low (these are commonly available). No pull-up is required on the *USB* power switch Enable or *OC#* line on carrier board; they are tied together on the Carrier and fed to the Module *USBx_EN_OC#* pin.

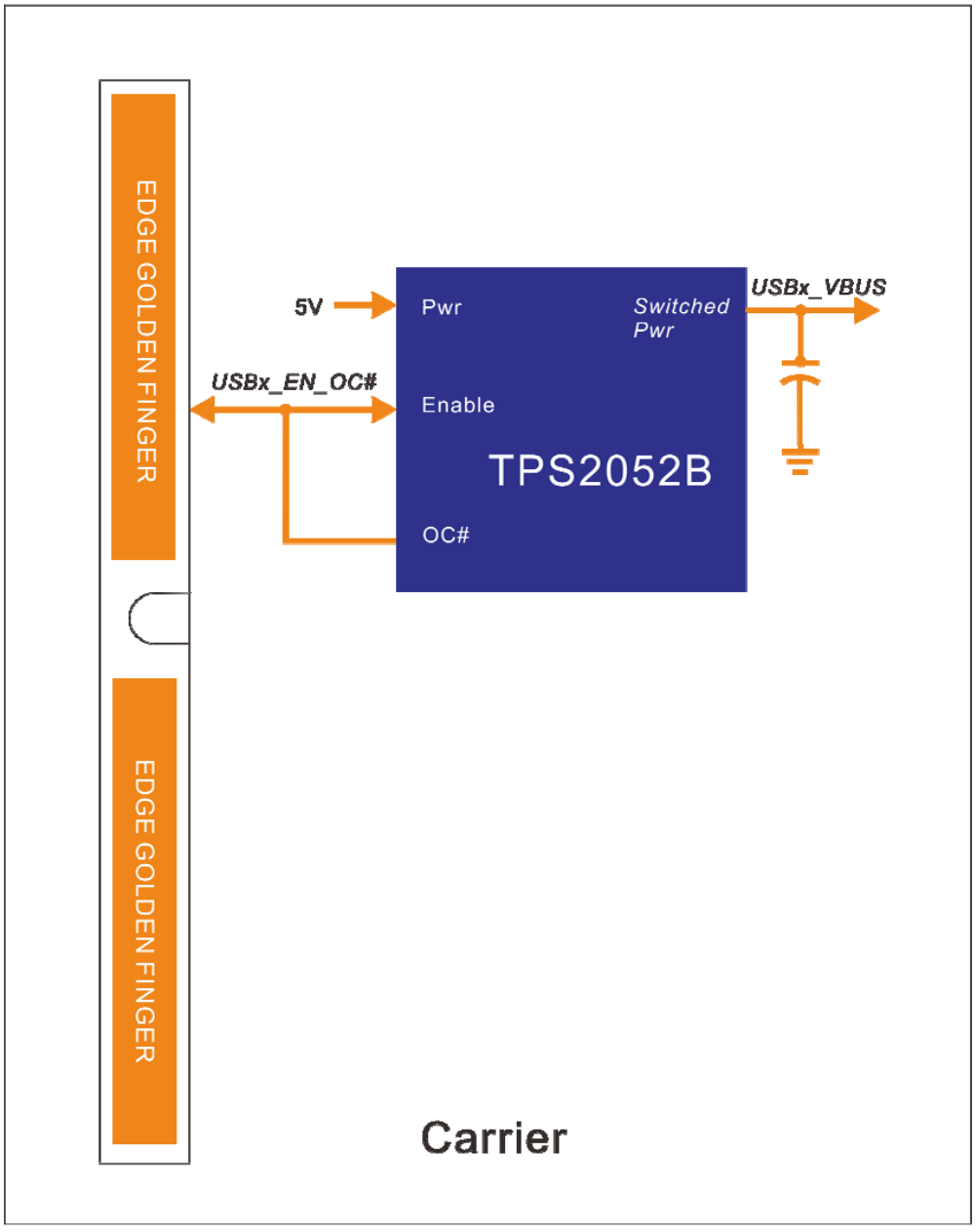


Figure 3. USB Power Distribution Implementation on Carrier

2.1.9. Gigabit Ethernet Controller (10/100/1000Mbps) Interface

The *SMARC-T4378* module supports ***two*** Gigabit Ethernet (10/100/1000Mbps) interfaces that supports IEEE 1588v2 Precision Time Protocol (PTP). The Gigabit Ethernet controller interfaces are accomplished by using the low-power Qualcomm Atheros *AR8035* physical layer (PHY) transceiver with variable I/O voltage that is compliant with the IEEE 802.3-2005 standards. The *AR8035* supports communication with an Ethernet MAC via a standard *RGMII* interface.
Each of the Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from *GBE0_MDI0*± to *GBE0_MDI3*± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT *RJ45* connector with integrated or external isolation magnetics on the carrier board.

This is diagrammed below.

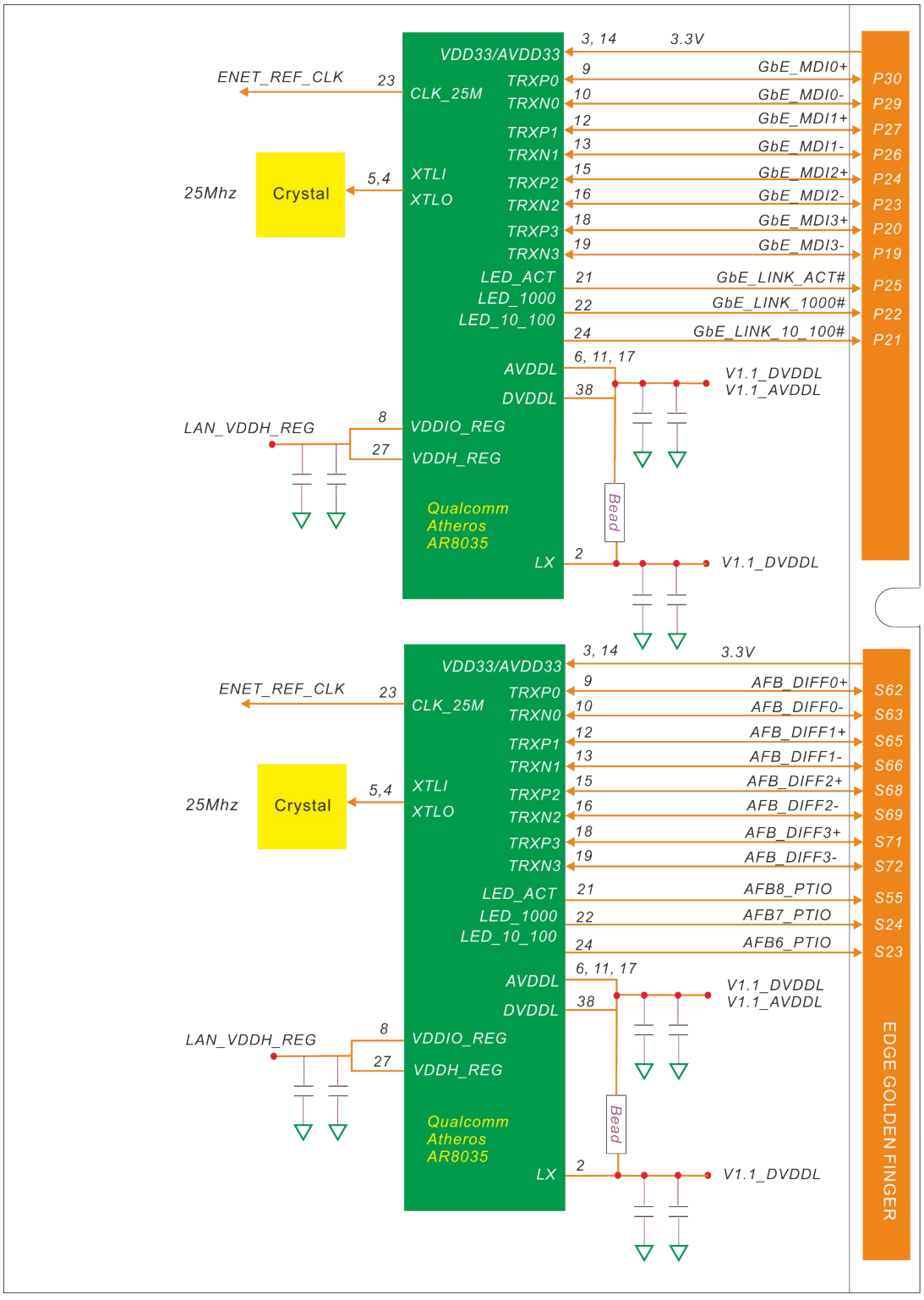


Figure 4: Gigabit Ethernet Connection from Qualcomm Atheros AR8035 to Golden Finger Connector

2.1.9.1. Path of Gigabit LAN1

AM4378 processor and the first Qualcomm Atheros *AR8035* implementation is shown in the following table:

TI AM4378 CPU			Qualcomm AR8035		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
Gigabit LAN 1						
A17	0	MDIO_DATA__ MDIO_DATA	39	MDIO	ENET_MDIO	Serial Management Interface data input/output
B17	0	MDIO_CLK__ MDIO_CLK	40	MDC	ENET_MDC	Serial Management Interface clock
F17	2	GMII1_RXD0__ RGMII1_RD0	29	RXD0	RMII_RD0	Bit 0 of the 4 data bits that are sent by the transceiver on the receive path.
B16	2	GMII1_RXD1__ RGMII1_RD1	28	RXD1	RMII_RD1	Bit 1 of the 4 data bits that are sent by the transceiver on the receive path.
E16	2	GMII1_RXD2__ RGMII1_RD2	26	RXD2	RMII1_RD2	Bit 2 of the 4 data bits that are sent by the transceiver on the receive path.
C14	2	GMII1_RXD3__ RGMI1I_RD3	25	RXD3	RGMII_RD3	Bit 3 of the 4 data bits that are sent by the transceiver on the receive path.
D13	2	GMII1_RXCLK__ RGMII1_RCLK	31	RX_CLK	RGMII_RXC	Reference clock
A15	2	GMII1_RXDV__ RGMII1_RCTL	30	RX_DV	RGMII_RX_CTL	Indicates both the receive data valid (RXDV) and receive error (RXER) functions per the RGMII specification.

TI AM4378 CPU			Qualcomm AR8035		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
Gigabit LAN 1						
A13	2	GMII1_TXEN__ RGMII1_TCTL	32	TX_EN	RGMII_TX_CTL	Indicates that valid transmission data is present on TXD[3:0].
B15	2	GMII1_TXD0__ RGMII1_TD0	34	TXD0	RGMII_TD0	The MAC transmits data to the transceiver using this signal.
A14	2	GMII1_TXD1__ RGMII1_TD1	35	TXD1	RGMII_TD1	The MAC transmits data to the transceiver using this signal.
C13	2	GMII1_TXD2__ RGMII1_TD2	36	TXD2	RGMII_TD2	The MAC transmits data to the transceiver using this signal.
C16	2	GMII1_TXD3__ RGMII1_TD3	37	TXD3	RGMII_TD3	The MAC transmits data to the transceiver using this signal.
D14	2	GMII1_TXCLK__ RGMII1_TCLK	33	GTX_CLK	RGMII_TXC	Used to latch data from the MAC into the PHY. 1000BASE-T: 125MHz 100BASE-TX: 25MHz 10BASE-T: 2.5MHz

The path from *AR8035* to the golden finger edge connector is show in the following table.

Qualcomm AR8035		Golden Finger Edge Connector		Net Names	Note
Pin	Pin Name	Pin#	Pin Name		
AR8035 PHY 1					
9	TRXP0	P30	GbE_MDI0+	GBE_MDI0+	Differential Transmit/Receive Positive Channel 0
10	TRXN0	P29	GbE_MDI0-	GBE_MDI0-	Differential Transmit/Receive Negative Channel 0
		P28	GbE_CTREF	GBE_CTREF	Center tap reference voltage
12	TRXP1	P27	GbE_MDI1+	GBE_MDI1+	Differential Transmit/Receive Positive Channel 1
13	TRXN1	P26	GbE_MDI1-	GBE_MDI1-	Differential Transmit/Receive Negative Channel 1
15	TRXP2	P24	GbE_MDI2+	GBE_MDI2+	Differential Transmit/Receive Positive Channel 2
16	TRXN2	P23	GbE_MDI2-	GBE_MDI2-	Differential Transmit/Receive Negative Channel 2
18	TRXP3	P20	GbE_MDI3+	GBE_MDI3+	Differential Transmit/Receive Positive Channel 3
19	TRXN3	P19	GbE_MDI3-	GBE_MDI3-	Differential Transmit/Receive Negative Channel 3

Qualcomm AR8035		Golden Finger Edge Connector		Net Names	Note
Pin	Pin Name	Pin#	Pin Name		
AR8035 PHY 1					
21	LED_ACT	P25	GbE_LINK_ACT#	GBE_LINK_ACT#	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity Could be able to sink 24mA or more Carrier LED current
24	LED_10_100	P21	GbE_LINK100#	GBE_LINK100#	Link Speed Indication LED for 100Mbps Could be able to sink 24mA or more Carrier LED current
22	LED_1000	P22	GbE_LINK1000#	GBE_LINK1000#	Link Speed Indication LED for 1000Mbps Could be able to sink 24mA or more Carrier LED current

2.1.9.2. Path of Gigabit LAN2

AM4378 processor and the second Qualcomm Atheros *AR8035* implementation is shown in the following table:

TI AM4378 CPU			Qualcomm AR8035		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
Gigabit LAN 2						
A17	0	MDIO_DATA__ MDIO_DATA	39	MDIO	ENET_MDIO	Serial Management Interface data input/output
B17	0	MDIO_CLK__ MDIO_CLK	40	MDC	ENET_MDC	Serial Management Interface clock
D8	2	GPMC_A11__ RGMII2_RD0	29	RXD0	RMII_RD0	Bit 0 of the 4 data bits that are sent by the transceiver on the receive path.
G8	2	GPMC_A10__ RGMII2_RD1	28	RXD1	RMII_RD1	Bit 1 of the 4 data bits that are sent by the transceiver on the receive path.
B4	2	GPMC_A9__ RGMII2_RD2	26	RXD2	RMII1_RD2	Bit 2 of the 4 data bits that are sent by the transceiver on the receive path.
F7	2	GPMC_A8__ RGMII2_RD3	25	RXD3	RGMII_RD3	Bit 3 of the 4 data bits that are sent by the transceiver on the receive path.
F6	2	GPMC_A7__ RGMII2_RCLK	31	RX_CLK	RGMII_RXC	Reference clock
C5	2	GPMC_A1__ RGMII2_RCTL	30	RX_DV	RGMII_RX_CTL	Indicates both the receive data valid (RXDV) and receive error (RXER) functions per the RGMII specification.

TI AM4378 CPU			Qualcomm AR8035		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
Gigabit LAN 2						
C3	2	GPMC_A0__ RGMII2_TCTL	32	TX_EN	RGMII_TX_CTL	Indicates that valid transmission data is present on TXD[3:0].
E7	2	GPMC_A5__ RGMII2_TD0	34	TXD0	RGMII_TD0	The MAC transmits data to the transceiver using this signal.
D7	2	GPMC_A4__ RGMII2_TD1	35	TXD1	RGMII_TD1	The MAC transmits data to the transceiver using this signal.
A4	2	GPMC_A3__ RGMII2_TD2	36	TXD2	RGMII_TD2	The MAC transmits data to the transceiver using this signal.
C6	2	GPMC_A2__ RGMII2_TD3	37	TXD3	RGMII_TD3	The MAC transmits data to the transceiver using this signal.
E8	2	GPMC_A6__ RGMII2_TCLK	33	GTX_CLK	RGMII_TXC	Used to latch data from the MAC into the PHY. 1000BASE-T: 125MHz 100BASE-TX: 25MHz 10BASE-T: 2.5MHz

The path from the second *AR8035* to the golden finger edge connector is show in the following table.

Qualcomm AR8035		Golden Finger Edge Connector		Net Names	Note
Pin	Pin Name	Pin#	Pin Name		
AR8035 PHY 2					
9	TRXP0	S62	AFB_DIFF0+	GBE1_MDI0+	Differential Transmit/Receive Positive Channel 0
10	TRXN0	S63	AFB_DIFF0-	GBE1_MDI0-	Differential Transmit/Receive Negative Channel 0
		S17	AFB0_OUT	GBE1_CTREF	Center tap reference voltage
12	TRXP1	S65	AFB_DIFF1+	GBE1_MDI1+	Differential Transmit/Receive Positive Channel 1
13	TRXN1	S66	AFB_DIFF1-	GBE1_MDI1-	Differential Transmit/Receive Negative Channel 1
15	TRXP2	S68	AFB_DIFF2+	GBE1_MDI2+	Differential Transmit/Receive Positive Channel 2
16	TRXN2	S69	AFB_DIFF2-	GBE1_MDI2-	Differential Transmit/Receive Negative Channel 2
18	TRXP3	S71	AFB_DIFF3+	GBE1_MDI3+	Differential Transmit/Receive Positive Channel 3
19	TRXN3	S72	AFB_DIFF3-	GBE1_MDI3-	Differential Transmit/Receive Negative Channel 3

Qualcomm AR8035		Golden Finger Edge Connector		Net Names	Note
Pin	Pin Name	Pin#	Pin Name		
AR8035 PHY 2					
21	LED_ACT	S55	AFB8_PTIO	GBE1_LINK_ACT#	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity Could be able to sink 24mA or more Carrier LED current
24	LED_10_100	S23	AFB6_PTIO	GBE1_LINK100#	Link Speed Indication LED for 100Mbps Could be able to sink 24mA or more Carrier LED current
22	LED_1000	S24	AFB7_PTIO	GBE1_LINK1000#	Link Speed Indication LED for 1000Mbps Could be able to sink 24mA or more Carrier LED current

2.1.9.3. Gigabit LAN Signals

The table below shows the Gigabit LAN related signals.

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
GBE(1)_MDI0+ GBE(1)_MDI0-	Bi-Dir	GBE_MDI	Bi-directional transmit/receive pair 0 to magnetics (Media Dependent Interface)
GBE(1)_MDI1+ GBE(1)_MDI1-	Bi-Dir	GBE_MDI	Bi-directional transmit/receive pair 1 to magnetics (Media Dependent Interface)
GBE(1)_MDI2+ GBE(1)_MDI2-	Bi-Dir	GBE_MDI	Bi-directional transmit/receive pair 2 to magnetics (Media Dependent Interface)
GBE(1)_MDI3+ GBE(1)_MDI3-	Bi-Dir	GBE_MDI	Bi-directional transmit/receive pair 3 to magnetics (Media Dependent Interface)
GBE(1)_100#	Output OD	CMOS 3.3V	Link Speed Indication LED for 100Mbps Could be able to sink 24mA or more Carrier LED current
GBE(1)_1000#	Output OD	CMOS 3.3V	Link Speed Indication LED for 1000Mbps Could be able to sink 24mA or more Carrier LED current
GBE(1)_LINK_ACK#	Output OD	CMOS 3.3V	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity Could be able to sink 24mA or more Carrier LED current
GBE(1)_CTREF	Output	Reference Voltage	Center-Tap reference voltage for GBE0 Carrier board Ethernet magnetic (not required by the Module GBE PHY)

2.1.9.4. Suggested Magnetics

Listed below are suggested magnetics.

For normal temperature (0°C ~70°C) products.

Vendor	P/N	Package	Cores	Temp	Configuration
Halo	HFJ11-1G02E	Integrated RJ45	8	0°C~70°C	HP Auto-MDIX
UDE	RB1-BA6BT9WA	Integrated RJ45	8	-40°C~85°C	HP Auto-MDIX
Halo	TG1G-S002NZRL	24-pin SOIC-W	8	0°C~70°C	HP Auto-MDIX

For industrial temperature (-40°C ~85°C) products.

Vendor	P/N	Package	Cores	Temp	Configuration
UDE	RB1-BA6BT9WA	Integrated RJ45	8	-40°C~85°C	HP Auto-MDIX
Halo	TG1G-E012NZRL	24-pin SOIC-W	8	-40°C~85°C	HP Auto-MDIX

2.1.10. SD/SDMMC Interface

SMARC-T4378 is configured to support three *MMC* controllers. One is used for internal 8-bit *eMMC* support, and the other two could be used for external SDHC/SDIO interfaces. The *SMARC-T4378* module supports two 4bit *SDIO* interface, per the *SMARC* specification. From the definition of *SMARC* specification, one will be interfaced to *SD/SDHC* card or device, and the other could be interfaced to external *eMMC* flash. However, they can be used as two *SD/SDHC* interfaces or external *eMMC* flash. The *SDIO* interface uses 3.3V signaling, per the *SMARC* spec and for compatibility with commonly available *SDIO* cards.

The following figure shows the SDIO/eMMC block diagram.

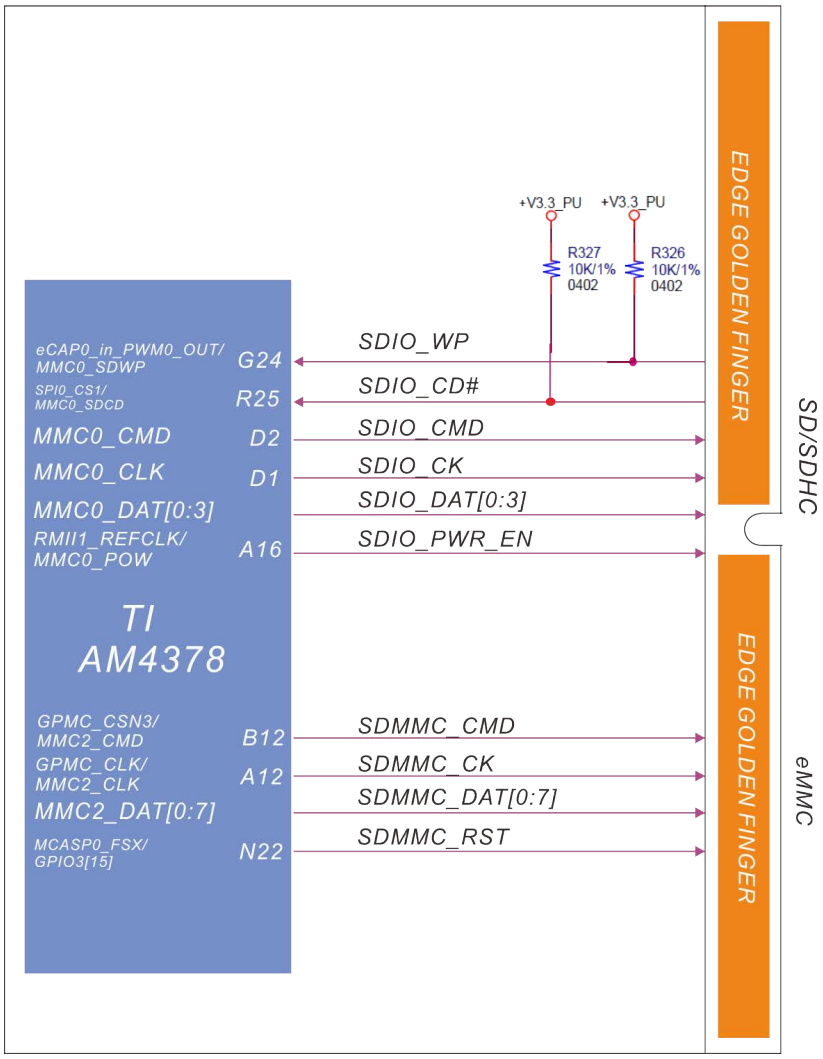


Figure 5. SD/SDIO/eMMC Interface Block Diagram

SDIO and *SDMMC* interface signals are exposed on the *SMARC* golden finger edge connector as shown below:

TI AM4378 CPU			SMARC-T4378 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
SD/SDIO						
C1	0	MMC0_DAT0__ MMC0_DAT0	P39	SDIO_D0	SDIO_D0	SDIO Data 0
C2	0	MMC0_DAT1__ MMC0_DAT1	P40	SDIO_D1	SDIO_D1	SDIO Data 1
B2	0	MMC0_DAT2__ MMC0_DAT2	P41	SDIO_D2	SDIO_D2	SDIO Data 2
B1	0	MMC0_DAT3__ MMC0_DAT3	P42	SDIO_D3	SDIO_D3	SDIO Data 3
G24	5	eCAP0_in_PWM0_OUT__ MMC0_SDWP	P33	SDIO_WP	SDIO_WP	SDIO write protect signal
D2	0	MMC0_CMD__ MMC0_CMD	P34	SDIO_CMD	SDIO_CMD	SDIO Command signal
R25	5	SPI0_CS1__ MMC0_SDCD	P35	SDIO_CD#	SDIO_CD#	SDIO card detect
D1	0	MMC0_CLK__ MMC0_CLK	P36	SDIO_CK	SDIO_CK	SDIO Clock Signal
A16	5	RMII1_REFCLK__ MMC0_POW	P37	SDIO_PWR_EN	SDIO_PWREN	SD card power enable

TI AM4378 CPU			SMARC-T4378 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
SDMMC						
E11	3	GPMC_AD12__ MMC2_DAT0	S26	SDMMC_D0	SDMMC_D0	8-bit eMMC Data 0
C11	3	GPMC_AD13__ MMC2_DAT1	S27	SDMMC_D1	SDMMC_D1	8-bit eMMC Data 1
B11	3	GPMC_AD14__ MMC2_DAT2	S28	SDMMC_D2	SDMMC_D2	8-bit eMMC Data 2
A11	3	GPMC_AD15__ MMC2_DAT3	S29	SDMMC_D3	SDMMC_D3	8-bit eMMC Data 3
B10	3	GPMC_AD8__ MMC2_DAT4	S30	SDMMC_D4	SDMMC_D4	8-bit eMMC Data 4
A10	3	GPMC_AD9__ MMC2_DAT5	S31	SDMMC_D5	SDMMC_D5	8-bit eMMC Data 5
F11	3	GPMC_AD10__ MMC2_DAT6	S32	SDMMC_D6	SDMMC_D6	8-bit eMMC Data 6
D11	3	GPMC_AD11__ MMC2_DAT7	S33	SDMMC_D7	SDMMC_D7	8-bit eMMC Data 7
A12	3	GPMC_CLK__ MMC2_CLK	S35	SDMMC_CK	SDMMC_CK	SDMMC Clock Signal
B12	3	GPMC_CSN3__ MMC2_CMD	S36	SDMMC_CMD	SDMMC_CMD	SDMMC Command signal
N22	7	MCASP0_FSX__ GPIO3[15]	S37	SDMMC_RST#	SDMMC_RST#	Reset signal to eMMC device

Note:

1. The *SDIO* card power should be switched on the Carrier board and the *SDIO* lines should be *ESD* protected. The *SMARC* Evaluation Carrier schematic is useful as an implementation reference.
2. **If *SD* boot up function is required, the pull-up resistor to 3.3V of *SDIO_PWR_EN* # on carrier board should be 4.7k or less.**
3. *SDIO_WP* and *SDIO_CD#* are 10k pull up to 3.3V on module.
4. If users would like to implement *SDMMC* interface as *SD/SDIO,* you can use other *GPIO*s for *WP* and *CD#* signals and use 10k pull-up resistors to 3.3V.

2.1.10.1. SDIO Card (4 bit) Interface

The Carrier *SDIO* Card can be selected as the Boot Device (See section 4.3).

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
SDIO_D[0:3]	*Bi-Dir*	*CMOS 3.3V*	*4 bit data path*
SDIO_CMD	*Bi-Dir*	*CMOS 3.3V*	*Command Line*
SDIO_CK	*Output*	*CMOS 3.3V*	*Clock*
SDIO_WP	*Input*	*CMOS 3.3V*	*Write Protect*
SDIO_CD#	*Input*	*CMOS 3.3V*	*Card Detect*
SDIO_PWR_EN	*Output*	*CMOS 3.3V*	*SD Card Power Enable*

Note:

SD Cards are not typically available with a 1.8V I/O voltage. The Module *SD* Card I/O level is specified as 3.3V and not *CMOS VDD_IO*.

2.1.10.2. eMMC (8 bit) Interface

The *SMARC* Module pin definition allows for an 8 bit *eMMC* interface on carrier board. There is an on-module 8 bit *4GB eMMC*. Both the on-module and on-carrier *eMMC* can be selected as the Boot Device – see Section 4.3 Boot Select.

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
SDMMC_D[0:7]	*Bi-Dir*	*CMOS VDDIO*	*8 bit data path*
SDMMC_CMD	*Bi-Dir*	*CMOS VDDIO*	*Command Line*
SDMMC_CK	*Output*	*CMOS VDDIO*	*Clock*
SDMMC_RST	*Output*	*CMOS VDDIO*	*Write Protect*

2.1.11. SPI Interface

The *SMARC-T4378* module supports three *TI AM4378 SPI* interfaces. One of them is solely used by the on-module SPI flash and the rest two ones are available off-Module for general purpose use. Each *SPI* channel has two chip-selects that can connect two SPI slave devices on each channel. Every device will share the "*SPI_DIN*", "*SPI_DO*" and "*SPI_CK*" pins, but each device will have its own chip select pin. The chip select signal is a low active signal.
The 4MB onboard *SPI NOR* flash uses the *SPI0* interface. User available SPI interfaces are *SPI2* and *SPI4*. The onboard *SPI NOR* flas h on *SMARC-T4378* is used as first stage bootloader device. The module will always boot up from *SPI NOR* flash, and the u-boot (first stage bootloader) in NOR flash will read the *BOOT_SEL* configuration and load the kernel zImage from the user assigned Boot Device.

The *SPI* interface is diagramed below.

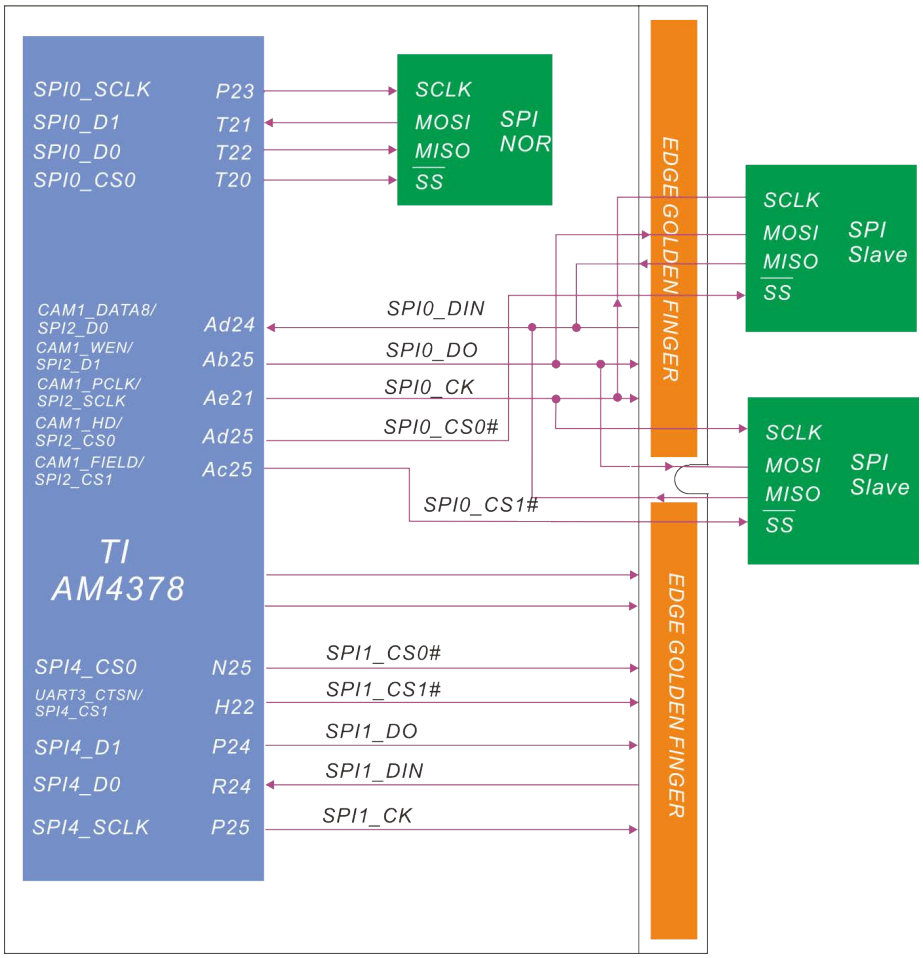


Figure 6: SPI Serial Flash Schematics

SPI interface signals are exposed on the *SMARC* golden finger edge connector as shown below:

TI AM4378 CPU			SMARC-T4378 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
SPI NOR Flash						
T20	0	SPI0_CS0__ SPI0_CS0				SPI_NOR Master Chip Select 0 output, reserve for onboard NOR flash
P23	0	SPI0_SCLK__ SPI0_SCLK				SPI_NOR Master Clock output
T22	0	SPI0_D0__ SPI0_D0				SPI_NOR Master Data input (input to CPU, output from SPI device)
T21	0	SPI0_D1__ SPI0_D1				SPI_NOR Master Data output (output from CPU, input to SPI device)

TI AM4378 CPU			SMARC-T4378 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
SPI0 Port						
AD25	4	CAM1_HD__ SPI2_CS0	P43	SPI0_CS0#	SPI0_CS0#	SPI0 Master Chip Select 0 output
AC25	4	CAM1_FIELD__ SPI2_CS1	P31	SPI0_CS1#	SPI0_CS1#	SPI0 Master Chip Select 1 output
AE21	4	CAM1_PCLK__ SPI2_SCLK	P44	SPI0_CK	SPI0_SCLK	SPI0 Master Clock output
AD24	4	CAM1_DATA8__ SPI2_D0	P45	SPI0_DIN	SPI0_DIN	SPI0 Master Data input (input to CPU, output from SPI device)
AB25	4	CAM1_WEN__ SPI2_D1	P46	SPI0_DO	SPI0_DO	SPI0 Master Data output (output from CPU, input to SPI device)
SPI1 Port						
N25	0	SPI4_CS0__ SPI4_CS0	P54	SPI1_CS0#	SPI1_CS0#	SPI1 Master Chip Select 0 output
H22	2	UART3_CTSN__ SPI4_CS1	P55	SPI1_CS1#	SPI1_CS1#	SPI1 Master Chip Select 1 output
P25	0	SPI4_SCLK__ SPI4_SCLK	P56	SPI1_CK	SPI1_SCLK	SPI1 Master Clock output
R24	0	SPI4_D0__ SPI4_D0	P57	SPI1_DIN	SPI1_MISO	SPI1 Master Data input (input to CPU, output from SPI device)
P24	0	SPI4_D1__ SPI4_D1	P58	SPI1_DO	SPI1_MOSI	SPI1 Master Data output (output from CPU, input to SPI device)

2.1.11.1. SPI0 Signals

The Carrier *SPI0* device may be selected as the Boot Device – see Section 4.3 Boot Select.

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
SPI0_CS0#	*Output*	*CMOS VDDIO*	*SPI0 Master Chip Select 0 output*
SPI0_CS1#	*Output*	*CMOS VDDIO*	*SPI0 Master Chip Select 1 output*
SPI0_CK	*Output*	*CMOS VDDIO*	*SPI0 Master Clock output*
SPI0_DIN	*Input*	*CMOS VDDIO*	*SPI0 Master Data input (input to CPU, output from SPI device)*
SPI0_DO	*Output*	*CMOS VDDIO*	*SPI0 Master Data output (output from CPU, input to SPI device)*

2.1.11.2. SPI1 Signals

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
SPI1_CS0#	Output	CMOS VDDIO	SPI1 Master Chip Select 0 output
SPI1_CS1#	Output	CMOS VDDIO	SPI1 Master Chip Select 1 output
SPI1_CK	Output	CMOS VDDIO	SPI1 Master Clock output
SPI1_DIN	Input	CMOS VDDIO	SPI1 Master Data input (input to CPU, output from SPI device)
SPI1_DO	Output	CMOS VDDIO	SPI1 Master Data output (output from CPU, input to SPI device)

2.1.12. I2S Interface

The *SMARC-T4378* module uses *I2S* format for Audio signals. These signals are derived from the Multichannel Audio Serial Port (*MCASP*) of the *TI® AM4378* processor. The *MCASP* is a full duplex serial port that allows communication with external devices using a variety of serial protocols. The *I2S* protocol is part of the protocols supported by the *TI® AM4378* Cortex A9 processor.

I2S interface signals are exposed on the *SMARC-T4378* golden finger edge connector as shown below:

TI AM4378 CPU			SMARC-T4378 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
D24	3	XDMA_EVENT_INTR0__ CLKOUT1	S38	Audio_MCK	AUD_MCLK	Master clock output to Audio codecs
K23	3	MCASP0_FSR__ MCASP1_FSX	S39	I2S0_LRCK	I2S0_LRCK	Left& Right audio synchronization clock
M25	3	MCASP0_AXR1__ MCASP1_AXR0	S40	I2S0_SDOUT	I2S0_SDOUT	Digital audio Output
L24	3	MCASP0_AHCLKX__ MCASP1_AXR1	S41	I2S0_SDIN	I2S0_SDIN	Digital audio Input
L23	3	MCASP0_ACLKR__ MCASP1_ACLKX	S42	I2S0_CK	I2S0_CK	Digital audio clock

Note:

SGTL5000 I2S audio codec is used in *EVK-STD-CARRIER* evaluation carrier board and *TLV320AIC3106 I2S* codec is used in *SMART-BEE* carrier board. An external 24.576 Mhz crystal is used as a reference clock output to audio codec instead of Pin *S38*. Theoretically, both ways will work.

2.1.12.1 I2S0 Signals

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
I2S0_LRCK	Bi-Dir	CMOS VDDIO	Left& Right audio synchronization clock
I2S0_SDOUT	Output	CMOS VDDIO	Digital audio Output
I2S0_SDIN	Input	CMOS VDDIO	Digital audio Input
I2S0_CK	Bi-Dir	CMOS VDDIO	Digital audio clock
I2S0_MCK	Output	CMOS VDDIO	Master clock output to Audio codecs

2.1.13. Asynchronous Serial Port

The *SMARC-T4378* module supports four *UARTs* (*SER0:3*). *UART SER0* and *SER2* support flow control signals (*RTS#, CTS#*). *UART SER1* and *SER3* do not support flow control (*TX, RX* only). When working with software, *SER 3* is used for *SMARC-T4378* debugging console port.

The module asynchronous serial port signals have a *VDDIO* (1.8V or 3.3V) level signal swing. They can be converted to RS232 level and polarity signals by using a suitable RS232 transceiver. Almost all transceivers available accept a 3.3V signal level: example include the Texas Instruments MAX3243. Note that RS232 transceivers invert the signal; a logic '1' is a negative voltage (-3.0V to -15V) and a logic '0' a positive voltage (3.0V to 15V) on the RS232 line.

If users using 1.8V *VDDIO* module, a level-shift *IC* from 1.8V to 3.3V might be required.

Asynchronous serial ports interface signals are exposed on the *SMARC* golden finger edge connector as shown below:

TI AM4378 CPU			SMARC-T4378 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
SER0 Port						
J24	0	UART0_TXD__ UART0_TXD	P129	SER0_TX	SER0_TX	Asynchronous serial port data out
K25	0	UART0_RXD__ UART0_RXD	P130	SER0_RX	SER0_RX	Asynchronous serial port data in
J25	0	UART0_RTSN__ UART0_RTSN	P131	SER0_RTS#	SER0_RTS#	Request to Send handshake line for SER0
L25	0	UART0_CTSN__ UART0_CTSN	P132	SER0_CTS#	SER0_CTS#	Clear to Send handshake line for SER0
SER1 Port						
H24	0	UART3_TXD__ UART3_TXD	P134	SER1_TX	SER1_TX	Asynchronous serial port data out
H25	0	UART3_RXD__ UART3_RXD	P135	SER1_RX	SER1_RX	Asynchronous serial port data in
SER2 Port						
AE23	2	CAM1_DATA5__ UART2_TXD	P136	SER2_TX	SER2_TX	Asynchronous serial port data out
AD22	2	CAM1_DATA4__ UART2_RXD	P137	SER2_RX	SER2_RX	Asynchronous serial port data in
AE24	2	CAM1_DATA7__ UART2_RTSN	P138	SER2_RTS#	SER2_RTS#	Request to Send handshake line for SER2
AD23	2	CAM1_DATA6__ UART2_CTSN	P139	SER2_CTS#	SER2_CTS#	Clear to Send handshake line for SER2
SER3 Port (Debugging Port)						
B3	6	GPMC_WPN__ UART4_TXD	P140	SER3_TX	SER3_TX	Asynchronous serial port data out
A2	6	GPMC_WAIT0__ UART4_RXD	P141	SER3_RX	SER3_RX	Asynchronous serial port data in

2.1.13.1. UART Signals

Module pins for up to four asynchronous serial ports are defined. The ports are designated *SER0 – SER3*. Ports *SER0* and *SER2* are 4 wire ports (2 data lines and 2 handshake lines). Ports *SER1* and *SER3* are 2 wire ports (data only).

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
SER[0:3]_TX	*Output*	*CMOS VDDIO*	*Asynchronous serial port data out*
SER[0:3]_RX	*Input*	*CMOS VDDIO*	*Asynchronous serial port data in*
SER[0]_RTS#	*Output*	*CMOS VDDIO*	*Request to Send handshake line for SER0*
SER[0]_CTS#	*Input*	*CMOS VDDIO*	*Clear to Send handshake line for SER0*
SER[2]_RTS#	*Output*	*CMOS VDDIO*	*Request to Send handshake line for SER2*
SER[2]_CTS#	*Input*	*CMOS VDDIO*	*Clear to Send handshake line for SER2*

2.1.14. I2C Interface

There is a minimum configuration of I2C ports up to a maximum of 5 ports defined in the *SMARC* specification: *PM* (Power Management), *LCD* (Liquid Crystal Display), *GP* (General Purpose), *CAM* (Camera) and *HDMI*. Because *SMARC-T4378* does not have camera and *HDMI* interfaces, only *I2C_PM*, *I2C_LCD* and *I2C_GP* buses are present and all support multiple masters and slaves in fast mode (400 KHz operation).
The *I2C_PM* is implemented directly from *TI AM4378 I2C1* interfaces. The *I2C_LCD* is implemented directly from *TI AM4378 I2C2* interfaces. The *I2C_GP* is implemented directly from *TI AM4378 I2C0* interfaces.

The following diagram shows the *SMARC-T4378 I2C* interfaces.

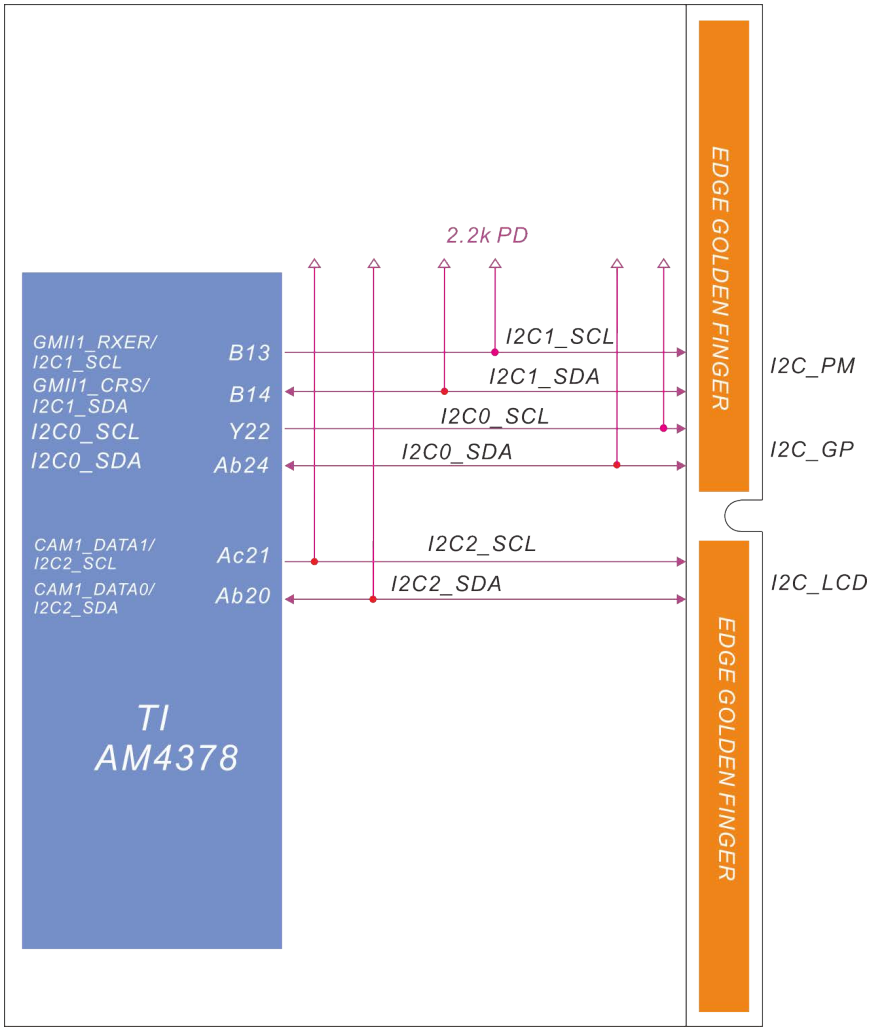


Figure 7: I2C Interface Block Diagram

This will be summarized below.

I2C Port		Primary Purpose	Alternative Use	I/O Voltage Level
Golden Finger Connector	AM4378 CPU			
I2C_PM	I2C1	Power Management support	System configuration management	CMOS 1.8V
I2C_GP	I2C0	General purpose use		CMOS VDDIO
I2C_LCD	I2C2	LCD display support, to read LCD display EDID EEPROMs (for parallel and LVDS LCD,)	General Purpose	CMOS VDDIO

Note:

The 2.2k pull-up resistors for *I2C_SCL* and *I2C_SDA* signals are on module.

The *I2C* interface signals are exposed on the *SMARC* golden finger edge connector as shown below:

TI AM4378 CPU			SMARC-T4378 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
I2C_PM						
B13	3	GMII1_RXER__ I2C1_SCL	P121	I2C_PM_CK	I2C_PM_CK	Power management I2C bus clock
B14	3	GMII1_CRS__ I2C1_SDA	P122	I2C_PM_DAT	I2C_PM_SDA	Power management I2C bus data
I2C_GP						
Y22	0	I2C0_SCL__ I2C0_SCL	S48	I2C_GP_CK	I2C_GP_CK	General purpose I2C bus clock
AB24	0	I2C0_SDA__ I2C0_SDA	S49	I2C_GP_DAT	I2C_GP_DAT	General purpose I2C bus data
I2C_LCD						
AC21	3	CAM1_DATA1__ I2C2_SCL	S139	I2C_LCD_CK	I2C_LCD_CK	LCD display I2C bus clock
AB20	3	CAM1_DATA0__ I2C2_SDA	S140	I2C_LCD_DAT	I2C_LCD_DAT	LCD display I2C bus data

There are two *I2C* devices on the *SMARC-T4378* Module at the *I2C_PM* (*I2C1*) bus and are operated at 1.8V. Those devices and their address details are listed in the following table:

#	Device	Description	Address (7-bit)	Address (8-bit)		Notes
				Read	Write	
I2C_PM (I2C1) Bus						
1	On Semiconductor CAT24C32	EEPROM	0x50	0xA1	0xA0	General purpose parameter EEPROM, Serial number, etc in PICMG EEEP format
2	Seiko S-35390A	Real-time clock IC	0x30	0x61	0x60	General purpose parameter with INT1 register access

2.1.15. CAN Bus Interface

The Controller Area Network (*CAN*) is a serial communications protocol which efficiently supports distributed real-time control with a high level of security. The *SMARC-T4378* module supports two *CAN* bus interfaces.
CAN interface signals are exposed on the *SMARC* golden finger edge connector as shown below:

TI AM4378 CPU			SMARC-T4378 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
CAN0 BUS						
K22	2	UART1_CTSN__ DCAN0_TX	P143	CAN0_TX	CAN0_TX	CAN0 Transmit output
L22	2	UART1_RTSN__ DCAN0_RX	P144	CAN0_RX	CAN0_RX	CAN0 Receive input
CAN1 BUS						
K21	2	UART1_RXD__ DCAN1_TX	P145	CAN1_TX	CAN1_TX	CAN1 Transmit output
L21	2	UART1_TXD__ DCAN1_RX	P146	CAN1_RX	CAN1_RX	CAN1 Receive input

By *SMARC* hardware specification, *CAN0* bus error condition signaling should be supported on the Module *GPI08* (*P116*) pin. This is an active low input to the Module from the *CAN* bus transceiver. *CAN1* bus error condition signaling should be supported on the Module *GPIO9* (*P117*) pin. This is an active low input to the Module from the *CAN* bus transceiver
A *CAN* transceiver on carrier is necessary to adapt the signals from *SMARC* golden finger edge connector, which is *TTL* levels, to the physical layer used. Because the *CAN* bus system is typically used to connect multiple systems and is often run over very long distances, both power supply and signal path must be electrically isolated to meet a certain isolation level. Users can refer the "***SMARC Carrier Board Hardware Design Guide***" or *CAN* transceiver application note such as *TI ISO1050* for more details.

2.1.15.1. CAN0 BUS Signals

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
CAN0_TX	Output	CMOS VDDIO	CAN0 Transmit output
CAN0_RX	Input	CMOS VDDIO	CAN0 Receive input

2.1.15.2. CAN1 BUS Signals

Edge Golden Finder Signal Name	Direction	Type Tolerance	Description
CAN1_TX	Output	CMOS VDDIO	CAN1 Transmit output
CAN1_RX	Input	CMOS VDDIO	CAN1 Receive input

2.1.16. GPIOs

The *SMARC-T4378* module supports 12 *GPIOs*, per the *SMARC* specification. Specific alternate functions are assigned to some *GPIOs* such as *PWM* / Tachometer capability, Camera support, *CAN* Error Signaling and HD Audio reset. All pins are capable of bi-directional operation. A default direction of operation is assigned, with half of them (*GPIO0 – GPIO5*) for use as outputs and the remainder (*GPIO6 – GPIO11*) as inputs by *SMARC* hardware specification.

GPIO signals are exposed on the *SMARC* golden finger edge connector as shown below:

TI AM4378 CPU			SMARC-T4378 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
GPIOs						
T23	9	SPI2_CS0__ GPIO0[23]	P108	GPIO0/CAM0_PWR#	GPIO0	Camera 0 Power Enable, active low output
P22	9	SPI2_D0__ GPIO0[20]	P109	GPIO1/CAM1_PWR#	GPIO1	Camera 1 Power Enable, active low output
P20	9	SPI2_D1__ GPIO0[21]	P110	GPIO2/CAM0_RST#	GPIO2	Camera 0 Reset, active low output
N20	9	SPI2_SCLK__ GPIO0[22]	P111	GPIO3/CAM1_RST#	GPIO3	Camera 1 Reset, active low output
AD19	7	CAM0_DATA5__ GPIO4[27]	P112	GPIO4/HDA_RST#	GPIO4	HD Audio Reset, active low output
AD20	7	CAM0_DATA7__ GPIO4[29]	P113	GPIO5/PWM_OUT	GPIO5	PWM output
M24	7	MCASP0_AHCLKR__ GPIO3[17]	P114	GPIO6/TACHIN	GPIO6	Tachometer input (used with the GPIO5 PWM)
H23	7	MCASP0_AXR0__ GPIO3[16]	P115	GPIO7/PCAM_FLD	GPIO7	PCAM_FLD (Field) signal input
Y18	7	CAM0_DATA2 GPIO4[24]	P116	GPIO8/CAN0_ERR#	GPIO8	CAN0 Error signal, active low input
AA18	7	CAM0_DATA3 GPIO4[25]	P117	GPIO9/CAN1_ERR#	GPIO9	CAN1 Error signal, active low input
AE19	7	CAM0_DATA4 GPIO4[26]	P118	GPIO10	GPIO10	
AE20	7	CAM0_DATA6 GPIO4[28]	P119	GPIO11	GPIO11	

2.1.16.1. GPIO Signals

Twelve Module pins are allocated for *GPIO* (general purpose input / output) use. All pins are capable of bi-directional operation. By *SMARC* specification, *GPIO0 – GPIO5* are recommended for use as outputs and the remainder (*GPIO6 – GPIO11*) as inputs.
At Module power-up, the state of the *GPIO* pins may not be defined, and may briefly be configured in the “wrong” state, before boot loader code corrects them. Carrier designers should be aware of this and plan accordingly.
All *GPIO* pins are capable of generating interrupts. The interrupt characteristics (edge or level sensitivity, polarity) are generally configurable in the *AM4378* register set.

Edge Golden Finder Signal Name	Preferred Direction	Type Tolerance	Description
GPIO0/CAM0_PWR#	Output	CMOS VDDIO	Camera 0 Power Enable, active low output
GPIO1/CAM1_PWR#	Output	CMOS VDDIO	Camera 1 Power Enable, active low output
GPIO2/CAM0_RST#	Output	CMOS VDDIO	Camera 0 Reset, active low output
GPIO3/CAM1_RST#	Output	CMOS VDDIO	Camera 1 Reset, active low output
GPIO4/HDA_RST#	Output	CMOS VDDIO	HD Audio Reset, active low output
GPIO5/PWM_OUT	Output	CMOS VDDIO	PWM output
GPIO6/TACHIN	Input	CMOS VDDIO	Tachometer input (used with the GPIO5 PWM)
GPIO7/PCAM_FLD	Input	CMOS VDDIO	PCAM_FLD (Field) signal input
GPIO8/CAN0_ERR#	Input	CMOS VDDIO	CAN0 Error signal, active low input
GPIO9/CAN1_ERR#	Input	CMOS VDDIO	CAN1 Error signal, active low input
GPIO10	Input	CMOS VDDIO	
GPIO11	Input	CMOS VDDIO	

2.1.17. Watchdog Timer Interface

AM4378 features an internal *WDT.* Embedian's Linux kernel enables the internal *AM4378 WDT* and makes this functionality available to users through the standard Linux Watchdog *API*.
A description of the *API* is available following the link below:
http://www.kernel.org/doc/Documentation/watchdog/watchdog-api.txt

WDT signals are exposed on the *SMARC* golden finger edge connector as shown below:

TI AM4378 CPU			SMARC-T4378 Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
Watchdog Timer						
K24	6	UART3_RTSN__ EHRPWM5B	S145	WDT_TIME_OUT#	WDT_TIME_OUT#	Watchdog-Timer Output

2.1.18. Four-Wire Resistive Touch (ADC) Interface

Resistive touch interface is not defined in SMARC hardware specification. However, to support legacy touch devices, *SMARC-T4378* has four-wire resistive touch interface on *AFB* (Alternative Function Block) pins.

Touchscreen controller on *Sitara AM4378* is an 8 channel general purpose ADC, with support for interleaving Touch Screen conversions for a 4-wire resistive panel. A resistive touchscreen operates by applying a voltage across a resistive network and measuring the change in resistance at a given point on the matrix where the screen is touched by an input (stylus or finger). The change in the resistance ratio marks the location on the touchscreen.
Four-wire *TSC* has been implemented on *SMARC-T4378* module. *TSC* signals are exposed on the *SMARC* golden finger edge connector as shown below:

TI AM335x CPU			SMARC T335X Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
4-wire TSC						
AA12	0	ADC0_AIN0__ ADC0_AIN0	S18	AFB1_OUT	XPUL	XP: Plus X-axis on-off control signal
Y13	0	ADC0_AIN2__ ADC0_AIN2	S19	AFB2_OUT	YPLL	YP: Plus Y-axis on-off control signal
Y12	0	ADC0_AIN1__ ADC0_AIN1	S21	AFB4_IN	XNUR	XM: Minus X-axis on-off control signal
AA13	0	ADC0_AIN3__ ADC0_AIN3	S22	AFB5_IN	YNLR	YM: Minus Y-axis on-off control signal

2.1.19. JTAG

Figure 8 shows the *SMARC-T4378 JTAG* connectors location and pin out.

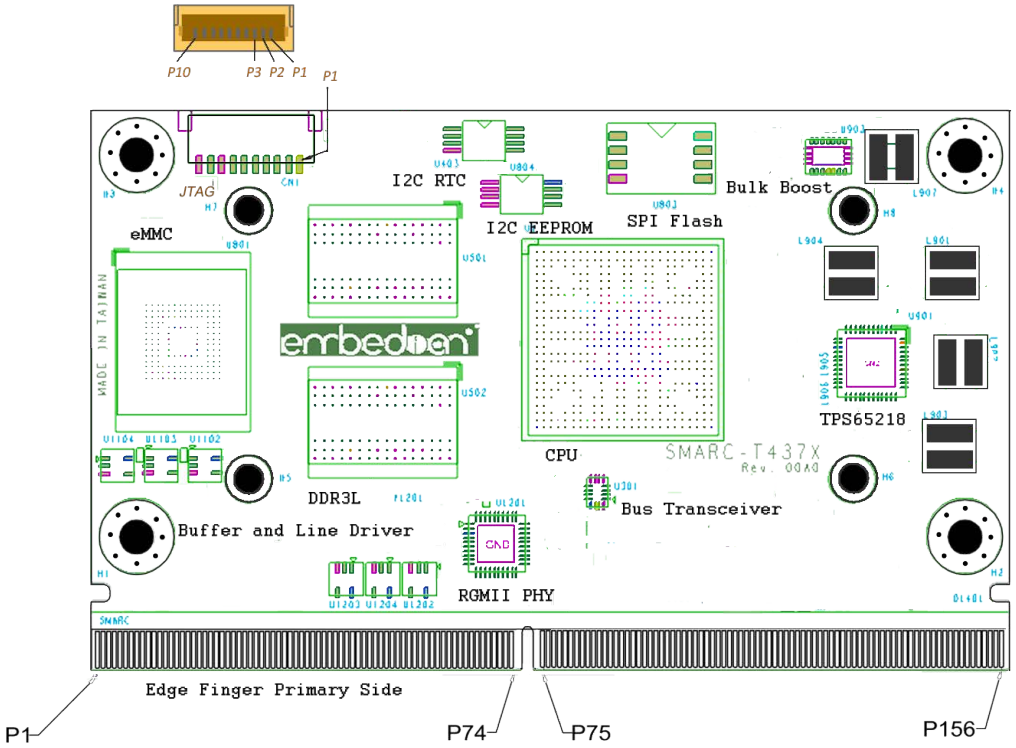


Figure 8: JTAG Connector Location and Pinout

JTAG functions for *CPU* debug and test are implemented on separate small form factor connector (*CN1*: *JST SM10B-SRSS-TB*, 1mm pitch R/A SMD Header). The *JTAG* pins are used to allow test equipment and circuit emulators to have access to the Module CPU. The pin-outs shown below are used:

TI T4378 CPU			JTAG(Connector: JST SM10B-SRSS-TB, 1mm pitch R/A SMD Header)		Type	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
JTAG						
			1	VDD_33A	Power	JTAG I/O Voltage (sourced by Module)
Y25	0	nTRST	2	nTRST	I	JTAG Reset, active low
Y24	0	TMS	3	TMS	I	JTAG mode select
AA24	0	TDO	4	TDO	O	JTAG data out
Y20	0	TDI	5	TDI	I	JTAG data in
AA25	0	TCK	6	TCK	I	JTAG clock
AA25	0	TCK	7	RTCK	I	JTAG return clock
			8	GND	Ground	Ground
			9	MFG_Mode#	I	Pulled low to allow in-circuit SPI ROM update
			10	GND	Ground	Ground

2.1.20. Boot ID EEPROM

The *SMARC-T4378* module includes an *I2C* serial *EEPROM* available on the *I2C_PM* bus. An On Semiconductor *24C32* or equivalent *EEPROM* is used in the module. The device operates at 1.8V. The Module serial *EEPROM* is placed at *I2C* slave addresses A2 A1 A0 set to 0 (I2C slave address 50 hex, 7 bit address format or A0 / A1 hex, 8 bit format) (for I2C EEPROMs, address bits A6 A5 A4 A3 are set to binary 0101 convention).

The module serial *EEPROM* is intended to retain module parameter information, including serial number. The module serial *EEPROM* data structure conforms to the *PICMG® EEEP* Embedded *EEPROM* Specification.

Note:
The *EEPROM ID* memory layout is now follow the mainline and as follows.

Name	Size (Bytes)	Contents
Header	4	MSB 0xEE3355AA LSB
Board Name	8	Name for Board in ASCII "SMCT4X80" = Embedian SMARC-T4378 Computer on Module running at 800Mhz with 512MB DDR3 Configuration "SMCT4X1G" = Embedian SMARC-T4378 Computer on Module running at 1Ghz and with 1GB DDR3L Configuration
Version	4	Hardware version code for version in ASCII "00A0" = rev. A0
Serial Number	12	Serial number of the board. This is a 12 character string which is: WWYY4XZZnnnn Where: WW = 2 digit week of the year of production YY = 2 digit year of production 4X = T4378 Module ZZ = 80 or 1G (CPU running speed and DDR3L Configuration Variants nnnn = incrementing board number
Configuration Option	32	Codes to show the configuration setup on this board. For the available module variants supported, the following codes are used: ASCII = "SMCT4X80" = default configuration Remaining 24 bytes are reserved
Available	6	Reserved
Available	6	Reserved
Available	32720	Available space for other non-volatile codes/data

2.2 SMARC-T4378 Debug

2.2.1. Serial Port Debug

SMARC module has 4 serial output ports, *SER0, SER1, SER2 and SER3*. Out of these 4 serial ports, *SER3* is set as the serial debug port use for *AM4378* from Embedian. Users can change to any port they want to. *SER3* is exposed (along with all other serial ports available on the module) in the *SMARC-T4378* Evaluation Carrier. The default baud rate setting is *115,200 8N1*.
SER3 pin out of the *SMARC-T4378* is shown below:

TI AM4378 CPU		SMARC-T4378 Edge Golden Finger		Net Names	Notes
mode	Pin Name	Pin#	Pin Name		
SER3 (Debugging Port)					
6	GPMC_WPN__ UART4_TXD	P140	SER3_TX	SER3_TX	Asynchronous serial port data out
6	GPMC_WAIT0__ UART4_RXD	P141	SER3_RX	SER3_RX	Asynchronous serial port data in

2.3 Mechanical Specifications

2.3.1. Module Dimensions

The *SMARC-T4378* complies with *SMARC* Hardware Specification in an 82mm x 50 mm form factor.

2.3.2. Height on Top

2.9mm maximum (without *PCB*) complied with *SMARC* specification defines as 3mm as the maximum.

2.3.3. Height on Bottom

0.9mm maximum (without *PCB*) complied with *SMARC* specification defines as 1.3mm as the maximum.

2.3.4. Mechanical Drawings

The mechanical information is shown in Figure 9: *SMARC-T4378* Mechanical Drawings (Top View) and Figure 10: *SMARC-T4378* Mechanical Drawings (Bottom View))

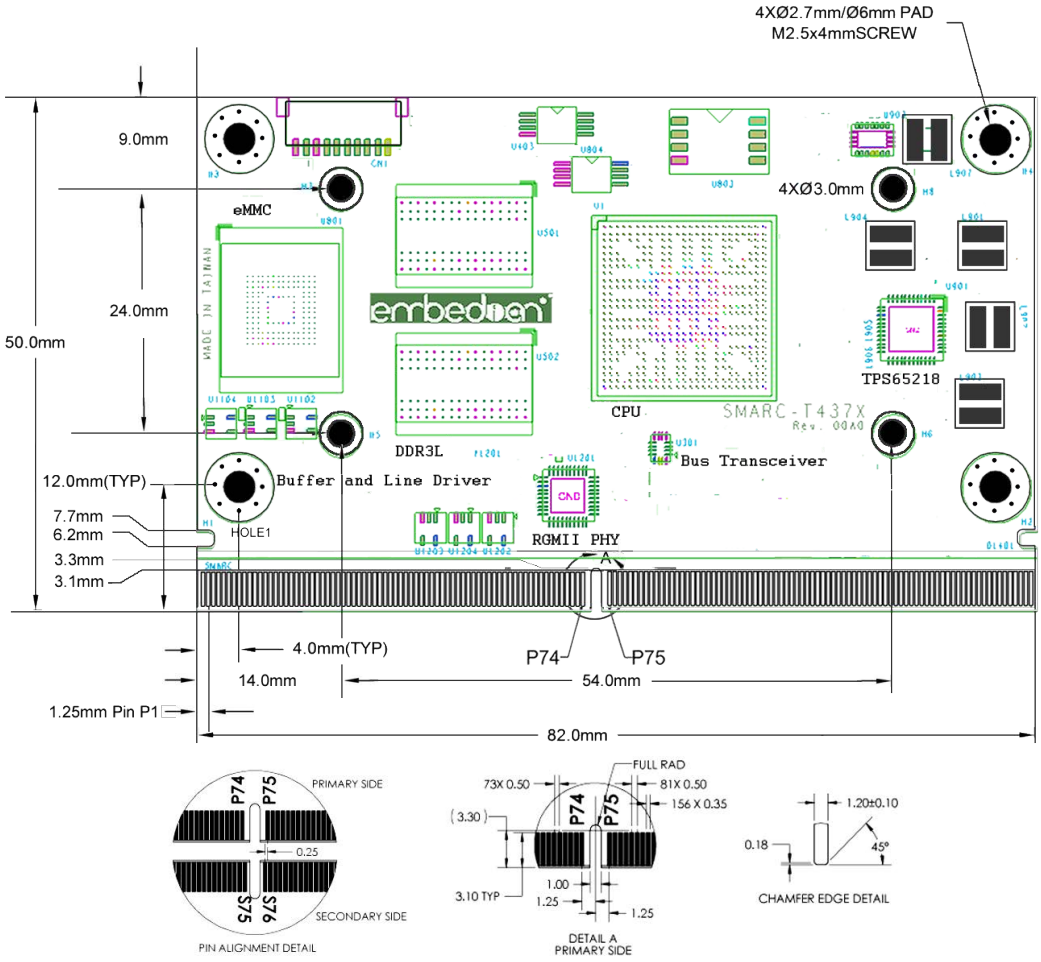


Figure 9. SMARC-T4378 Mechanical Drawings (Top View)

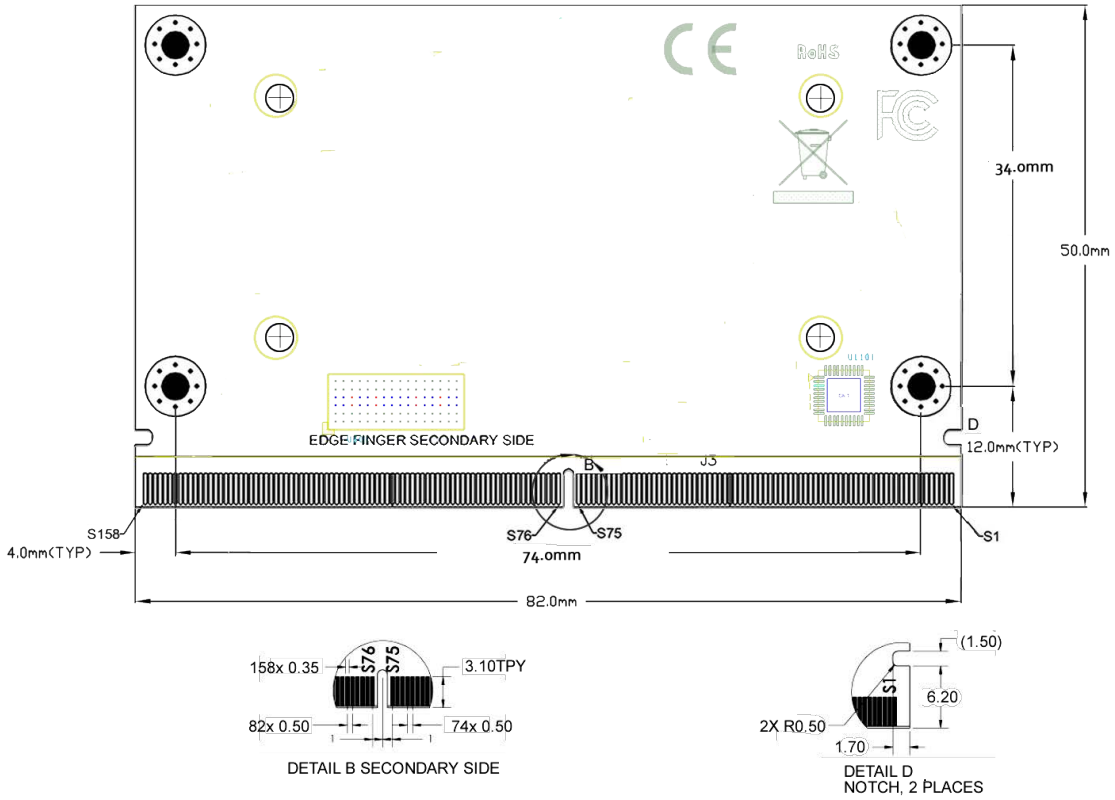


Figure 10. SMARC-T4378 Mechanical Drawings (Bottom View)

The figure on the following page details the 82mm x 50mm Module mechanical attributes, including the pin numbering and edge finger pattern.

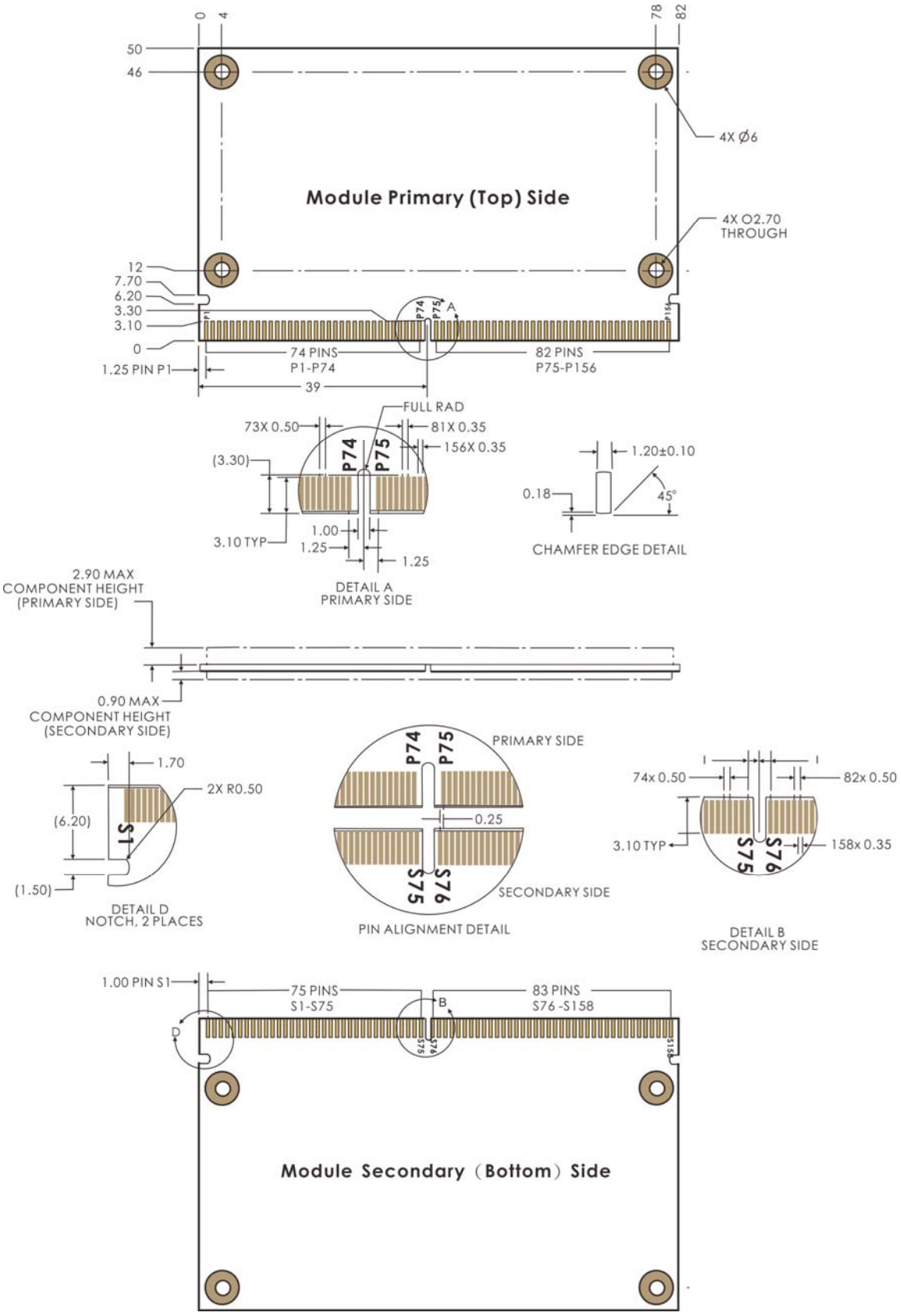


Figure 11: SMARC-T4378 Module Mechanical Outline

Top side major component (IC and Connector) information is shown in Figure 12: *SMARC-T4378* Top side components.

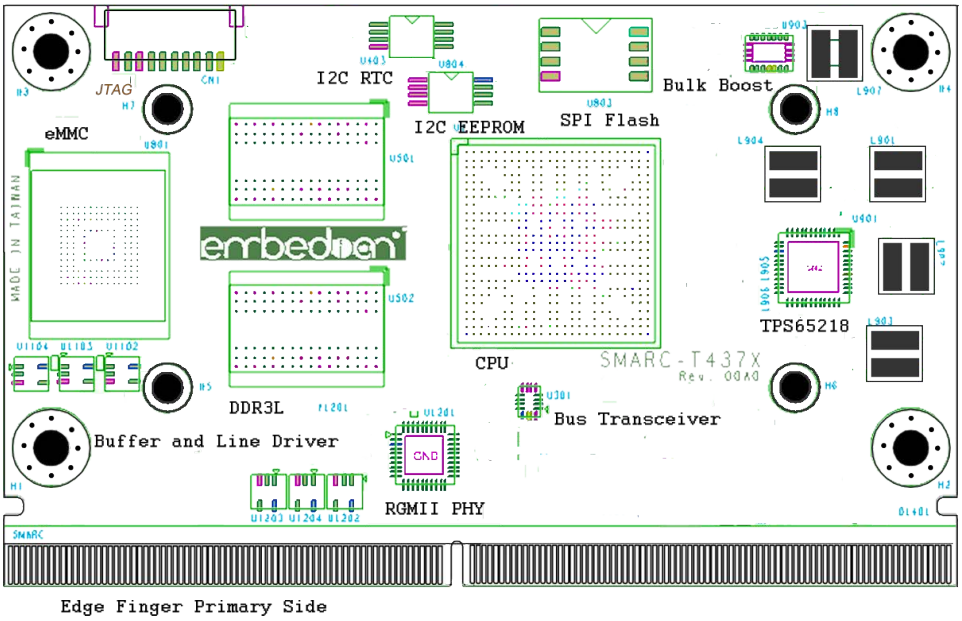


Figure 12. SMARC-T4378 Top Side Components

Bottom side major component (IC and Connector) information is shown in Figure 13: *SMARC-T4378* Bottom side components.

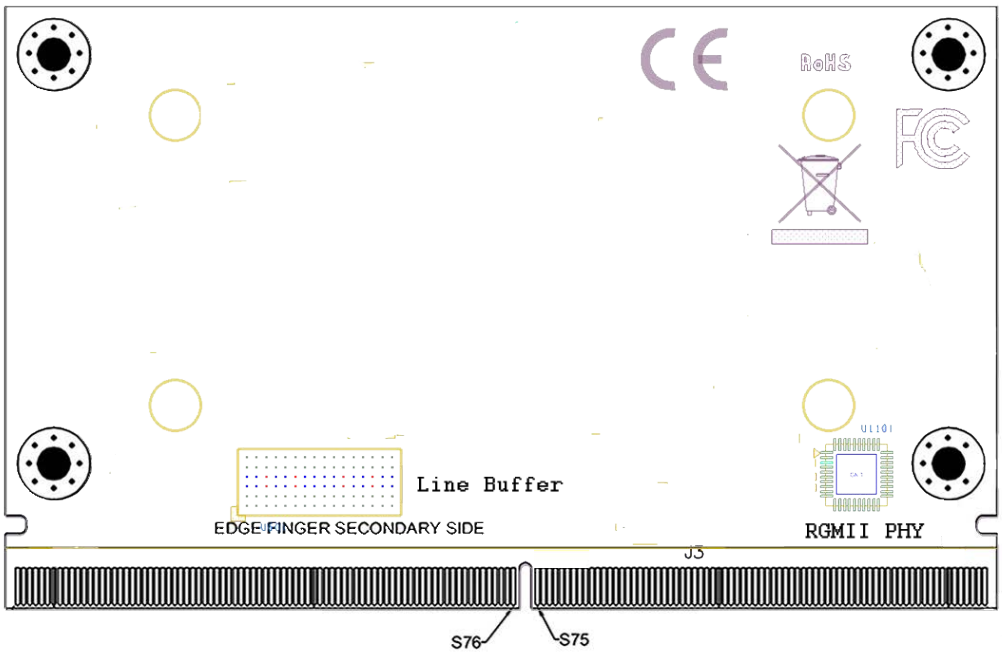


Figure 13. SMARC-T4378 Bottom Side Components

SMARC-T4378 height information from Carrier board Top side to tallest Module component is shown in Figure 14: *SMARC-T4378* Minimum "Z" Height:

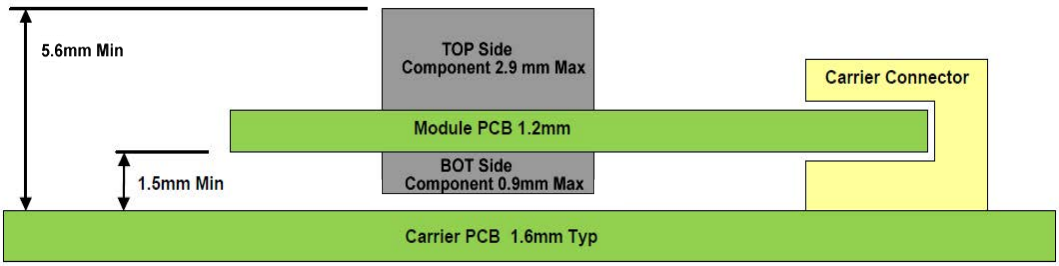


Figure 14. SMARC-T4378 Minimum "Z" Height

The *SMARC* connector board-to-board stack heights that are available may result in the use of non-standard spacer lengths. The board-to-board stack heights available include 1.5mm, 2.7mm and 5mm. Of these three, only the spacer for the 5mm stack would likely be a standard length.

When a 1.5mm stack height Carrier board connector is used, there shall not be components on the Carrier board Top side in the Module region. Additionally, when 1.5mm stack height connectors are used, there should not be PCB traces on the Carrier top side in the Module shadow. This is to prevent possible problems with metallic Module heat sink attachment hardware that may protrude through the Module.

If Carrier board components are required in this region, then the Carrier components must be on the Carrier Bottom side, or a taller Module-to-Carrier connector may be used. Stack heights of 2.7mm, 3mm, 5mm and up are available.

2.3.5. Carrier Board Connector PCB Footprint

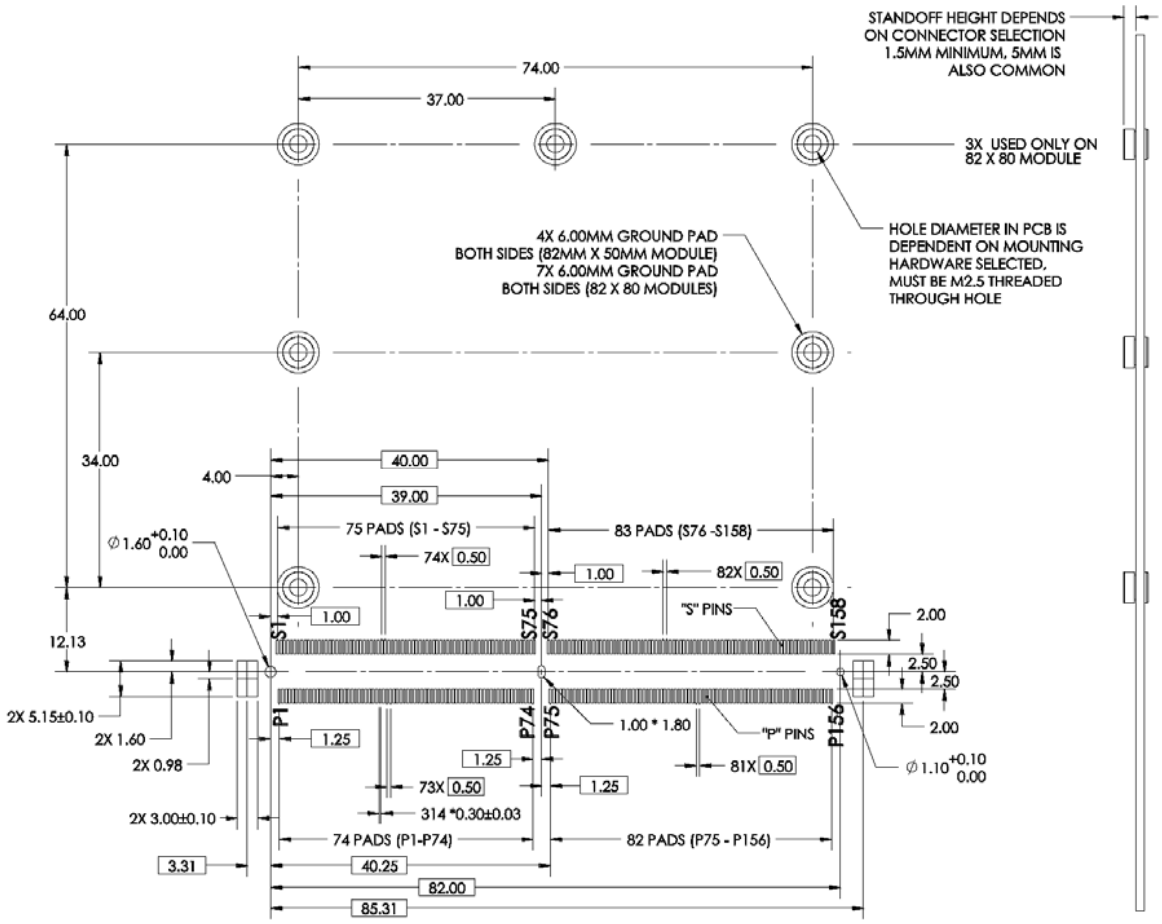


Figure 15: Carrier Board Connector PCB Footprint

Note:

The diameter for the 4 holes (82mm x 50mm Module) or 7 holes (82mm x 80mm Module) depends on the spacer hardware selection. See the section below for more information on this.

2.3.6. Module Assembly Hardware

The *SMARC-T4378* module is attached to the carrier with four *M2.5* screws. A 4mm length screw is usually used. The attachment holes are located on the corners of the module. Attachment holes have a 6mm diameter pad, 2.7

mm dia drill hole as shown Figure 9: *SMARC-T4378* Mechanical Drawings (Top View)

2.3.7. Carrier Board Standoffs

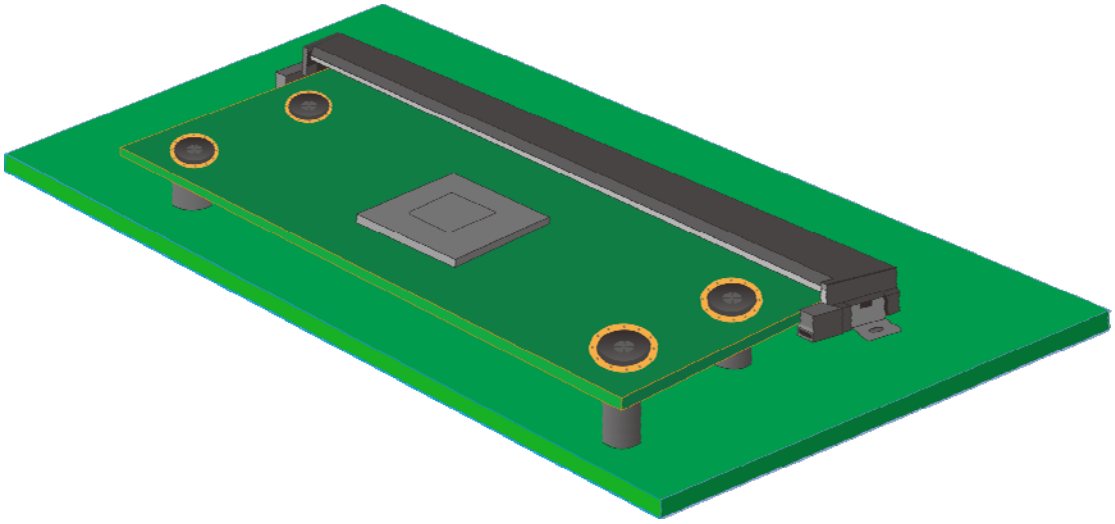


Figure 16: Screw Fixation

Standoffs secured to the Carrier board are expected. The standoffs are to be used with *M2.5* hardware. Most implementations will use Carrier board standoffs that have *M2.5* threads (as opposed to clearance holes). A short *M2.5* screw and washer, inserted from the Module top side, secures the Module to the Carrier board threaded standoff.

The *SMARC* connector board-to-board stack heights that are available may result in the use of non-standard spacer lengths. The board-to-board stack heights available include 1.5mm, 2.7mm and 5mm. Of these three, only the spacer for the 5mm stack would likely be a standard length.

Penn Engineering and Manufacturing (*PEM*) (www.pemnet.com) makes surface mount spacers with M2.5 internal threads. The product line is called *SMTSO* (“surface mount technology stand offs”). The shortest standard length offered is 2mm. A custom part with 1.5mm standoff length, M2.5 internal thread, and 5.56mm standoff *OD* is available from *PEM*. The Carrier *PCB* requires a 4.22mm hole and 6.2mm pad to accept these parts.

Other vendors such as *RAF* Electronic Hardware (www.rafhdwe.com) offer *M2.5* compatible swaged standoffs. Swaged standoffs require the use of a press and anvil at the *CM*. Their use is common in the industry. The standoff *OD* and Carrier *PCB* hole size requirements are different from the *PEM SMTSO* standoffs described above.

2.3.8. Carrier Connector

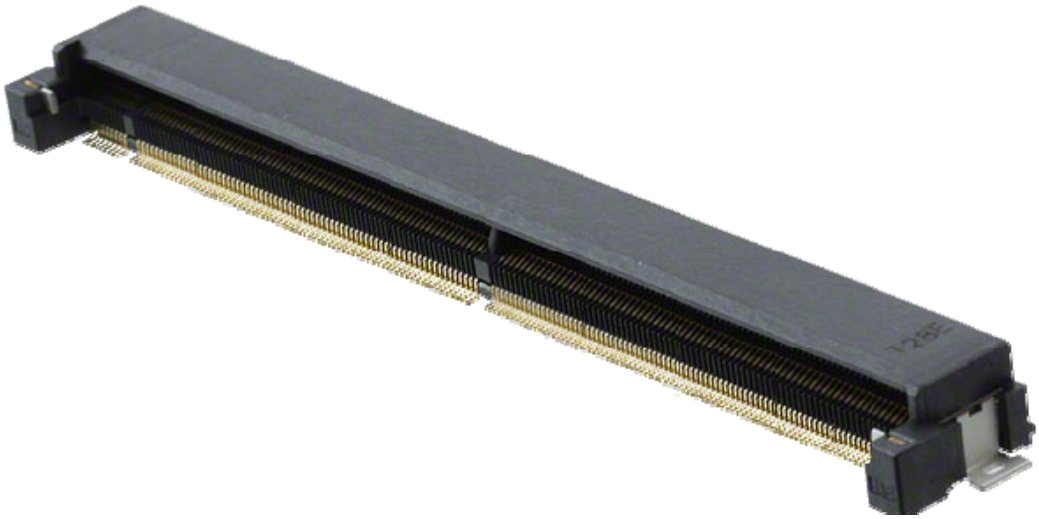


Figure 17: MXM3 Carrier Connector

The Carrier board connector is a 314 pin 0.5mm pitch right angle part designed for use with 1.2mm thick mating PCBs with the appropriate edge finger pattern. The connector is commonly used for *MXM3* graphics cards. The *SMARC* Module uses the connector in a way quite different from the *MXM3* usage.

Vender	Vendor P/N	Stack Height	Body Height	Contact Plating	Pin Style	Body Color
Foxconn	AS0B821-S43B - *H	1.5mm	4.3mm	Flash	Std	Black
Foxconn	AS0B821-S43N - *H	1.5mm	4.3mm	Flash	Std	Ivory
Foxconn	AS0B826-S43B - *H	1.5mm	4.3mm	10 u-in	Std	Black
Foxconn	AS0B826-S43N - *H	1.5mm	4.3mm	10 u-in	Std	Ivory
Lotes	AAA-MXM-008-P04_A	1.5mm	4.3mm	Flash	Std	Tan
Lotes	AAA-MXM-008-P03	1.5mm	4.3mm	15 u-in	Std	Tan
Speedtech	B35P101-02111-H	1.56mm	4.0mm	Flash	Std	Black
Speedtech	B35P101-02011-H	1.56mm	4.0mm	Flash	Std	Tan
Speedtech	B35P101-02112-H	1.56mm	4.0mm	10 u-in	Std	Black
Speedtech	B35P101-02012-H	1.56mm	4.0mm	10 u-in	Std	Tan
Speedtech	B35P101-02113-H	1.56mm	4.0mm	15 u-in	Std	Black
Speedtech	B35P101-02013-H	1.56mm	4.0mm	15 u-in	Std	Tan
Aces	91781-314 2 8-001	2.7mm	5.2mm	3 u-in	Std	Black

Vender	Vendor P/N	Stack Height	Body Height	Contact Plating	Pin Style	Body Color
Foxconn	AS0B821-S55B - *H	2.7mm	5.5mm	Flash	Std	Black
Foxconn	AS0B821-S55N - *H	2.7mm	5.5mm	Flash	Std	Ivory
Foxconn	AS0B826-S55B - *H	2.7mm	5.5mm	10 u-in	Std	Black
Foxconn	AS0B826-S55N - *H	2.7mm	5.5mm	10 u-in	Std	Ivory
Speedtech	B35P101-02121-H	2.76mm	5.2mm	Flash	Std	Black
Speedtech	B35P101-02021-H	2.76mm	5.2mm	Flash	Std	Tan
Speedtech	B35P101-02122-H	2.76mm	5.2mm	10 u-in	Std	Black
Speedtech	B35P101-02022-H	2.76mm	5.2mm	10 u-in	Std	Tan
Speedtech	B35P101-02123-H	2.76mm	5.2mm	15 u-in	Std	Black
Speedtech	B35P101-02023-H	2.76mm	5.2mm	15 u-in	Std	Tan
Foxconn	AS0B821-S78B - *H	5.0mm	7.8mm	Flash	Std	Black
Foxconn	AS0B821-S78N - *H	5.0mm	7.8mm	Flash	Std	Ivory
Foxconn	AS0B826-S78B - *H	5.0mm	7.8mm	10 u-in	Std	Black
Foxconn	AS0B826-S78N - *H	5.0mm	7.8mm	10 u-in	Std	Ivory
Yamaichi (1)	CN113-314-2001	5.0mm	7.8mm	0.3 u-meter	Std	Black

Other, taller stack heights may be available from these and other vendors. Stack heights as tall as 11mm are shown on the Aces web site.

Note:

1. *Yamaichi CN113-314-2001* is automotive grade.
2. The vendor drawings for the connectors listed above show a PCB footprint pattern for use with an MXM3 graphics card. This footprint, and the associated pin numbering, is not suitable for *SMARC* use. The

MXM3 standard gangs large groups of pins together to provide ~80W capable power paths needed for X86 graphics cards. The *SMARC* module “ungangs” these pins to allow more signal pins. Footprint and pin numbering information for application of this 314 pin connector to *SMARC* is given in the sections below.

2.3.9. Module Cooling Solution—Heat Spreader

A standard heat-spreader plate for use with the *SMARC* 82mm x 50mm form factor is described below. A standard heat spreader plate definition allows the customer to use a Module from multiple vendors.

The heat spreader plate is sized at 82mm x 42mm x 3mm, and sits 3mm above the *SMARC* Module. The heat spreader plate ‘Y’ dimension is deliberately set at 42mm and not 50mm, to allow the plate to clear the *SMARC* MXM3 connector. The plate is shown in the figures below.

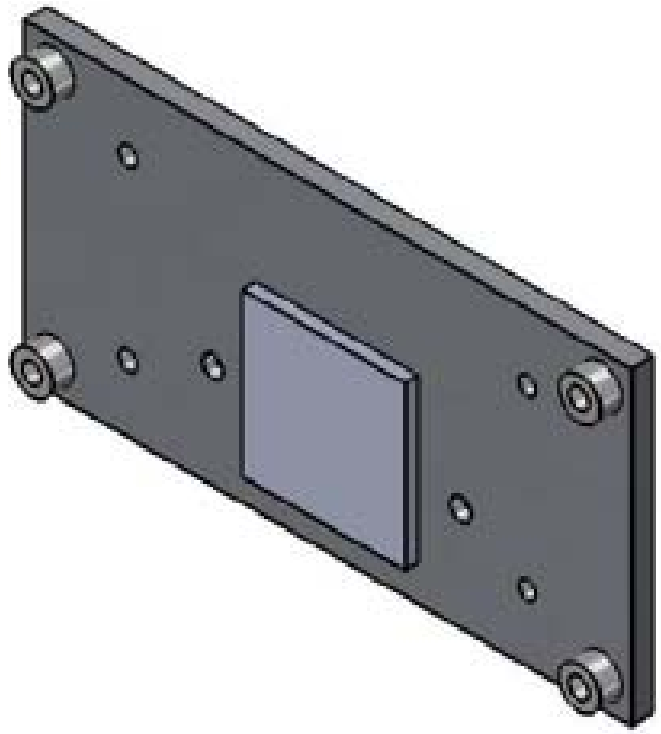


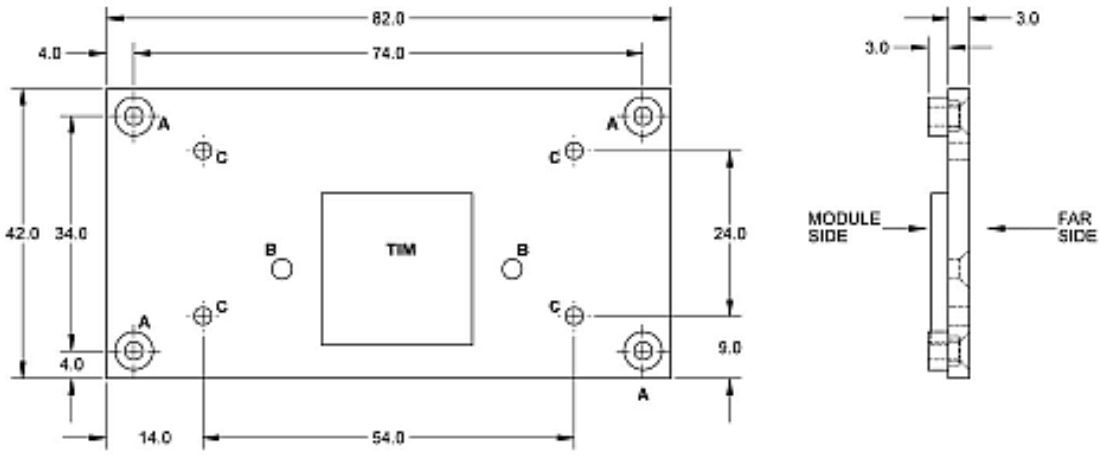
Figure 18: Heat Spreader

The internal square in the figure above is a thermally conductive and mechanically compliant Thermal Interface Material (or “TIM”). The exact X-Y position and Z thickness details of the TIM vary from design to design.

The two holes immediately adjacent to the TIM serve to secure the PCB in the SOC area and compress the TIM.

The four interior holes that are further from the center allow a heat sink to be attached to the heat spreader plate, or they can be used to secure the heat spreader plate to a chassis wall that serves as a heat sink.

Dimensions and further details may be found in the following figure.



Dimensions in the figure above are in millimeters. “TIM” stands for “Thermal Interface Material”. The TIM takes up the small gap between the SOC top and the Module - facing side of the heat spreader.

Hole Reference	Description	Size
A	*SMARC Module corner mounting holes Spacing determined by SMARC specification for 82mm x 50mm Modules.* *Typically these holes have 3mm length press fit or swaged clearance standoffs on the Module side.* *These holes are typically countersunk on the far side of the plate, to allow the heat spreader plate to be flush with a secondary heat sink.*	*Hole size depends on standoffs used. Standoff diameter must be compatible with SMARC Module mounting hole pad and hole size (6.0mm pads, 2.7mm holes on the Module). The holes and standoffs are for use with M2.5 screw hardware.* *The far side of these holes are counter-sunk to allow the attachment screw to be flush with the far side heat spreader surface.*
B	*Not Defined*	
C	*Fixed location holes to allow the attachment of a heat sink to the heat spreader, or to allow the heat spreader to be secured to a chassis wall that can serve as a heat sink.*	*M3 threaded holes*

2.4 Electrical Specifications

2.4.1. Supply Voltage

The *SMARC-T4378* module operates over an input voltage range of *3.0V* to *5.25V*. Power is provided from the carrier through *10* power pins as defined by the *SMARC* specification.

Caution! A single 5V *DC* input is recommended.

2.4.2. RTC/Backup Voltage

3.0V *RTC* backup power is provided through the *VDD_RTC* pin from the carrier board. This connection provides back up power to the module *PMIC*. The *RTC* is powered via the primary system 3.3V supply during normal operation and via the *VBAT* power input, if it is present, during power-off.

2.4.3. No Separate Standby Voltage

The *SMARC-T4378* does not have a standby power rail. Standby operation is powered through the main supply voltage rail, as defined in the *SMARC* specification.

2.4.4. Module I/O Voltage

The *SMARC-T4378* module supports 1.8V (*SMARC* v1.1 compliant) or 3.3V (*SMARC* v1.0 compliant) level I/O voltage depending on the part number that users selected.

2.4.5. MTBF

The *SMARC-T4378* System MTBF (hours) : >100,000 hours

The above *MTBF* (Mean Time Between Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and a Bellcore calculation for the remaining parts. The Bellcore calculation used is "Method 1 Case 1". In that particular method the components are assumed to be operating at a 50 % stress level in a 40° C ambient environment and the system is assumed to have not been burned in. Manufacturer's data has been used wherever possible. The manufacturer's data, when used, is specified at 50°C, so in that sense the following results are slightly conservative. The *MTBF* values shown below are for a 40°C in an office or telecommunications environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, salt water exposure, etc.) lower *MTBF* values.

2.4.6. Power Consumption

The power consumption values listed in this document were measured under a controlled environment. The hardware used for testing includes an *SMARC-T4378* module, *EVK-STD-CARRIER* carrier board, *VGA DSUB* monitor, *SD* card and *USB* keyboard. The carrier board was powered externally by a power supply unit so that it does not influence the power consumption value that is measured for the module. The *USB* keyboard was detached once the module was configured within the *OS*. All recorded values were averaged over a 30 second time period. The modules were not cooled by the heatspreader specific to the module variants.

Each module was measured while running 32 bit Linaro Ubuntu 14.04. To measure the worst case power consumption, the cooling solution was removed and the *CPU* core temperature was allowed to run between 95° and 100°C at 100% workload. The peak current value was then recorded. This value should be taken into consideration when designing the system's power supply to ensure that the power supply is sufficient during worst case scenarios.

Power consumption values were recorded during the following stages:
Linaro Ubuntu 14.04 (32 bit)

- Desktop Idle
- 100% CPU workload
- 100% CPU workload at approximately 100°C peak power consumption

Note: With the linux stress tool, we stressed the CPU to maximum frequency.

The table below provides additional information about the different variants offered by the *SMARC-T4378*.

2.4.6.1. SMARC-T4378-01G Cortex A9 1GHz and 1GB DDR3L

With *4GB* onboard *eMMC*.

P/N: SMARC-T4378-S	TI T4378 Cortex A9 1GHz Solo Core 512KB L2 Cache		
Memory Size	1024MB		
Operating System	Ubuntu 14.04		
Power States	Desktop Idle	100% workload	Max. power consumption
Power Consumption (Amp/Watts)	0.2A/1W	0.3A/1.5W	0.40A/2.0W

2.4.6.2. SMARC-T4378-800 Cortex A9 800MHz and 512MB DDR3L

With *4GB* onboard *eMMC*.

P/N: SMARC-T4378-U	TI T4378 Cortex A9 1GHz Dual Lite Core 512KB L2 Cache		
Memory Size	512MB		
Operating System	Ubuntu 14.04		
Power States	Desktop Idle	100% workload	Max. power consumption
Power Consumption (Amp/Watts)	0.18A/0.9W	0.28A/1.4W	0.38A/1.9W

2.5 Environmental Specifications

2.5.1. Operating Temperature

The *SMARC-T4378* module operates from *0°C* to *60°C* air temperature, without a passive heat sink arrangement. Industrial temperature (*-40°C ~85°C* is also available with different part number *SMARC-T4378-I*).

2.5.2. Humidity

Operating: *10%* to *90% RH* (non-condensing).
Non-operating: *5%* to *95% RH* (non-condensing).

2.5.3. ROHS/REACH Compliance

The *SMARC-T4378* module is compliant to the 2002/95/EC *RoHS* directive and *REACH* directive.

Connector PinOut

This Chapter gives detail pinout of *SMARC-T4378* golden finger edge connector.

Section include：

- *SMARC-T4378* Connector Pin Mapping

Chapter 3 Connector Pinout

The Module pins are designated as *P1 – P156* on the Module Primary (Top) side, and *S1 – S158* on the Module Secondary (Bottom) side. There are total of 314 pins on the Module. The connector is sometimes identified as a 321 pin connector, but 7 pins are lost to the key (4 on the primary side and 3 on secondary side).

The Secondary (Bottom) side faces the Carrier board when a normal or standard Carrier connector is used.

The *SMARC-T4378* module pins are deliberately numbered as *P1 – P156* and *S1 – S158* for clarity and to differentiate the *SMARC* Module from *MXM3* graphics modules, which use the same connector but use the pins for very different functions. *MXM3* cards and *MXM3* baseboard connectors use different pin numbering scheme.

3.1 SMARC-T4378 Connector Pin Mapping

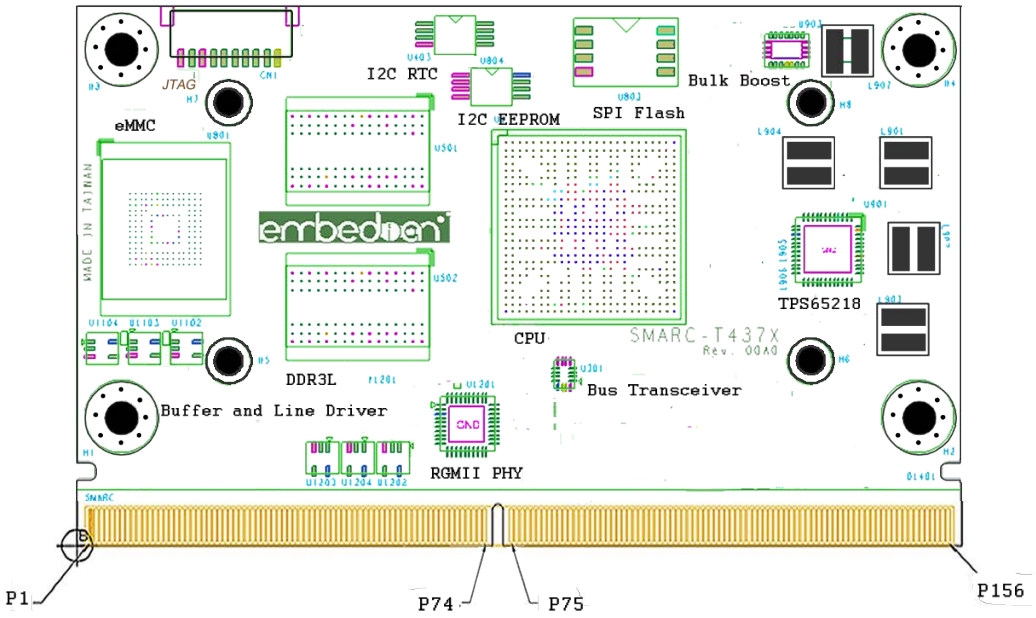


Figure 19: SMARC-T4378 edge finger primary pins

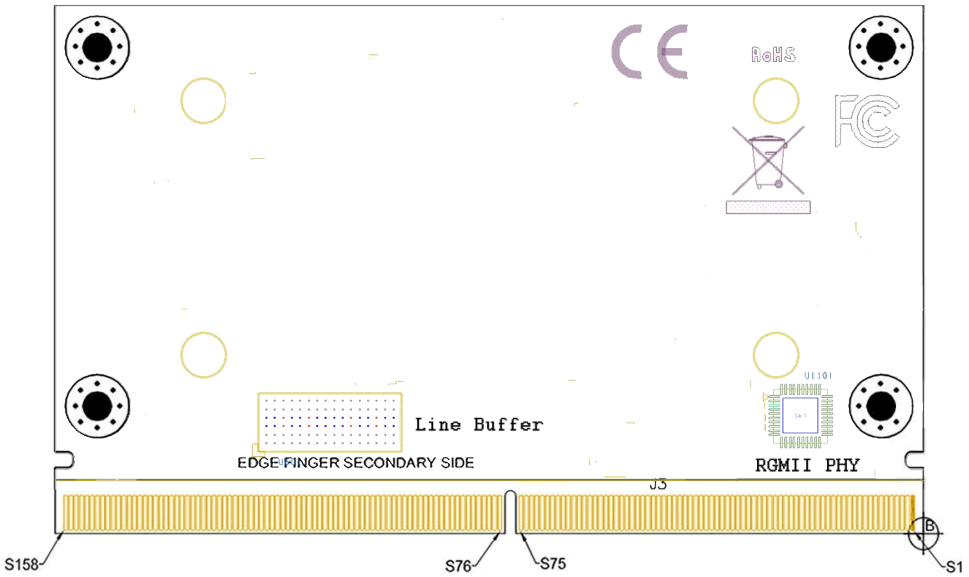


Figure 20: SMARC-T4378 edge finger secondary pins

The next tables describe each pin, its properties, and its use on the module and development board.

The "*SMARC Edge Finger*" column shows the connection of the signals defined in the *SMARC* specification. The "*TI T4378 CPU*" column shows the connection of the *CPU* signals on the module. The format of this column is "*Ball/Mode/Signal Name*" where "*Signal Name*" is the chip where the signals are connected, and "*Ball*" is the name of the pad where the signals are connected as they are defined in the *AM4378* processor datasheet.

Pinout Legend

I	*Input*
O	*Output*
I/O	*Input or output*
P	*Power*
AI	*Analogue input*
AO	*Analogue output*
AIO	*Analogue Input or analogue output*
OD	*Open Drain Signal*
#	*Low level active signal*

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P1	PCAM_PXL_CK1					Not used
P2	GND				P	Ground
P3	CSI1_CK+ / PCAM_D0					Not used
P4	CSI1_CK- / PCAM_D1					Not used
P5	PCAM_DE					Not used
P6	PCAM_MCK					Not used
P7	CSI1_D0+ / PCAM_D2					Not used
P8	CSI1_D0- / PCAM_D3					Not used
P9	GND				P	Ground
P10	CSI1_D1+ / PCAM_D4					Not used
P11	CSI1_D1- / PCAM_D5					Not used
P12	GND				P	Ground
P13	CSI1_D2+ / PCAM_D6					Not used
P14	CSI1_D2- / PCAM_D7					Not used
P15	GND				P	Ground
P16	CSI1_D3+ / PCAM_D8					Not used
P17	CSI1_D3- / PCAM_D9					Not used
P18	GND				P	Ground

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P19	GbE_MDI3-				AIO	Qualcomm AR8035 Differential Transmit/Receive Negative Channel 3
P20	GbE_MDI3+				AIO	Qualcomm AR8035 Differential Transmit/Receive Positive Channel 3
P21	GbE_LINK100#				O OD	Link Speed Indication LED for 100Mbps Could be able to sink 24mA or more Carrier LED current
P22	GbE_LINK1000#				O OD	Link Speed Indication LED for 1000Mbps Could be able to sink 24mA or more Carrier LED current
P23	GbE_MDI2-				AIO	Qualcomm AR8035 Differential Transmit/Receive Negative Channel 2
P24	GbE_MDI2+				AIO	Qualcomm AR8035 Differential Transmit/Receive Positive Channel 2
P25	GbE_LINK_ACT#				O OD	GBE0 Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity Could be able to sink 24mA or more Carrier LED current

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P26	GbE_MDI1-				AIO	Qualcomm AR8035 Differential Transmit/Receive Negative Channel 1
P27	GbE_MDI1+				AIO	Qualcomm AR8035 Differential Transmit/Receive Positive Channel 1
P28	GbE_CTREF				O	Qualcomm AR8035 Center tap reference voltage for GBE Carrier board Ethernet magnetic
P29	GbE_MDI0-				AIO	Qualcomm AR8035 Differential Transmit/Receive Negative Channel 0
P30	GbE_MDI0+				AIO	Qualcomm AR8035: Differential Transmit/Receive Positive Channel 0

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P31	SPI0_CS1#	AC25	4	CAM1_FIELD__ SPI2_CS1	O	SPI0 Master Chip Select 1 output.
P32	GND				P	Ground
P33	SDIO_WP	G24	5	eCAP0_in_PWM0_ OUT__ MMC0_SDWP	I	Write Protect
P34	SDIO_CMD	D2	0	MMC0_CMD__ MMC0_CMD	IO	Command Line
P35	SDIO_CD#	R25	5	SPI0_CS1__ MMC0_SDCD	I	Card Detect
P36	SDIO_CK	D1	0	MMC0_CLK__ MMC0_CLK	O	Clock
P37	SDIO_PWR_EN	A16	5	RMII1_REFCLK__ MMC0_POW	O	SD card power enable
P38	GND				P	Ground
P39	SDIO_D0	C1	0	MMC0_DAT0__ MMC0_DAT0	IO	Data path
P40	SDIO_D1	C2	0	MMC0_DAT1__ MMC0_DAT1	IO	Data path
P41	SDIO_D2	B2	0	MMC0_DAT2__ MMC0_DAT2	IO	Data path
P42	SDIO_D3	B1	0	MMC0_DAT3__ MMC0_DAT3	IO	Data path
P43	SPI0_CS0#	AD25	4	CAM1_HD__ SPI2_CS0	O	SPI0 Master Chip Select 0 output, reserved for on-module NOR flash
P44	SPI0_CK	AE21	4	CAM1_PCLK__ SPI2_SCLK	O	SPI0 Master Clock output
P45	SPI0_DIN	AD24	4	CAM1_DATA8__ SPI2_D0	I	SPI0 Master Data input (input to CPU, output from SPI device)

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P46	SPI0_DO	AB25	4	CAM1_WEN__ SPI2_D1	O	SPI0 Master Data output (output from CPU, input to SPI device)
P47	GND				P	Ground
P48	SATA_TX+					Not used
P49	SATA_TX-					Not used
P50	GND				P	Ground
P51	SATA_RX+					Not used
P52	SATA_RX-					Not used
P53	GND				P	Ground
P54	SPI1_CS0#	N25	0	SPI4_CS0__ SPI4_CS0	O	SPI1 Master Chip Select 0 output
P55	SPI1_CS1#	H22	2	UART3_CTSN__ SPI4_CS1	O	SPI1 Master Chip Select 1 output
P56	SPI1_CK	P25	0	SPI4_SCLK__ SPI4_SCLK	O	SPI1 Master Clock output
P57	SPI1_DIN	R24	0	SPI4_D0__ SPI4_D0	I	SPI1 Master Data input (input to CPU, output from SPI device)
P58	SPI1_DO	P24	0	SPI4_D1__ SPI4_D1	O	SPI1 Master Data output (output from CPU, input to SPI device)
P59	GND				P	Ground

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P60	USB0+	W25		USB0_DP	IO	Differential USB0 data
P61	USB0-	W24		USB0_DM	IO	Differential USB0 data
P62	USB0_EN_OC#	G21 D16	0 9	USB0_DRVVBUS__ USB0_DRVVBUS GMII1_COL__ GPIO0[0]	IO OD	Pulled low by Module OD driver to disable USB0 power Pulled low by Carrier OD driver to indicate over-current situation If this signal is used, a pull-up is required on the Carrier
P63	USB0_VBUS_DET	U23		Turn on USB0_VBUS	I	USB host power detection, when this port is used as a device
P64	USB0_OTG_ID	U24	0	USB0_ID__ USB0_ID	I	USB OTG ID input, active high
P65	USB1+	V24		USB1_DP	IO	Differential USB0 data pair
P66	USB1-	V25		USB1_DM	IO	

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P67	USB1_EN_OC#	F25 A3	0 7	USB1_DRVVBUS __ USB1_DRVVBUS GPMC_BE1N__ GPIO1[28]	IO OD	Pulled low by Module OD driver to disable USB0 power Pulled low by Carrier OD driver to indicate over-current situation If this signal is used, a pull-up is required on the Carrier
P68	GND				P	Ground
P69	USB2+					Not used
P70	USB2-					Not used
P71	USB2_EN_OC#					Not used
P72	PCIE_C_PRSNT#					Not used
P73	PCIE_B_PRSNT#					Not used
P74	PCIE_A_PRSNT#					Not used
P75	PCIE_A_RST#					Not used
P76	PCIE_C_CKREQ#					Not used
P77	PCIE_B_CKREQ#					Not used
P78	PCIE_A_CKREQ#					Not used
P79	GND				P	Ground
P80	PCIE_C_REFCK+					Not used

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P81	PCIE_C_REFCK-					Not used
P82	GND				P	Ground
P83	PCIE_A_REFCK+					Not used
P84	PCIE_A_REFCK-					Not used
P85	GND				P	
P86	PCIE_A_RX+					Not used
P87	PCIE_A_RX-					Not used
P88	GND					Ground
P89	PCIE_A_TX+					Not used
P90	PCIE_A_TX-					Not used
P91	GND				P	Ground
P92	HDMI_D2+					Not used
P93	HDMI_D2-					TMDS / HDMI Not used

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P94	GND				P	Ground
P95	HDMI_D1+					Not used
P96	HDMI_D1-					Not used
P97	GND				P	Ground
P98	HDMI_D0+					Not used
P99	HDMI_D0-					Not used
P100	GND				P	Ground
P101	HDMI_CK+					Not used
P102	HDMI_CK-					Not used
P103	GND				P	Ground
P104	HDMI_HPD					Not used
P105	HDMI_CTRL_CK					Not used
P106	HDMI_CTRL_DAT					Not used
P107	HDMI_CEC					HDMI Consumer Electronics Control 1 – wire peripheral control interface

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P108	GPIO0 / CAM0_PWR#	T23	9	SPI2_CS0__ GPIO0[23]	IO	Camera 0 Power Enable, active low output
P109	GPIO1 / CAM1_PWR#	P22	9	SPI2_D0__ GPIO0[20]	IO	Camera 1 Power Enable, active low output
P110	GPIO2 / CAM0_RST#	P20	9	SPI2_D1__ GPIO0[21]	IO	Camera 0 Reset, active low output
P111	GPIO3 / CAM1_RST#	N20	9	SPI2_SCLK__ GPIO0[22]	IO	Camera 1 Reset, active low output
P112	GPIO4 / HDA_RST#	AD19	7	CAM0_DATA5__ GPIO4[27]	IO	HD Audio Reset, active low output
P113	GPIO5 / PWM_OUT	AD20	7	CAM0_DATA7__ GPIO4[29]	IO	PWM output
P114	GPIO6 / TACHIN	M24	7	MCASP0_AHCLKR __ GPIO3[17]	IO	Tachometer input (used with the GPIO5 PWM)
P115	GPIO7 / PCAM_FLD	H23	7	MCASP0_AXR0_ _ GPIO3[16]	IO	PCAM_FLD (Field) signal input
P116	GPIO8 / CAN0_ERR#	Y18	7	CAM0_DATA2 GPIO4[24]	IO	CAN0 Error signal, active low input
P117	GPIO9 / CAN1_ERR#	AA18	7	CAM0_DATA3 GPIO4[25]	IO	CAN1 Error signal, active low input
P118	GPIO10	AE19	7	CAM0_DATA4 GPIO4[26]	IO	
P119	GPIO11	AE20	7	CAM0_DATA6 GPIO4[28]	IO	
P120	GND				P	

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P121	I2C_PM_CK	B13	3	GMII1_RXER__ I2C1_SCL	IO OD	Power management I2C bus clock
P122	I2C_PM_DAT	B14	3	GMII1_CRS__ I2C1_SDA	IO OD	Power management I2C bus data
P123	BOOT_SEL0#	D25	7	GPIO5[8]__ GPIO5[8]	I	SYSBOOT and Line De-multiplexer Logic Pulled up on Module. Driven by OD part on Carrier.
P124	BOOT_SEL1#	F24	7	GPIO5[9]__ GPIO5[9]	I	SYSBOOT and Line De-multiplexer Logic Pulled up on Module. Driven by OD part on Carrier.
P125	BOOT_SEL2#	G20	7	GPIO5[10]__ GPIO5[10]	I	SYSBOOT and Line De-multiplexer Logic Pulled up on Module. Driven by OD part on Carrier.
P126	RESET_OUT#				O	General purpose reset output to Carrier board.

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P127	RESET_IN#				I	Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise Pulled up on Module. Driven by OD part on Carrier.
P128	POWER_BTN#	F23			I	Power-button input from carrier board. Carrier to float the line in in-active state. Active low, level sensitive. It is de-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.
P129	SER0_TX	J24	0	UART0_TXD__ UART0_TXD	O	Asynchronous serial port data out
P130	SER0_RX	K25	0	UART0_RXD__ UART0_RXD	I	Asynchronous serial port data in
P131	SER0_RTS#	J25	0	UART0_RTSN__ UART0_RTSN	O	Request to Send handshake line for SER0
P132	SER0_CTS#	L25	0	UART0_CTSN__ UART0_CTSN	I	Clear to Send handshake line for SER0
P133	GND				P	Ground
P134	SER1_TX	H24	0	UART3_TXD__ UART3_TXD	O	Asynchronous serial port data out
P135	SER1_RX	H25	0	UART3_RXD__ UART3_RXD	I	Asynchronous serial port data in

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P136	SER2_TX	AE23	2	CAM1_DATA5__ UART2_TXD		Asynchronous serial port data out
P137	SER2_RX	AD22	2	CAM1_DATA4__ UART2_RXD		Asynchronous serial port data in
P138	SER2_RTS#	AE24	2	CAM1_DATA7__ UART2_RTSN		Request to Send handshake line for SER2
P139	SER2_CTS#	AD23	2	CAM1_DATA6__ UART2_CTSN		Clear to Send handshake line for SER2
P140	SER3_TX	B3	6	GPMC_WPN__ UART4_TXD	O	Asynchronous serial port data out
P141	SER3_RX	A2	6	GPMC_WAIT0__ UART4_RXD	I	Asynchronous serial port data in
P142	GND				P	Ground
P143	CAN0_TX	K22	2	UART1_CTSN__ DCAN0_TX	O	CAN0 Transmit output
P144	CAN0_RX	L22	2	UART1_RTSN__ DCAN0_RX	I	CAN0 Receive input
P145	CAN1_TX	K21	2	UART1_RXD__ DCAN1_TX	O	CAN1 Transmit output
P146	CAN1_RX	L21	2	UART1_TXD__ DCAN1_RX	I	CAN1 Receive input

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P147	VDD_IN				P	Power in
P148	VDD_IN				P	Power in
P149	VDD_IN				P	Power in
P150	VDD_IN				P	Power in
P151	VDD_IN				P	Power in
P152	VDD_IN				P	Power in
P153	VDD_IN				P	Power in
P154	VDD_IN				P	Power in
P155	VDD_IN				P	Power in
P156	VDD_IN				P	Power in

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S1	PCAM_VSYNC					Not used
S2	PCAM_HSYNC					Not used
S3	GND				P	Ground
S4	PCAM_PXL_CK0					Not used
S5	I2C_CAM_CK					Not used
S6	CAM_MCK	C24	3	XDMA_EVENT_INTR1__ CCM_CLKO2	O	Master clock output for CSI camera support
S7	I2C_CAM_DAT					Not used
S8	CSI0_CK+ / PCAM_D10					Not used
S9	CSI0_CK- / PCAM_D11					Not used
S10	GND				P	Ground
S11	CSI0_D0+ / PCAM_D12					Not used
S12	CSI0_D0- / PCAM_D13					Not used
S13	GND				P	Ground
S14	CSI0_D1+ / PCAM_D14					Not used
S15	CSI0_D1- / PCAM_D15					Not used
S16	GND				P	Ground

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S17	AFB0_OUT					Center tap reference voltage
S18	AFB1_OUT	AA12	0	ADC0_AIN0__ ADC0_AIN0	AI	XP: Plus X-axis on-off control signal
S19	AFB2_OUT	Y13	0	ADC0_AIN2__ ADC0_AIN2	AI	YP: Plus Y-axis on-off control signal
S20	AFB3_IN					Not used
S21	AFB4_IN	Y12	0	ADC0_AIN1__ ADC0_AIN1	AI	XM: Minus X-axis on-off control signal
S22	AFB5_IN	AA13	0	ADC0_AIN3__ ADC0_AIN3	AI	YM: Minus Y-axis on-off control signal
S23	AFB6_PTIO				O OD	Link Speed Indication LED for 100Mbps GBE_1_ LINK100#: Could be able to sink 24mA or more Carrier LED current
S24	AFB7_PTIO				O OD	Link Speed Indication LED for 1000Mbps GBE_1_ LINK1000#: Could be able to sink 24mA or more Carrier LED current
S25	GND				P	Ground

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S26	SDMMC_D0	E11	3	GPMC_AD12__ MMC2_DAT0	IO	8-bit eMMC Data 0
S27	SDMMC_D1	C11	3	GPMC_AD13__ MMC2_DAT1	IO	8-bit eMMC Data 1
S28	SDMMC_D2	B11	3	GPMC_AD14__ MMC2_DAT2	IO	8-bit eMMC Data 2
S29	SDMMC_D3	A11	3	GPMC_AD15__ MMC2_DAT3	IO	8-bit eMMC Data 3
S30	SDMMC_D4	B10	3	GPMC_AD8__ MMC2_DAT4	IO	8-bit eMMC Data 4
S31	SDMMC_D5	A10	3	GPMC_AD9__ MMC2_DAT5	IO	8-bit eMMC Data 5
S32	SDMMC_D6	F11	3	GPMC_AD10__ MMC2_DAT6	IO	8-bit eMMC Data 6
S33	SDMMC_D7	D11	3	GPMC_AD11__ MMC2_DAT7	IO	8-bit eMMC Data 7
S34	GND					Ground
S35	SDMMC_CK	A12	3	GPMC_CLK__ MMC2_CLK	O	SDMMC Clock Signal
S36	SDMMC_CMD	B12	3	GPMC_CSN3__ MMC2_CMD	O	SDMMC Command signal
S37	SDMMC_RST#	N22	7	MCASP0_FSX__ GPIO3[15]	O	Reset signal to eMMC device

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S38	AUDIO_MCK	D24	3	XDMA_EVENT_INTR0__ CLKOUT1	O	Master clock output to Audio codecs
S39	I2S0_LRCK	K23	3	MCASP0_FSR__ MCASP1_FSX	IO	Left& Right audio synchronization clock
S40	I2S0_SDOUT	M25	3	MCASP0_AXR1_ _ MCASP1_AXR0	O	Digital audio Output
S41	I2S0_SDIN	L24	3	MCASP0_AHCLKX__ MCASP1_AXR1	I	Digital audio Input
S42	I2S0_CK	L23	3	MCASP0_ACLKR __ MCASP1_ACLKX	IO	Digital audio clock
S43	I2S1_LRCK					Not used
S44	I2S1_SDOUT					Not used
S45	I2S1_SDIN					Not used
S46	I2S1_CK					Not used
S47	GND				G	Ground

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S48	I2C_GP_CK	Y22	0	I2C0_SCL__ I2C0_SCL	IO OD	Port1 of TCA9546 General purpose I2C bus clock
S49	I2C_GP_DAT	AB24	0	I2C0_SDA__ I2C0_SDA	IO OD	Port1 of TCA9546 General purpose I2C bus clock
S50	I2S2_LRCK					Not used
S51	I2S2_SDOUT					Not used
S52	I2S2_SDIN					Not used
S53	I2S2_CK					Not used
S54	SATA_ACT#					Not used
S55	AFB8_PTIO				O OD	GBE1 Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity Could be able to sink 24mA or more Carrier LED current
S56	AFB9_PTIO					Not used
S57	PCAM_ON_CSI0#					Not used
S58	PCAM_ON_CSI1#					Not used
S59	SPDIF_OUT					Not used
S60	SPDIF_IN					Not used
S61	GND				P	Ground

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S62	AFB_DIFF0+				AIO	GBE1_MDI0+: Bi-directional transmit/receive pair 0 to magnetics (Media Dependent Interface) for AFB 2nd GBE, Qualcomm AR8035 Differential Transmit/Receive Positive Channel 0
S63	AFB_DIFF0-				AIO	GBE1_MDI0-: Bi-directional transmit/receive pair 0 to magnetics (Media Dependent Interface) for AFB 2nd GBE, Qualcomm AR8035: Differential Transmit/Receive Negative Channel 0
S64	GND					

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S65	AFB_DIFF1+				AIO	GBE1_MDI1+: Bi-directional transmit/receive pair 1 to magnetics (Media Dependent Interface) for AFB 2nd GBE, Qualcomm AR8035: Differential Transmit/Receive Positive Channel 1
S66	AFB_DIFF1-				AIO	GBE1_MDI1-: Bi-directional transmit/receive pair 1 to magnetics (Media Dependent Interface) for AFB 2nd GBE, Qualcomm AR8035: Differential Transmit/Receive Negative Channel 1
S67	GND					

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S68	AFB_DIFF2+				AIO	GBE1_MDI2+: Bi-directional transmit/receive pair 1 to magnetics (Media Dependent Interface) for AFB 2nd GBE, Qualcomm AR8035: Differential Transmit/Receive Positive Channel 2
S69	AFB_DIFF2-				AIO	GBE1_MDI2-: Bi-directional transmit/receive pair 1 to magnetics (Media Dependent Interface) for AFB 2nd GBE, Qualcomm AR8035: Differential Transmit/Receive Negative Channel 2
S70	GND				P	Ground

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S71	AFB_DIFF3+				AIO	GBE1_MDI2+: Bi-directional transmit/receive pair 1 to magnetics (Media Dependent Interface) for AFB 2nd GBE, Qualcomm AR8035: Differential Transmit/Receive Positive Channel 3
S72	AFB_DIFF3-				AIO	GBE1_MDI2-: Bi-directional transmit/receive pair 1 to magnetics (Media Dependent Interface) for AFB 2nd GBE, Qualcomm AR8035: Differential Transmit/Receive Negative Channel 3
S73	GND				P	Ground

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S74	AFB_DIFF4+					Not used
S75	AFB_DIFF4-					Not used
S76	PCIE_B_RST#					Not used
S77	PCIE_C_RST#					Not used
S78	PCIE_C_RX+					Not used
S79	PCIE_C_RX-					Not used
S80	GND				P	Ground
S81	PCIE_C_TX+					Not used
S82	PCIE_C_TX-					Not used
S83	GND				P	Ground
S84	PCIE_B_REFCK+					Not used
S85	PCIE_B_REFCK-					Not used
S86	GND				P	Ground
S87	PCIE_B_RX+					Not used
S88	PCIE_B_RX-					Not used
S89	GND				P	Ground
S90	PCIE_B_TX+					Not used
S91	PCIE_B_TX-					Not used
S92	GND				P	Ground

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S93	LCD_D0	B22	0	DSS_DATA0__ DSS_DATA0	O	8 bit BLU color data - 18 bit display implementations leave the two LS bits (D0, D1) not connected
S94	LCD_D1	A21	0	DSS_DATA1__ DSS_DATA1	O	
S95	LCD_D2	B21	0	DSS_DATA2__ DSS_DATA2	O	
S96	LCD_D3	C21	0	DSS_DATA3__ DSS_DATA3	O	
S97	LCD_D4	A20	0	DSS_DATA4__ DSS_DATA4	O	
S98	LCD_D5	B20	0	DSS_DATA5__ DSS_DATA5	O	
S99	LCD_D6	C20	0	DSS_DATA6__ DSS_DATA6	O	
S100	LCD_D7	E19	0	DSS_DATA7__ DSS_DATA7	O	
S101	GND				P	Ground

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S102	LCD_D8	A19	0	DSS_DATA8__ DSS_DATA8	O	8 bit GRN color data - 18 bit display implementations leave the two LS bits (D8, D9) not connected
S103	LCD_D9	B19	0	DSS_DATA9__ DSS_DATA9	O	
S104	LCD_D10	A18	0	DSS_DATA10__ DSS_DATA10	O	
S105	LCD_D11	B18	0	DSS_DATA11__ DSS_DATA11	O	
S106	LCD_D12	C19	0	DSS_DATA12__ DSS_DATA12	O	
S107	LCD_D13	D19	0	DSS_DATA13__ DSS_DATA13	O	
S108	LCD_D14	C17	0	DSS_DATA14__ DSS_DATA14	O	
S109	LCD_D15	D17	0	DSS_DATA15__ DSS_DATA15	O	
S110	GND				P	Ground

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S111	LCD_D16	AC24	2	CAM1_DATA9__ DSS_DATA16	O	8 bit RED color data - 18 bit display implementations leave the two LS bits (D16, D17) not connected
S112	LCD_D17	AA19	2	CAM0_DATA9__ DSS_DATA17	O	
S113	LCD_D18	AB19	2	CAM0_DATA8__ DSS_DATA18	O	
S114	LCD_D19	AC20	2	CAM0_PCLK__ DSS_DATA19	O	
S115	LCD_D20	AD17	2	CAM0_WEN__ DSS_DATA20	O	
S116	LCD_D21	AC18	2	CAM0_FIELD__ DSS_DATA21	O	
S117	LCD_D22	AD18	2	CAM0_VD__ DSS_DATA22	O	
S118	LCD_D23	AE17	2	CAM0_HD__ DSS_DATA23	O	
S119	GND				P	Ground
S120	LCD_DE	A24	0	DSS_AC_BIAS_EN__ DSS_AC_BIAS_EN	O	Display Enable- signal is high during the active display line; low otherwise
S121	LCD_VS	B23	0	DSS_VSYNC__ DSS_VSYNC	O	Vertical Sync- high pulse indicates the start of a new display frame
S122	LCD_HS	A23	0	DSS_HSYNC__ DSS_HSYNC	O	Horizontal Sync - high pulse indicates the start of a new horizontal display line

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S123	LCD_PCK	A22	0	DSS_PCLK__ DSS_PCLK	O	Pixel clock - display data transitions on the positive clock edge
S124	GND				P	Ground
S125	LVDS0+					Not used
S126	LVDS0-					Not used
S127	LCD_BKLT_EN	D10	7	GPMC_WEN__ GPIO2[4]	O	High enables panel backlight
S128	LVDS1+					Not used
S129	LVDS1-					Not used
S130	GND				P	Ground
S131	LVDS2+					Not used
S132	LVDS2-					Not used
S133	LCD_VDD_EN	C10	7	GPMC_BE0N_CLE__ GPIO2[5]	O	High enables panel VDD
S134	LVDS_CK+					Not used
S135	LVDS_CK-					Not used
S136	GND				P	Ground
S137	LVDS3+					Not used
S138	LVDS3-					Not used

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S139	I2C_LCD_CK	AC21	3	CAM1_DATA1__ I2C2_SCL	IO OD	LCD display I2C bus clock
S140	I2C_LCD_DAT	AB20	3	CAM1_DATA0__ I2C2_SDA	IO OD	LCD display I2C bus clock
S141	LCD_BKLT_PWM	AC23	6	GAM1_VD__ EHRPWM0B	O	Display backlight PWM control
S142	LCD_DUAL_PCK					Not used
S143	GND				P	Ground
S144	RSVD / EDP_HPD					Not used
S145	WDT_TIME_OUT#	K24	6	UART3_RTSN__ EHRPWM5B	O	Watchdog Timer Output
S146	PCIE_WAKE#					Not used

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S147	VDD_RTC				P	Low current RTC circuit backup power - 3.0V nominal It is sourced from a Carrier based Lithium cell or Super Cap
S148	LID#	A8	7	GPMC_CSN0__ GPIO1[29]	I	Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.
S149	SLEEP#	E10	7	GPMC_OEN_REN__ GPIO2[3]	I	Sleep indicator from Carrier board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module. Pulled up on Module. Driven by OD part on Carrier.

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S150	VIN_PWR_BAD#				I	Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) shall not be enabled while this signal is held low by the Carrier. Pulled up on Module. Driven by OD part on Carrier.
S151	CHARGING#	AE18	7	CAM0_DATA0__ GPIO5[19]	I	Held low by Carrier if DC input for battery charger is present. Pulled up on Module. Driven by OD part on Carrier.
S152	CHARGER_PRSNT#	E24	7	GPIO5[13]__ GPIO5[13]	I	
S153	CARRIER_STBY#	A9	7	GPMC_ADVN_ALE__ GPIO2[2]	O	The Module shall drive this signal low when the system is in a standby power state

SMARC Edge Finger		TI T4378 CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S154	CARRIER_PWR_ON				O	Carrier board circuits (apart from power management and power path circuits) should not be powered up until the Module asserts the CARRIER_PWR_ ON signal.
S155	FORCE_RECOV#	E25	7	GPIO5[12]__ GPIO5[12]	I	Pulled up on Module. Driven by OD part on Carrier.
S156	BATLOW#	AB18	7	CAM0_DATA1__ GPIO5[20]	I	Battery low indication to Module. Carrier to float the line in in-active state. Pulled up on Module. Driven by OD part on Carrier.
S157	TEST#				I	Held low by Carrier to invoke Module SD Boot UP. Pulled up on Module. Driven by OD part on Carrier.
S158	VDD_IO_SEL#				IO	If the Carrier supports only 1.8V I/O, then the Carrier shall tie the VDD_IO_SEL# pin directly to GND. Otherwise floating this pin.

Chapter 4

Power Control Signals between SMARC Module and Carrier

This Chapter points out the handshaking rule between *SMARC* module and carrier.
Section include：

- *SMARC-T4378* Module Power
- Power Signals
- Power Flow and Control Signals Block Diagram
- Power States
- Power Sequences
- Terminations
- Boot Select

Chapter 4 Power Control Signals between SMARC-T4378 Module and Carrier

SMARC modules are designed to be driven with a single *+3V* to *+5.25V* input power rail. A *+5V* is recommended for non-battery operated systems. Unlike Q7 module, there is no separate voltage rail for standby power, other than the very low current RTC voltage rail. All module operating and standby power comes from the single set of *VDD_IN* pins. This suits battery power sources well, and is also easy to use with non-battery sources.

SMARC module has specific handshaking rules to the carrier by *SMARC* hardware specification. To design the carrier board, users need to follow these rules or it might not boot up. Some pull-up and pull-down also need to be cared to make all functions work.

4.1 SMARC-T4378 Module Power

4.1.1. Input Voltage / Main Power Rail

The allowable Module DC input voltage range for *SMARC-T4378* is from 3.0V to 5.25V. This voltage is brought in on the *VDD_IN* pins and returned through the numerous *GND* pins on the connector. A single 5V DC input is recommended if device is not operated by battery.

Ten pins are allocated to *VDD_IN*. The connector pin current rating is 0.5A per pin. This works out to 5A total for the 10 pins. At the lowest allowed Module input voltage, this would allow up to 16.75W of electrical power to be brought in (with no de-rating on the connector current capability). With a 40% connector current de-rating, up to 10W may be brought in at 3V.
SMARC-T4378 typically consumes 1.5~4W depending on solo or quad cores and is pretty safe in using the connector.

4.1.2. No Separate Standby Voltage

There is no separate voltage rail for standby power, other than the very low

current RTC voltage rail. *SMARC-T4378* operating and standby power comes from the single set of *VDD_IN* pins. This suits battery power sources well, and is also easy to use with non-battery sources.

4.1.3. RTC/Backup Voltage

RTC backup power is brought in on the *VDD_RTC* rail. The RTC consumption is typically 15 microA or less. The allowable *VDD_RTC* voltage range shall be 2.0V to 3.25V. The *VDD_RTC* rail is sourced from a Carrier based Lithium cell, or it may be left open if the RTC backup functions are not required. *SMARC-T4378* module is able to boot without a *VDD_RTC* voltage source.

Lithium cells, if used on Carrier, shall be protected against charging by a Carrier Schottky diode. The diode is placed in series with the positive battery terminal. The diode anode is on the battery side, and the cathode on the Module *VDD_RTC* side.

Note that if a Super cap is used, current may flow out of the Module *VDD_RTC* rail to charge the Super Cap.

4.1.4. Power Sequencing

The Module signal *CARRIER_PWR_ON* exists to ensure that the Module is powered before the main body of Carrier circuits (those outside the power and power control path on the Carrier). The main body of Carrier board circuits should not be powered until the Module asserts the *CARRIER_PWR_ON* signal as a high. Module hardware will assert *CARRIER_PWR_ON* when all Module supplies necessary for Module booting are up.

The IO power of carrier board will be turn on at the stage of power on sequence. If the IO power of carrier board been turn on earlier than the *SMARC* module, the power on carrier board might feedback to *SMARC* module through IO lines and disturbs the *SMARC* module power on sequence. More seriously, it might cause to the CPU won't boot up. It is always recommended that the power on module has to be earlier than that on carrier board.

The boot up of module depends on when you release the reset signal of your carrier board. The module will boot up when the reset signal on your carrier board is released. Before that, the module will not boot up. That's

why designer needs to put the *RESET_IN#* in the last stage of power to serve as the "*power good*" signal of the carrier board.

The module will not boot up till the module power is ready because the carrier board hasn't released the reset signal yet.

The sequence is as follows:

Module Power Ready --> *CARRIER_POWER_ON* -->*RESET_IN#* -->*Boot Up*

4.1.5. RESET_IN#

The *SMARC* module does not know the IO power status from the carrier board, and put *RESET_IN#* in the last stage of power can serve as the "*power good*" signal of carrier board. This also assures that the power of carrier board is good when *SMARC* module booting up.

4.1.6. VDD_IO

SMARC 1.0 specification defines the I/O voltage to be 1.8V or 3.3V or both. The 3.3V *VDD_IO* is depreciated from *SMARC* 1.1 specification. However, many users still preferred 3.3V *VDD_IO* because it is easier for carrier design.

SMARC-T4378 supports **both** *1.8V* and *3.3V VDD_IO*. If the Carrier supports only 1.8V I/O, then the Carrier will tie the *VDD_IO_SEL#* pin directly to GND. If the Carrier supports only 3.3V *VDD_IO*, Carriers will float the signal for 3.3V.
3.3V SMARC-T4378 will not power up if module senses a 1.8V *VDD_IO* Carrier on the *VDD_IO_SEL#* (due to the Carrier pulling the line down) to protect the module. It will cut the module power down if *VDD_IO_SEL#* is connected to GND (this is the case of 1.8V *SMARC* module).

4.1.7. Power Bad Indication (VIN_PWR_BAD#)

Power bad indication is from carrier board and is an input signal for Module. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) will not be enabled while this signal is held low by the Carrier.
This signal has a *100K* pull-up on module and is driven by *OD* part on

Carrier.

4.1.8. System Power Domains

It is useful to describe an *SMARC* system as being divided into a hierarchy of three power domains:
1) Battery Charger power domain (can be neglected if the system is not battery powered only)
2) *SMARC* Module power domain
3) Carrier Circuits power domain
The Battery Charger domain includes circuits that are active whenever either charger input power and / or battery power are available. These circuits may include power supply supervisor(s), battery chargers, fuel gauges and, depending on the battery configuration, switching power section(s) to step down a high incoming battery voltage.
The *SMARC* Module domain includes the *SMARC* module.
The Carrier Circuits domain includes “everything else” (and does not include items from the Battery Charger and Module domain, even though they may be mounted on the Carrier).
This is illustrated in the figure below.

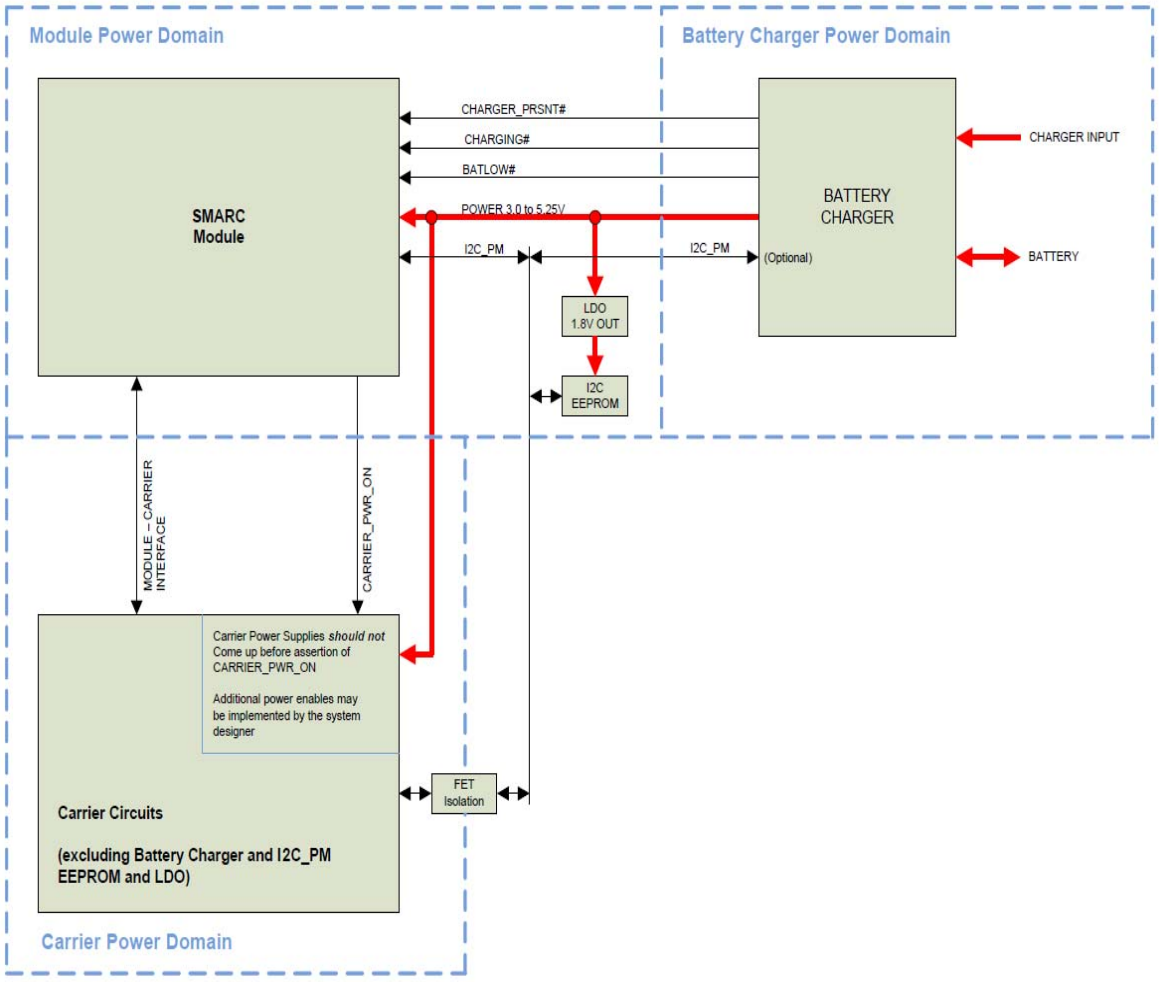


Figure 21 System Power Domains

4.2 Power Signals

4.2.1. Power Supply Signals

SMARC Edge Finger		I/O	Type	Power Rail	Description
Pin#	Pin Name				
P147, P148, P149, P150, P151,P152, P153, P154, P155, P156	VDD_IN	I	PWR	3.0V~5.25V[1]	Main power supply input for the module
P2, S3, P9, S10, P12, S13, P15, S16, P18, S25, P32, S34, P38, S47, P47, P50, P53, P59, S61, S64, S67, P68, S70, S73, P79, S80, P82, S83, P85, S86,P88, S89, P91, S92, P94, P97, P100, S101, P103, S110, S119, P120, S124, S130, P133, S136, P142, S143	GND	I	PWR		Common signal and power ground
S147	VDD_RTC	I	PWR	3.3V	RTC supply, can be left unconnected if internal RTC is not used

Note: 5V is recommended for non-battery operated system.

4.2.2. Power Control Signals

The input pins listed in the following table are all active low and are meant to be driven by OD (open drain) devices on the Carrier. The Carrier either floats the line or drives it to *GND*. No Carrier pull-ups are needed. The pull-up functions are performed on the Module. The voltage rail that these lines are pulled to on the Module varies, depending on the design, and may be *3.3V* or *VDD_IN*.

SMARC Edge Finger		I/O	Type	Power Rail	Description
Pin#	Pin Name				
S150	VIN_PWR_BAD#	I	CMOS	VDD_IN	Power bad indication from Carrier board
S154	CARRIER_PWR_ON	O	CMOS	VDD_IO	Signal to inform Carrier board circuits being powered up
P126	RESET_OUT#	O	CMOS	VDD_IO	General purpose reset output to Carrier board.
P127	RESET_IN#	I	CMOS	VDD_IO	Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise. Pulled up on Module. Driven by OD part on Carrier.
S158	VDD_IO_SEL#	IO	Strap	VDD_IN	A low logic level on this signal indicates that the Module VDD_IO level is configured for the default level of 1.8V; a high value indicates that the Module is configured for 3.3V VDD_IO. Pullup to VDD_IN rail through a resistance of 100K on module
P128	POWER_BTN#	I	CMOS	VDD_IO	Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. It is de-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.

4.2.3. Power Management Signals

The pins listed in the following table are related to power management. They will be used in a battery-operated system.

SMARC Edge Finger		I/O	Type	Power Rail	Description
Pin#	Pin Name				
S156	BATLOW#	I	CMOS	VDD_IO	Battery low indication to Module. Carrier to float the line in in-active state. Pulled up on Module. Driven by OD part on Carrier.
S154	CARRIER_PWR_ON	O	CMOS	VDD_IO	Signal to inform Carrier board circuits being powered up
S153	CARRIER_STBY#	O	CMOS	VDD_IO	Module will drive this signal low when the system is in a standby power state
S152	CHARGER_PRSNT#	I	CMOS	VDD_IO	Held low by Carrier if DC input for battery charger is present. Pulled up on Module. Driven by OD part on Carrier.
S151	CHARGING#	I	Strap	VDD_IO	Held low by Carrier during battery charging. Carrier to float the line when charge is complete. Pulled up on Module. Driven by OD part on Carrier.

SMARC Edge Finger		I/O	Type	Power Rail	Description
Pin#	Pin Name				
S149	SLEEP#	I	CMOS	VDD_IO	Sleep indicator from Carrier board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module. Pulled up on Module. Driven by OD part on Carrier.
S148	LID#	I	CMOS	VDD_IO	Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.

4.2.4. Special Control Signals (TEST#)

SMARC-T4378 module boots up from an onboard *NOR* Flash first. The *u-boot* in this *SPI NOR* flash will read the *BOOT_SEL* configuration and decides where to load the *kernel zImage*.
In some situations like the *u-boot* in *NOR* flash needed to be upgrade or at factory default where the firmware in *NOR* flash is empty or at development stage that the *u-boot* in *NOR* needs to be modified, users will need an alternative way to boot up from *SD* card first. The *TEST#* pin serves as this purpose. The *TEST#* pin is pulled high on module. If carrier board leaves this pin floating or pulls high, the module will boot up from *SPI NOR*. If carrier board pulls this pin to *GND*, the module will boot up from *SD* card. The first stage bootloader in *AM4378 CPU ROM* codes will load the 2nd stage bootloader (*MLO*) based on the setting of this #*TEST* pin (*S157*).

4.3 Power Flow and Control Signals Block Diagram

Following figures shows the power flow and control signals block diagram.

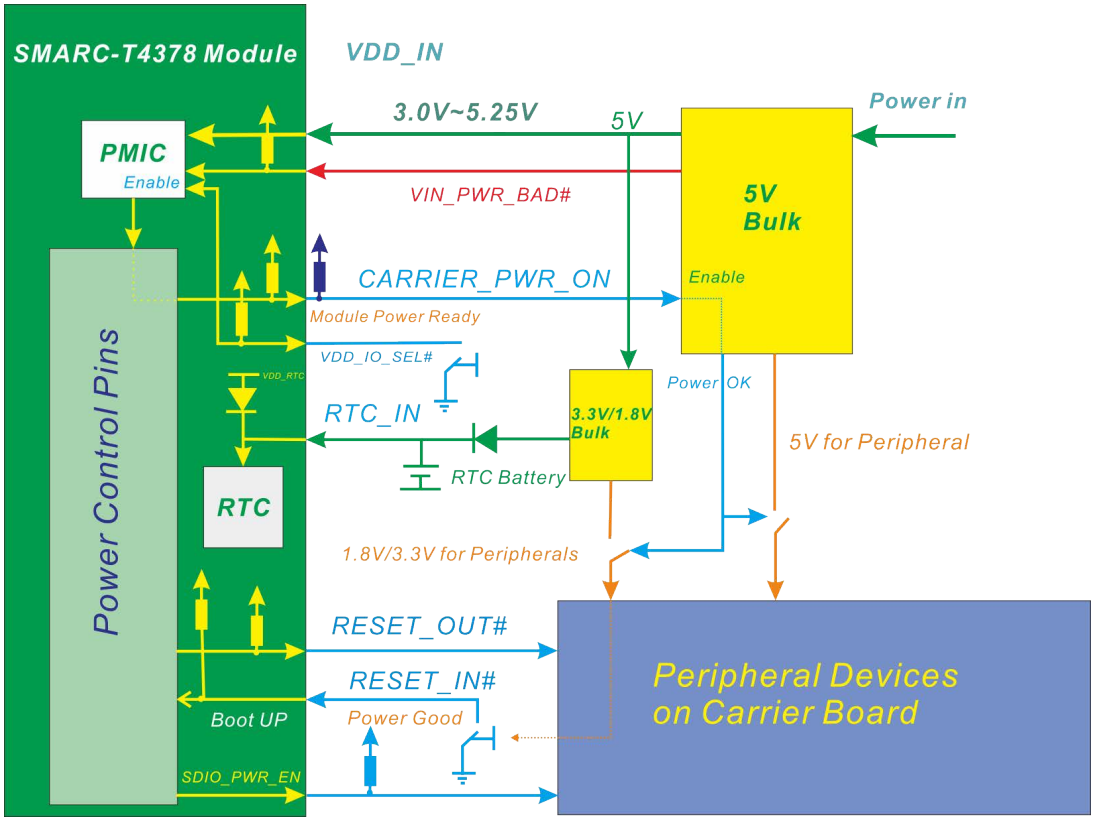


Figure 22: Power Block Diagram

When main power is supplied from the carrier, a voltage detector will assert *VIN_PWR_BAD#* signal to tell the module and carrier that the power is good. *VDD_IO_SEL#* will be floating on carrier that represents a 3.3V *VDD_IO* carrier or connecting to GND on carrier for 1.8V *VDD_IO*. These two signals will turn on the PMIC on module to power on the module. If *SMARC-T4378* supports 3.3V I/O only, the carrier needs to float *VDD_IO_SEL#* pin. The module will not power up if the module senses a low level on the *VDD_IO_SEL#* (due to the carrier pulling the line down) and the Module supports only 3.3V I/O or receives a low-active *VIN_PWR_BAD#* signal.

Carrier power circuits in the carrier Power domain should not power up unless the module asserts *CARRIER_PWR_ON*. The module signal *CARRIER_PWR_ON* exists to ensure that the module is powered before the main body of carrier circuits (those outside the power and power control path on the carrier).

The main body of carrier board circuits will not be powered until the module asserts the *CARRIER_PWR_ON* and *VDD_IO_SEL#* signals being correct. Module hardware will assert *CARRIER_PWR_ON and VDD_IO_SEL#* when all power supplies necessary for module booting are ready. The module will continue to assert signal *RESET_OUT#* after the release of *CARRIER_PWR_ON*, for a period sufficient to allow carrier power circuits to come up. When Carrier power is ready, it will assert *RESET_IN#* to inform module booting up.

If users would like to have SD boot up, *SDIO_PWR_EN* signal have to be pull up to 3.3V on carrier.

Module and carrier power supplies will not be enabled if the *VIN_PWR_BAD#* is held low by carrier. It is a power bad indication signal from carrier and is 100k pull up to *VDD_IN* on module.

4.4 Power States

The *SMARC-T4378* module supports different power states. The table below describes the behavior in the different states and which power rails and peripherals are active. Additional power states can be implemented if required using available *GPIO*s to control additional power domains and peripherals.

Abbr.	Name	Description	Module	Carrier Board
UPG	Unplugged	No power is applied to the system, except the RTC battery might be available	No main VDD_IN applied from fixed DC supply, VDD_IN available if backup battery is implemented	No power supply input, RTC battery maybe inserted
OFF	off	System is off, but the carrier board input supply is available	The main VDD_IN is available, but the CPU and peripherals are not running. Only the PMIC is running	Carrier board provides power for module, the peripheral supplies are not available
SUS	Suspend	System is suspended and waits for wakeup sources to trigger	CPU is suspended, wakeup capable peripherals are running while others might be switched off	Power rails are available on carrier board, peripherals might be stopped by software
RUN	Running	System is running	All power rails are available, CPU and peripherals are running	All power rails are available, peripherals are running
RST	Reset	System is put in reset state by holding RESET_IN# is low	All power rails are available, CPU and peripherals are in reset state	All power rails are available, peripherals are in reset state

The figure below shows a sequence diagram for the different power states. The module automatically enters into the running mode when the main power rail is applied to the module. In the running mode, the system can be set to suspend by software. There might be different wake up sources available. Consult the datasheet for *SMARC-T4378* module for more information about the available wakeup events.

In the running state, a shutdown request can be triggered by software. This turns off all power rails on the module and requests the carrier board to switch of the power rails for the peripherals. The module can be brought back to the

running mode in two ways. The module main voltage rail (*VDD_IN*) can be removed and applied again. If needed, this could also be done with a button and a small circuit. *SMARC-T4378* module supports being power cycled by asserting the *RESET_IN#* signal (e.g. by pressing the reset button or shunt and relief the reset jumper), please consult the associated module datasheet for more information about the support power cycle methods.

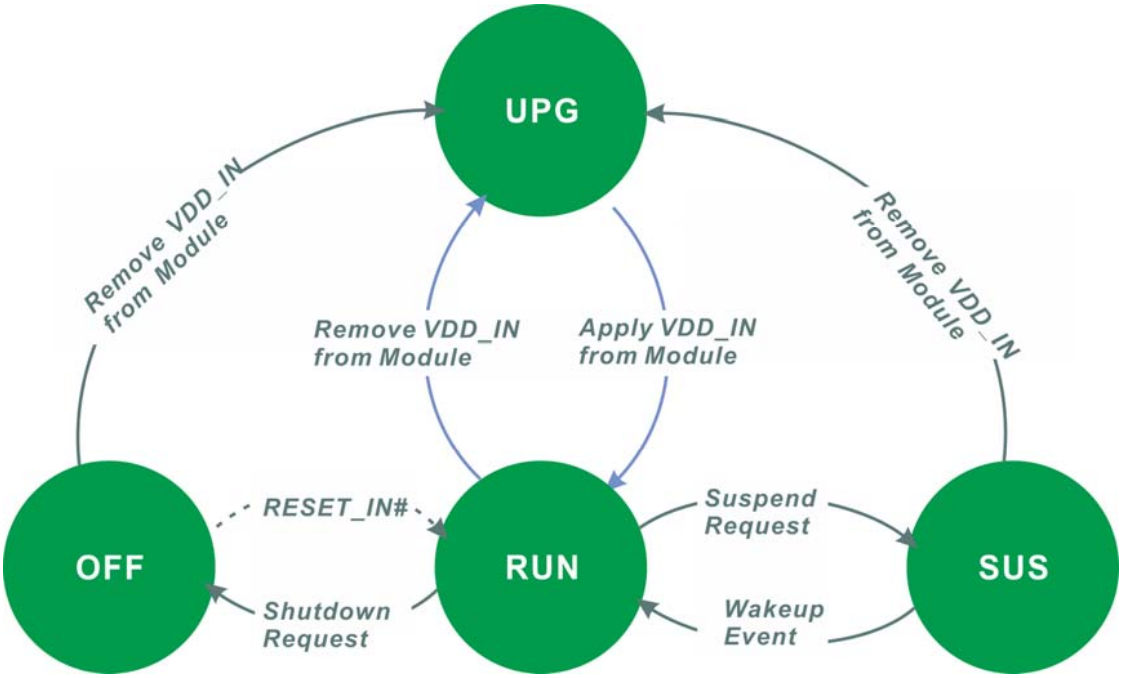


Figure 23: Power States and Transitions

4.5 Power Sequences

When main power is supplied from the carrier, a voltage detector will assert *VIN_PWR_BAD#* signal to tell the module and carrier that the power is good. *VDD_IO_SEL#* will be floating on carrier that represents a 3.3V *VDD_IO* carrier and connecting to *GND* on carrier that represents a 1.8V *VDD_IO*. These two signals will enable the PMIC on module to power on the module. The module will not power up if the module senses an incorrect voltage level on the *VDD_IO_SEL#* or receives a low-active *VIN_PWR_BAD#* signal.

The *SMARC-T4378* module starts asserting *CARRIER_PWR_ON* and *VDD_IO_SEL#* as soon as the main voltage supply is applied to the module and all module supplies necessary for module booting are up. This is to ensure

that the module is powered before the main body of carrier circuits (those outside the power and power control path on the carrier) and the *VDD_IO* of module and carrier is matching. The module will continue to assert signal *RESET_OUT#* after the release of *CARRIER_PWR_ON* and *VDD_IO_SEL#*, for a period sufficient time (at least 10ms) to allow carrier power circuits that the peripheral supplies need to ramp up.

The peripheral power rails on the carrier board need to ramp up in a correct sequence. The sequence starts normally with the highest voltage (e.g. *5V*) followed by the lower voltages (e.g. *3.3V* then *1.8V* and so on). Peripherals normally require that a lower voltage rails is never present if a higher rail is missing. Check the datasheet of all peripheral components on the carrier board for a proper sequencing. The *SMARC-T4378* modules guarantees to apply the reset output *RESET_OUT#* not earlier than 100ms after the *CARRIER_PWR_ON* goes high. This gives the carrier board a sufficient time for ramping up all power rails. *SDIO_PWR_EN* signal have to be pull up to *3.3V* on carrier if users would like to have SD boot up functionality.

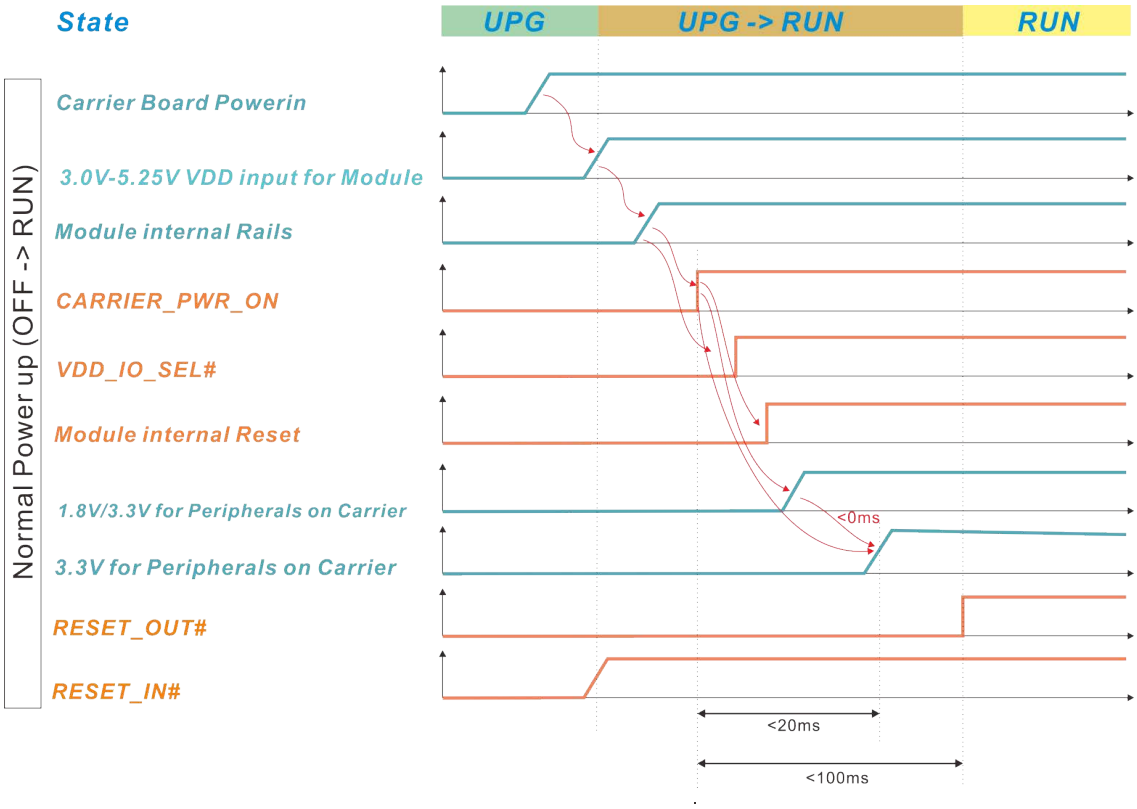


Figure 24: Power-Up Sequence

If the operating system supports it, a shutdown sequence can be initiated. Some systems may benefit from shutting down instead of just removing the main power supply as this allows the operating system to take care of any

housekeeping (e.g. bringing mass storage devices to a controlled halt). Some operating system may not provide the shutdown function.

As it is not permitted that a lower voltage rail is present when a higher voltage rail has been switched off, the sequence of shutting down the peripheral voltages needs to be considered. The lower voltages (e.g. peripheral *3.3V*) need to ramp down before the higher ones do (e.g. peripheral *5V*).

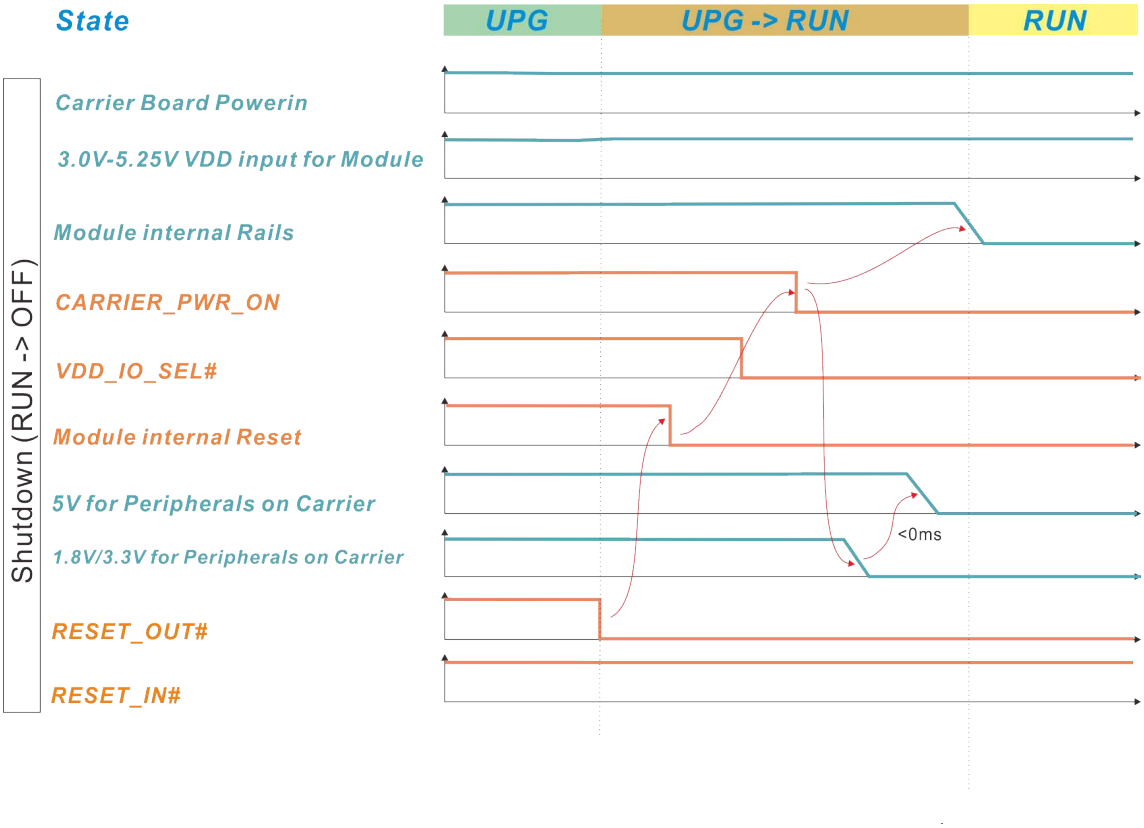


Figure 25: Shutdown Sequence

When the *RESET_IN#* is asserted, a reset cycle is initiated. The module internal reset and the external reset output *RESET_OUT#* are asserted as long as *RESET_IN#* is asserted. If the reset input *RESET_IN#* is de-asserted, the internal reset and the *RESET_OUT#* will remain low for at least 1ms until they are also de-asserted and the module starts booting again. This guarantees a minimum reset time of 1ms even if the reset input *RESET_IN#* is triggered for a short time.

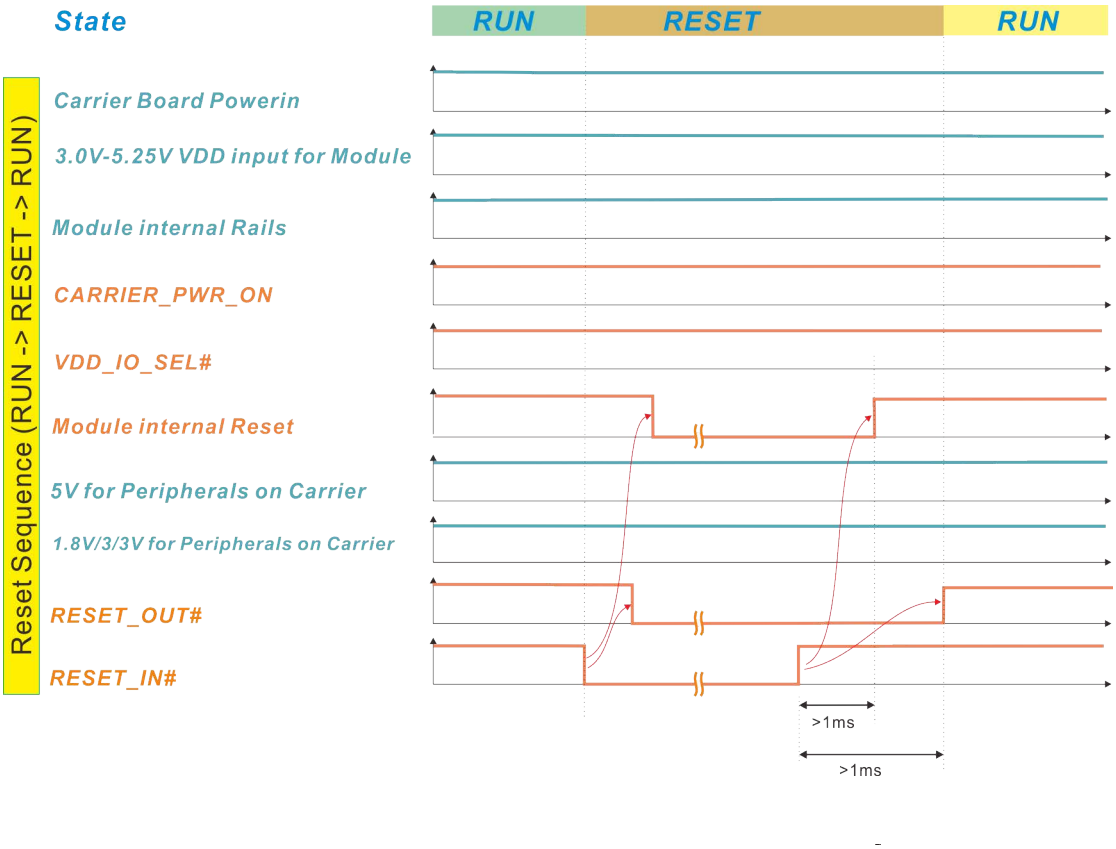


Figure 26: Reset Sequence

4.6 Terminations

4.6.1. Module Terminations

The Module signals listed below will be terminated on the Module. The terminations follow the guidance given in the table below.

Signal Name	Series Termination	Parallel Termination	Notes
I2C_PM_DAT		2.2K pull-up to 1.8V	
I2C_PM_CK		2.2K pull-up to 1.8V	
I2C_LCD_DAT		2.2K pull-up to VDD_IO	
I2C_LCD_CK		2.2K pull-up to VDD_IO	
I2C_GP_DAT		2.2K pull-up to VDD_IO	
I2C_GP_CK		2.2K pull-up to VDD_IO	
SDIO_CD#		10k pull-up to 3.3V	
SDIO_WP		10k pull-up to 3.3V	

Signal Name	Series Termination	Parallel Termination	Notes
USBx_EN_OC#		10K pull-up to 3.3V or a switched 3.3V on the Module	x is '0' or '1' Switched 3.3V: if a USB channel is not used, then the USBx_EN_OC# pull-up rail may be held at GND to prevent leakage currents.
VIN_PWR_BAD#		100k pull-up to VIN	

4.6.2. Carrier/Off-Module Terminations

The following Carrier terminations are required, if the relevant interface is used. If unused, the *SMARC* Module pins may be left un-connected.

Module Signal Group Name	Carrier Series Termination	Carrier Parallel Termination	Notes
GBE_MDI	*Magnetics module appropriate for 10/100/1000 GBE transceivers*	*Secondary side center tap terminations appropriate for Gigabit Ethernet implementations*	
GBE_LINK **(GBE status LED sinks)**		*If used, current limiting resistors and diodes to pulled to a positive supply rail*	*The open drain GBE status signals, GBE_LINK100#, GBE_LINK1000# and GBE_LINK_ACT#, if used, need Carrier based current limiting resistors and LEDs. The LED may be integrated into a Carrier RJ45 jack. A resistor of 68 ohms, and a LED with the anode tied to Carrier 3.3V, is typical.*

4.7 Boot Device Selection

SMARC hardware specification defines three pins (*BOOT_SEL[0:2]*) that allow the Carrier board user to select from eight possible boot devices. The first stage of bootloader on *SMARC-T4378* will always boot up to *SPI NOR* flash first. The *u-boot* on *NOR* flash will read the boot device configuration and load the kernel zImage from selected boot devices. The *BOOT_SELx#* pins are weakly pulled up on the Module and the pin states decoded by module logic. The Carrier shall either leave the Module pin Not Connected ("*Float*" in the table below) or shall pull the pin to *GND*, per the table below.

	Carrier Connection			Boot Source
	BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#	
0	GND	GND	GND	Carrier SATA
1	GND	GND	Float	Carrier SD Card
2	GND	Float	GND	Carrier eMMC Flash
3	GND	Float	Float	Carrier SPI
4	Float	GND	GND	USB1
5	Float	GND	Float	GBE
6	Float	Float	GND	Module eMMC Flash
7	Float	Float	Float	Module SPI

Note:

u-boot is preloaded at fautory default.