# User's Manual

## Computer on Module

*NXP i.MX7 Cortex A7 24bits dual-channel LVDS LCD*
*4 x COM Ports*
*1 x SDHC*
*1 x USB OTG 2.0*
*2 x 10/100/1000M Gigabit Ethernet*
*2 x CAN Bus, 2 x SPIs, 4 x I2Cs*
*1 x PCIe, 1 x MIPI*

# *SMARC-FiMX7*

## (SMARC 2.0 Compliant)


SMARC-FiMX7 Rev. 00B0
SMARC 2.0
MADE IN TAIWAN
embedian

## Revision History

| Revision | Date | Changes from Previous Revision |
|---|---|---|
| 1.0 | 2017/01/6 | Initial Release |
| 2.0 | 2017/08/02 | Change Pinmux for Rev. 00B0 |
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# USER INFORMATION

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# Table of Contents

# Using this Manual

This guide provides information about the Embedian *SMARC-FiMX7* for NXP *i.MX7* embedded *SMARC* core module family.

## Conventions used in this guide

This table describes the typographic conventions used in this guide:

| This Convention | Is used for |
|---|---|
| *Italic type* | Emphasis, new terms, variables, and document titles. |
| `monospaced type` | Filenames, pathnames, and code examples. |

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## Additional Resources

Please also refer to the most recent NXP i.MX7 processor reference manual and related documentation for additional information.


# Introduction

This Chapter gives background information on the *SMARC-FiMX7*
Section include：

- Features and Functionality
- Module Variant
- Differences between Module Variants
- Block diagram
- Software Support / Hardware Abstraction
- Module Variant
- Document and Standard References

# Chapter 1 Introduction

The *SMARC-FiMX7* is a versatile small form factor Computer-On-Module with *NXP i.MX7* processor and offers scalability with single and dual core processors. The dual core *ARM® Cortex®-A7* runs a peak frequency of 1.2GHz, while the single core *ARM® Cortex®-M4* has a peak frequency of 200MHz. The single core *Cortex-A7* has a peak frequency of 800MHz, while the single core Cortex-M4 runs at 200MHz. Both the SoCs support asymmetric or heterogeneous multi-core processing, in which the real time applications can run on the *Cortex-M4*, while the user applications are taken care by *Cortex-A7*. *SMARC-FiMX7* is also the first *SMARC 2.0* specification compliant module from Embedian.
The module connector has 314 edge fingers that mate with a low profile 314 pin 0.5mm pitch right angle connector (this connector is sometimes identified as an 321 pin connector, but 7 pins are lost to the key).
Featuring NXP's *i.MX7* System-on-Chip, Embedian's *SMARC-FiMX7* offers single- or dual-channel *LVDS LCD* interface, dual Gigabit Ethernet, *SDHC*, *USB OTG 2.0*, four *UARTs* support and many peripheral interfaces in a cost effective, low power, miniature package.
Embedian's *SMARC-FiMX7* thin and robust design makes it an ideal building block for reliable system design.

The module is the ideal choice for a broad range of target markets including

- Building Automation
- Enterprise Scanners and Printers
- Smart Grid and Smart Metering
- HMI Control / Security
- IOT solutions
- Smart Home Controls
- Healthcare/Patient Monitoring
- General Control Systems
- Automotive Communication Systems
- Access Control Panels
- And more

Complete and cost-efficient Embedian evaluation kits for Yocto, Ubuntu 14.04/16.04 and Android 6.0+ allow immediate and professional embedded product development with dramatically reduced design risk and time-to-market.

## *1.1 Features and Functionality*

The *SMARC-FiMX7* module is based on the *i.MX7* processor with solo and dual core from *NXP*. This processor offers a high number of interfaces. The module has the following features:

- ***SMARC 2.0*** compliant in an 82mm x 50mm form factor.
- Processor: *NXP i.MX7* ARM Cortex-A7 up to 1.2GHz
- Memory: Onboard 4GB eMMC Flash and 4MB SPI NOR Flash
- Onboard 512MB or 1GB DDR3 Note 1
- Networking: 2 x 10/100/1000 Mbps Ethernet Note 2
    - Display: 18 or 24 bit dual-channel LVDS
- Expansion: 1 x SDHC/SDIO, 1 x USB 2.0 Host
- USB: 1 x USB 2.0 Host, 1 x USB 2.0 OTG, 1 x PCIe Note 3 Gen 2.1
- A single 4KB EEPROM is provided on I2C0 that holds the board information. This information includes board name, serial number, and revision information.
- Additional Interface:
    - 4 x UARTs
    - 2 x SPI
    - 4 x I2C
    - 1 x I2S
    - 2 x CAN Bus
    - 2 x PWM
    - 12 x GPIOs
    - WDT
- SW Support: L:inux, Yocto, Ubuntu, Android 6.0+
- Power Consumption (Typcal)
    - Solo Core (*512MB DDR3L*): 0.9 Watts
    - Dual Core (*1GB DDR3L*): 1.2 Watts
- Thermal:
    - Operating Temperature Range: -20°C ~ 85°C
    - Storage Temperature: -40° ~100°C
    - Junction Temperature SoC: -40° ~105°C
- Power Supply
- 3V to 5.25V (single 5V is recommended in non-battery operation)
- 1.8V module *VDDIO* support

**Note1:**
*SMARC-FiMX7-S* (solo core) only has 512MB DDR3 on board
*SMARC-FiMX7-D* (dual core) only has 1GB DDR3 memory on board (2GB DDR3 memory is available on request.)

**Note2:**
*SMARC-FiMX7-S* (solo core) only supports **one** GBE port.
*SMARC-FiMX7-D* (dual core) supports **two** GBE ports.

**Note3:**
*SMARC-FiMX7-S* (solo core) only supports **one** USB OTG 2.0
*SMARC-FiMX7-D* (dual core) supports one USB Host 2.0, one USB OTG 2.0 and one PCIe interfaces..

## 1.2 Module Variant

The *SMARC-FiMX7* module is available with various options based on processors in this family from *NXP*.


1: "*S*" (solo core running up to 800Mhz, 512MB *DDR3L*)
"*D*" (dual core running up to 1.2GHz, 1GB *DDR3L*)

## 1.3 Differences between Module Variants

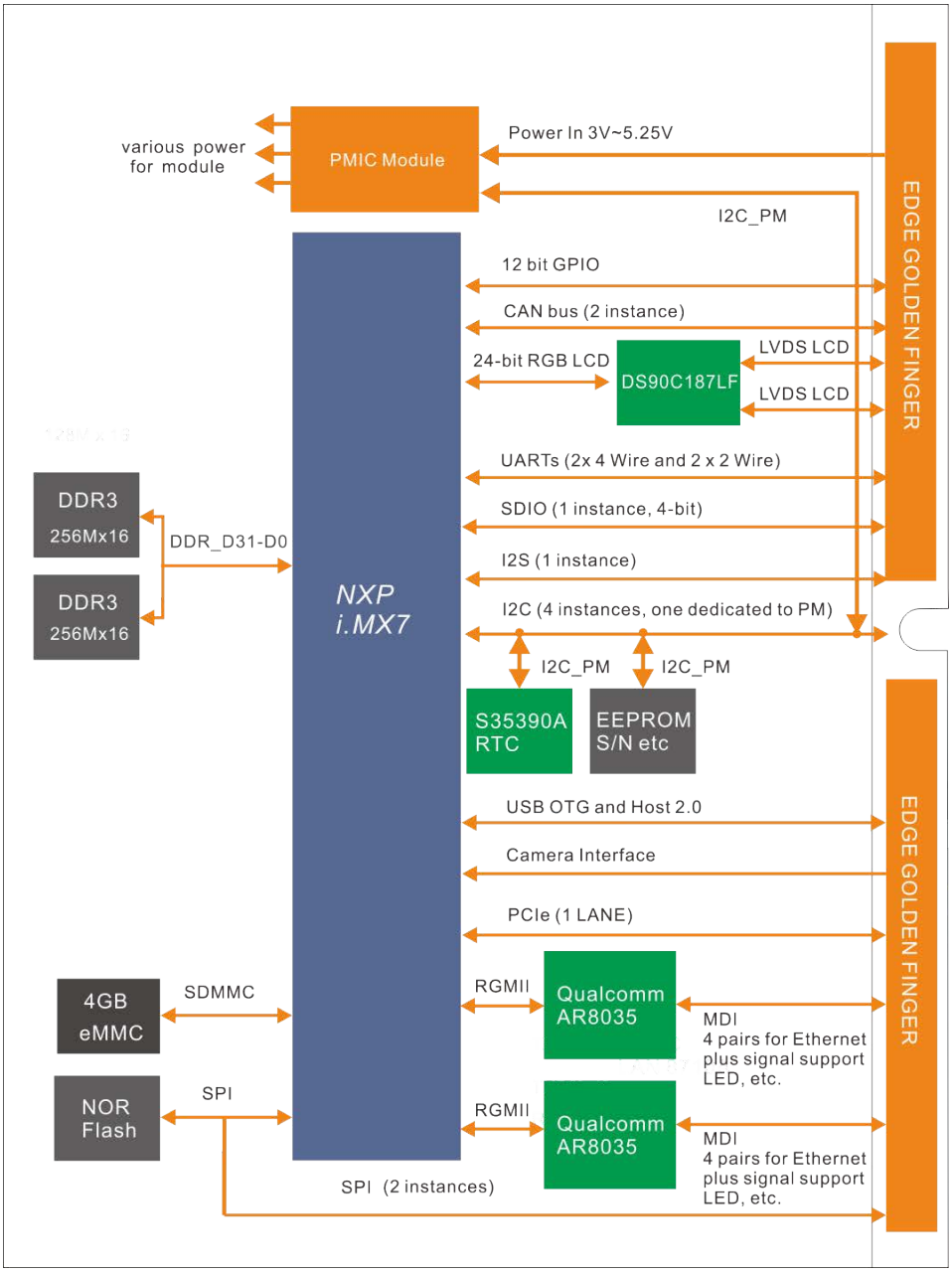
The following table shows the differences between *SMARC-FiMX7-S* and *SMARC-FiMX7-D*. It means the same if the items are not listing in the following table.

| | SMARC-FiMX7-S | SMARC-FiMX7-D |
|---|---|---|
| CPU | MCIMX7S5EVM08S (800Mhz) | MCIMX7D5EVM10S (1.2GHz) |
| DDR3L | 512MB | 1GB |
| GBE w/ AVB | 1 | 2 |
| USB | 1 x USB OTG 2.0 PHY | 1 x USB Host 2.0 PHY, 1 x USB OTG 2.0 PHY |
| PCIe (Gen 2.1) | N/A | 1 |

## 1.4 Block Diagram

The following diagram illustrates the system organization of the *SMARC-FiMX7*. Arrows indicate direction of control and not necessarily signal flow.

### Figure 1: SMARC-FiMX7 Block Diagram




Details for this diagram will be explained in the following chapters.

## 1.5 Software Support / Hardware Abstraction

The Embedian *SMARC-FiMX7* Module is supported by Embedian BSPs (Board Support Package). *SMARC-FiMX7* BSP supports Linux (Ubuntu 14.04/16.04 LTS and Yocto Project) and Android 6.0+. Check with your Embedian contact for the latest BSPs.
This manual goes into a lot of detail on I/O particulars – information is provided on exactly how the various *SMARC* edge fingers tie into the NXP i.MX7 SoC and to other Module hardware. This is provided for reference and context. Almost all of the I/O particulars are covered and abstracted in the BSP and it should generally not be necessary for users to deal with I/O at the register level.

## 1.6 Document and Standard References

### 1.6.1. External Industry Standard Documents

- ***eMMC (Embedded Multi-Media Card)*** the eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 *(www.jedec.org)*.
- ***The I2C Specification,*** Version 2.1, January 2000, Philips Semiconductor (now NXP) *(www.nxp.com)*.
- ***I2S Bus Specification,*** Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (*www.nxp.com*).
- ***JTAG (Joint Test Action Group*** defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (*www.ieee.org*).
- ***MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification,*** Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (*www.mxm-sig.org*).
- ***PICMG® EEEP Embedded EEPROM Specification,*** Rev. 1.0, August 2010 (*www.picmg.org*).
- ***SD Specifications Part 1 Physical Layer Simplified Specification,*** Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (*www.sdcard.org*).
- ***SPI Bus –*** “Serial Peripheral Interface” - de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus).
- ***USB Specifications*** (*www.usb.org*).
- ***Serial ATA Revision 3.1,*** July 18, 2011, Gold Revision, © Serial ATA

International Organization *(www.sata-io.org)*

- ***PCI Express Specifications (www.pci-sig.org)***
- ***SPDIF (aka S/PDIF) ("Sony Philips Digital Interface)-*** *IEC 60958-3*
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### 1.6.2. SGET Documents

- ***SMARC_Hardware_Specification_V1p0***, version 1.0, December 20, 2012.
- ***SMARC_Hardware_Specification_V1p1***, version 1.1, May 29, 2014.
- ***SMARC_Hardware_Specification_V200***, version 2.0, June 2, 2016.
- ***SMARC_Design_Guide_v1p0,*** version 1.0, August 26, 2013

### 1.6.3. Embedian Documents

The following documents are listed for reference. The Module schematic is not usually available outside of Embedian, without special permission. The other schematics will be available. Contact your Embedian representative for more information. The *SMARC* Evaluation Carrier Board Schematic is particularly useful as an example of the implementation of various interfaces on a Carrier board.

- ***SMARC Evaluation Carrier Board Schematic***, PDF and OrCAD format
- ***SMARC Evaluation Carrier Board User's Manual***
- ***SMARC-FiMX7 User's Manual***
- ***SMARC-FiMX7 Schematic Checklist***

### 1.6.4. NXP Documents

- ***IMX7DRM, i.MX7 Dual Applications Processors Reference Manual,*** Aug 12, 2016 (rev. 0.1)
- ***IMX7SRM, i.MX7 Solo Applications Processors Reference Manual,*** Aug 12, 2016 (rev. 0.1)
- ***IMX7DSHDG, Hardware Development Guide for i.MX7 Dual and Solo Applications Processors,*** Jul 29, 2016 (rev. 0)
- ***AN5334, i.MX7 Dual/Solo Product Lifetime Usage***, Sep. 27, 2016 (rev. 0)
- ***AN5317, Loading Code on Cortex-M4 from Linux for the i.MX 6SoloX and i.MX 7Dual/7Solo Application Processors***, Aug 16, 2016 (rev. 0)

### 1.6.5. NXP Development Tools

- ***IOMUX_TOOL for ARM® i.MX7 Microprocessors***
- ***IMX_CST_TOOL,*** NXP Code Signing Tool for the High Assurance Boot library.

### 1.6.6. NXP Software Documents

- ***L4.1.15_2.0.0_LINUX_DOCS,*** i.MX7 Solo/Dual Linux BSP Source Code Files. Oct. 10, 2016 (Rev.# L4.1.15_2.0.0)

### 1.6.7. Embedian Software Documents

- ***Embedian Linux BSP for SMARC-FiMX7 Module***
- ***Embedian Android BSP for SMARC-FiMX7 Module***
- ***Embedian Linux BSP User's Guide***
- ***Embedian Android BSP User's Guide***

### 1.6.8. NXP Design Network

- ***SABRESD***
- ***Nucleus***
- ***QNX***


# Specifications

This Chapter provides SMARC-FiMX7 specifications.
Section include：

- *SMARC-FiMX7* General Functions
- *SMARC-FiMX7* Debug
- Mechanical Specifications
- Electrical Specification
- Environment Specification

# Chapter 2 Specifications

## 2.1 SMARC-FiMX7 General Functions

### 2.1.1. SMARC-FiMX7 Feature Set

This section lists the complete feature set supported by the *SMARC-FiMX7* module.

| SMARC Feature Specification | SMARC 2.0 Specification Maximum Number Possible | SMARC-FiMX7 Feature Support | SMARC-FiMX7 Feature Support Instances |
|---|---|---|---|
| **LVDS LCD Display Support** | 1 | Yes | 1 (18 or 24 bits)[Note1] |
| **DP++** | 1 | No | N/A |
| **HDMI Display Support** | 1 | No | N/A |
| **Serial Camera Support** | 2 | Yes | 1 (2 lanes) |
| **USB Interface** | 6 | Yes | 2 |
| **PCIe Interface** | 4 | Yes | 1 (one Lane, 0 on solo core) |
| **SATA Interface** | 1 | No | N/A |
| **GbE Interface** | 1 | Yes | 1 |
| **2nd GBE Interface** | 1 | Yes | 1 (0 on solo core) |
| **SDIO Interface (4bit)** | 1 | Yes | 1 (max. 25MHz) |
| **SPI Interface** | 2 | Yes | 2 |
| **I2S Interface** | 2 | Yes | 1 |
| **I2C Interface** | 5 | Yes | 4 |
| **Serial** | 4 | Yes | 4 |
| **CAN** | 2 | Yes | 2 |
| **VDDIO** | 1.8V | 1.8V | 1.8V |

**Note:**

1. Single channel *LVDS* interface: 1 x 18 bpp OR 1 x 24 bpp (up to 175 MHz per interface e.g SXGA+ 1400x1050 @ 60Hz + 35% blanking)
2. Dual channel *LVDS* interface: 2 x 18 bpp OR 2 x 24 bpp (up to 185 MHz pixel clock e.g 1080p or SXGA+ 1400x1050 @ 60 Hz + 35% blanking).

### 2.1.2. Form Factor

The *SMARC-FiMX7* module complies with the *SMARC* General Specification module size requirements in an 82mm x 50mm form factor.

### 2.1.3. CPU

The *SMARC-FiMX7* implements *NXP's i.MX7* ARM processor.

| NXP CPU | i.MX7 Solo | i.MX7 Dual |
|---|---|---|
| **Cores** | 1 | 2 |
| **Clock** | 800MHz (A7)<br>200MHz(M4) | 1.2GHz (A7)<br>200MHz (M4) |
| **Memory Speed** | DDR3-533 | DDR3-533 |
| **Memory Bus** | 32-bit | 64-bit |
| **Cache** | (A7) 32 KB/32 KB L1, 512 KB L2<br>(M4) 16 KB/16 KB L1 | (A7) 32 KB/32 KB L1, 512 KB L2<br>(M4) 16 KB/16 KB L1 |
| **Hardware Video Acceleration** | Software Only | Software Only |
| **Hardware 2D/3D Graphics Acceleration** | No, but has an ePxP | No, but has an ePxP |
| **Parallel LCD Resolutions** | 1920x1080x60 (Convert to LVDS signals on module) | 1920x1080x60 (Convert to LVDS signals on module) |

### Note:

1. The *LVDS* interface can be used either as a single channel or as a dual channel. It is also possible to use the *LVDS* interface as two independent single *LVDS* channels. To do this, it is recommended to configure the *LVDS* display in the bootloader. Three independent displays are possible when connected as two single *LVDS* channel and one *HDMI* interface.

### 2.1.4. Module Memory

The *SMARC-FiMX7* module supports different configurations of *DDR3L* memory. The following table shows the available options.

| SMARC Variants | i.MX7 Solo | i.MX7 Dual |
|---|---|---|
| **512MB DDR3L** | *Yes* | *No* |
| **1GB DDR3L** | *No* | *Yes* |
| **2GB DDR3L** | *No* | *Only on Request* |

Check with your Embedian contact or on the Embedian web site for updated information.

### 2.1.5. Onboard Storage

The *SMARC-FiMX7* module supports a 4GB *eMMC* flash memory device, 4MB SPI NOR flash and a 32Kb I2C serial EEPROM on the Module *I2C_GP* (*I2C2*) bus. The device used is an On Semiconductor *AT24C32* equivalent. The Module serial *EEPROM* is intended to retain Module parameter information, including a module serial number. The Module serial *EEPROM* data structure conforms to the *PICMG® EEEP* Embedded *EEPROM* Specification.). The onboard 4MB *SPI NOR* flash is used as *SPI* boot media. The module will always boot up from the onboard *SPI NOR* flash first. The firmware in *NOR* flash will read the configuration from the boot selection and boot up the devices from that selected.

### 2.1.6. Clocks

A 32.768 KHz clock is required for the *i.MX7 CPU RTC* (Real Time Clock) and external (S-35390A) *RTC*.
The *NXP i.MX7 CPU* is provided with a 24 MHz clock using a crystal in normal oscillation mode (On-chip Oscillator).
The *Qualcomm AR8035 PHY* is provided with a 25 MHz clock using a crystal in normal oscillation mode.

### 2.1.7 LVDS Interface

The *SMARC-FiMX7* implements two 18 / 24 bit single channel LVDS output streams that are defined in SMARC 2.0 edge connector for the Primary displays. They can also be configured as an 18 / 24 bit dual-channel LVDS directly out of the *SMARC* Module.

The *LVDS LCD* signals found on the *SMARC-FiMX7* offers two LVDS channels, with up to 185 Mhz pixel clock. They are generated from 24-bit parallel RGB signals from the *NXP® i.MX7* Cortex A7 processor passing through a TI *DS90C187LF* Low Power 1.8V Dual Pixel FPD-Link (LVDS) Serializer. Each channel consists of one clock pair and four data pairs. The LVDS signals support the flow of synchronous RGB data from the i.MX7 CPU to external display devices through LVDS interface.
The LVDS interface also supports various resolutions but with stipulated maximum data rates. The data rates supported are as follows:
For single channel output: Up to 175 MHz per interface (e.g SXGA+ 1400x1050 @ 60Hz + 35 % blanking).
For dual channel output: Up to 185 MHz pixel clock (e.g 1920x1080 @ 60Hz + 35 % blanking)

The LVDS ports support the following configurations:

- One single channel output
- One dual channel output: single input split to two output channels

***Note:***
The *LVDS* interface can be used either as a single channel or as a dual channel.

The following figure shows the *LVDS LCD* block diagram.

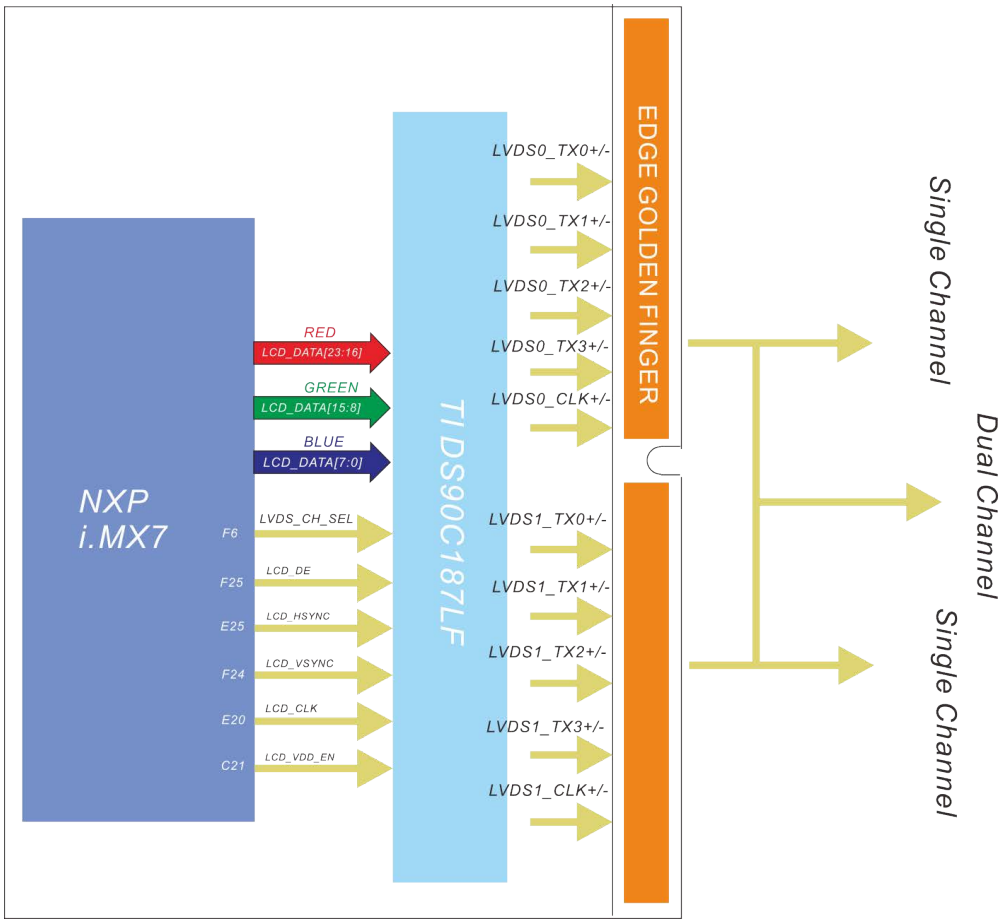



***Figure 2: SMARC-FiMX7 LVDS LCD Diagram***

### 2.1.7.1 LVDS channel select

*SMARC-FiMX7* LVDS LCD interface can be configured as a single-channel LVDS output (default) or a dual-channel LVDS output by *LVDS_CH_SEL* signal. When *LVDS_CH_SEL* is set to low, it will be single-channel LVDS interface. When *LVDS_CH_SEL* is set to high, it will become a dual-channel LVDS interface.

| NXP i.MX7 CPU | | | SMARC-FiMX7 Edge Golden Finger | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| LVDS_CH_SEL | | | | | | |
| F6 | ALT5 | SD2_CMD__ GPIO5_IO13 | | | LVDS_CH _SEL | Set 0 as single channel. Set 1 as dual channel. |

### 2.1.7.2 LVDS Signals Data Flow

*i.MX7* processor and *TI DS90C187LF* implementation is shown in the following table:

| NXP i.MX7 CPU | | | TI DS90C187LF | | Net Names | Note |
|---|---|---|---|---|---|---|
| **Ball** | Mode | Pin Name | Pin# | Pin Name | | |
| G23 | ALT0 | LCD1_DATA23__ LCD1_DATA23 | B14 | INA_22 | LCD_DATA23 | R7 |
| D25 | ALT0 | LCD1_DATA22__ LCD1_DATA22 | B13 | INA_21 | LCD_DATA22 | R6 |
| E24 | ALT0 | LCD1_DATA21__ LCD1_DATA21 | B37 | INA_5 | LCD_DATA21 | R5 |
| C25 | ALT0 | LCD1_DATA20__ LCD1_DATA20 | B36 | INA_4 | LCD_DATA20 | R4 |
| D24 | ALT0 | LCD1_DATA19__ LCD1_DATA19 | B35 | INA_3 | LCD_DATA19 | R3 |
| E23 | ALT0 | LCD1_DATA18__ LCD1_DATA18 | B34 | INA_2 | LCD_DATA18 | R2 |
| G21 | ALT0 | LCD1_DATA17__ LCD1_DATA17 | B33 | INA_1 | LCD_DATA17 | R1 |
| B25 | ALT0 | LCD1_DATA16__ LCD1_DATA16 | B32 | INA_0 | LCD_DATA16 | R0 |
| C24 | ALT0 | LCD1_DATA15__ LCD1_DATA15 | B16 | INA_24 | LCD_DATA15 | G7 |
| D23 | ALT0 | LCD1_DATA14__ LCD1_DATA14 | B15 | INA_23 | LCD_DATA14 | G6 |
| E22 | ALT0 | LCD1_DATA13__ LCD1_DATA13 | B3 | INA_11 | LCD_DATA13 | G5 |
| F21 | ALT0 | LCD1_DATA12__ LCD1_DATA12 | B2 | INA_10 | LCD_DATA12 | G4 |
| G20 | ALT0 | LCD1_DATA11__ LCD1_DATA11 | B1 | INA_9 | LCD_DATA11 | G3 |
| B24 | ALT0 | LCD1_DATA10__ LCD1_DATA10 | B40 | INA_8 | LCD_DATA10 | G2 |
| C23 | ALT0 | LCD1_DATA09__ LCD1_DATA09 | B39 | INA_7 | LCD_DATAD09 | G1 |
| E21 | ALT0 | LCD1_DATA08__ LCD1_DATA08 | B38 | INA_6 | LCD_DATA08 | G0 |

| NXP i.MX7 CPU | | | TI DS90C187LF | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| F20 | ALT0 | LCD1_DATA07__ LCD1_DATA07 | B14 | INA_26 | LCD_DATA07 | B7 |
| A24 | ALT0 | LCD1_DATA06__ LCD1_DATA06 | B13 | INA_25 | LCD_DATA06 | B6 |
| B23 | ALT0 | LCD1_DATA05__ LCD1_DATA05 | B37 | INA_17 | LCD_DATA05 | B5 |
| C22 | ALT0 | LCD1_DATA04__ LCD1_DATA04 | B36 | INA_16 | LCD_DATA04 | B4 |
| A23 | ALT0 | LCD1_DATA03__ LCD1_DATA03 | B35 | INA_15 | LCD_DATA03 | B3 |
| B22 | ALT0 | LCD1_DATA02__ LCD1_DATA02 | B34 | INA_14 | LCD_DATA02 | B2 |
| A22 | ALT0 | LCD1_DATA01__ LCD1_DATA01 | B33 | INA_13 | LCD_DATA01 | B1 |
| D21 | ALT0 | LCD1_DATA00__ LCD1_DATA00 | B32 | INA_12 | LCD_DATA00 | B0 |
| E20 | ALT0 | LCD1_CLK__ LCD1_CLK | A6 | IN_CLK | LCD_CLK | LCD Clock |
| F25 | ALT0 | LCD1_ENABLE__ LCD1_ENABLE | B12 | DE | LCD_DE | Data Enable |
| E25 | ALT0 | LCD1_HSYNC__ LCD1_HSYNC | B11 | VS | LCD_HSYNC | Hsync |
| F24 | ATL0 | LCD1_VSYNC__ LCD1_VSYNC | B10 | HS | LCD_VSYNC | Vsync |
| C21 | ALT0 | LCD1_RESET__ LCD1_RESET | A40 | PDB | LCD_VDD_EN | Power Enable |

The path from *TI DS90C187LF* to the golden finger edge connector is show in the following table.

| TI DS90C187LF | | Golden Finger Edge Connector | | Net Names | Note |
|---|---|---|---|---|---|
| Pin | Pin Name | Pin# | Pin Name | | |
| DS90C187LF, Channel1 (Default) | | | | | |
| B31 | LVDS0_0+ | S125 | LVDS0_0+/ eDP0_TX0+/ DSI0_D0+ | LVDS0_0+ | LVDS0 LCD data channel differential pairs 1 |
| A38 | LVDS0_0- | S126 | LVDS0_0-/ eDP0_TX0-/ DSI0_D0- | LVDS0_0- | |
| B30 | LVDS0_1+ | S128 | LVDS0_1+/ eDP0_TX1+/ DSI0_D1+ | LVDS0_1+ | LVDS0 LCD data channel differential pairs 2 |
| A37 | LVDS0_1- | S129 | LVDS0_1-/ eDP0_TX1-/ DSI0_D1- | LVDS0_1- | |
| B29 | LVDS0_2+ | S131 | LVDS0_2+/ eDP0_TX2+/ DSI0_D2+ | LVDS0_2+ | LVDS0 LCD data channel differential pairs 3 |
| A36 | LVDS0_2- | S132 | LVDS0_2-/ eDP0_TX2-/ DSI0_D2- | LVDS0_2- | |
| B28 | LVDS0_CK+ | S134 | LVDS0_CK+/ eDP0_AUX+/ DSI0_CLK+ | LVDS0_CK+ | LVDS0 LCD differential clock pairs |
| A35 | LVDS0_CK- | S135 | LVDS0_CK-/ eDP0_AUX-/ DSI0_CLK- | LVDS0_CK- | |
| B27 | LVDS0_3+ | S137 | LVDS0_3+/ eDP0_TX3+/ DSI0_D3+ | LVDS0_3+ | LVDS0 LCD data channel differential pairs 4 |
| A34 | LVDS0_3- | S138 | LVDS0_3-/ eDP0_TX3-/ DSI0_D3- | LVDS0_3- | |

| TI DS90C187LF | | Golden Finger Edge Connector | | Net Names | Note |
|---|---|---|---|---|---|
| Pin | Pin Name | Pin# | Pin Name | | |
| DS90C187LF, Channel2 | | | | | |
| B23 | LVDS1_CK+ | S108 | LVDS1_CK+/ eDP1_AUX+/ DSI1_CLK+ | LVDS1_CK+ | LVDS1 LCD differential clock pairs |
| A30 | LVDS1_CK- | S109 | LVDS1_CK-/ eDP1_AUX-/ DSI1_CLK- | LVDS1_CK- | |
| B26 | LVDS1_0+ | S111 | LVDS1_0+/ eDP1_TX0+/ DSI1_D0+ | LVDS1_0+ | LVDS1 LCD data channel differential pairs 1 |
| A33 | LVDS1_0- | S112 | LVDS1_0-/ eDP1_TX0-/ DSI1_D0- | LVDS1_0- | |
| B25 | LVDS1_1+ | S114 | LVDS1_1+/ eDP1_TX1+/ DSI1_D1+ | LVDS1_1+ | LVDS1 LCD data channel differential pairs 2 |
| A32 | LVDS1_1- | S115 | LVDS1_1-/ eDP1_TX1-/ DSI1_D1- | LVDS1_1- | |
| B24 | LVDS1_2+ | S117 | LVDS1_2+/ eDP1_TX2+/ DSI1_D2+ | LVDS1_2+ | LVDS1 LCD data channel differential pairs 3 |
| A31 | LVDS1_2- | S118 | LVDS1_2-/ eDP1_TX2-/ DSI1_D2- | LVDS1_2- | |
| B21 | LVDS1_3+ | S120 | LVDS1_3+/ eDP1_TX3+/ DSI1_D3+ | LVDS1_3+ | LVDS1 LCD data channel differential pairs 4 |
| A28 | LVDS1_3- | S121 | LVDS1_3-/ eDP1_TX3-/ DSI1_D3- | LVDS1_3- | |

A 24 bit dual channel LVDS implementation comprises 10 differential pairs: 4 pairs for odd pixel and control data; 1 pair for the LVDS clock for the odd data; 4 pairs for the even pixel data and control data, and 1 pair for the even LVDS clock. To use the dual channel LVDS mode, you need a display supporting the dual channel LVDS mode in order to receive odd and even pixel data.

### 2.1.7.3 Other LCD Control Signals

The signals in the table below support the *LVDS LCD* interfaces (as these are created from the same i.MX7 source).

| Edge Golden Finder Signal Name | Direction | Type Tolerance | Description |
|---|---|---|---|
| *LCD0_VDD_EN* | *Output* | *CMOS 1.8V* | *High enables panel VDD* |
| *LCD0_BKLT_EN* | *Output* | *CMOS 1.8V* | *High enables panel backlight* |
| *LCD0_BKLT_PWM* | *Output* | *CMOS 1.8V* | *Display backlight PWM control* |
| *I2C_LCD_DAT* | *Bi-Dir OD* | *CMOS 1.8V* | *I2C data – to read LCD display EDID EEPROMs* |
| *I2C_LCD_CK* | *Output* | *CMOS 1.8V* | *I2C clock – to read LCD display EDID EEPROMs* |

Below list *LCD* control signals that mapping to *CPU* iomux and *SMARC* edge connector.

| NXP i.MX7 CPU | | | SMARC-FiMX7 Edge Golden Finger | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| D12 | ALT5 | SAI1_RX_BCLK__ GPIO6_IO17 | S127 | LCD0_BKLT_EN | LCD_ BKLT_EN | High enables panel backlight |
| C21 | ALT5 | LCD1_RESET__ GOIO3_IO04 | S133 | LCD0_VDD_EN | LCD_VDD _EN | High enables panel VDD |
| N3 | ALT1 | GPIO1_IO02__ PWM2_OUT | S141 | LCD0_BKLT_PWM | LCD0_ BKLT_ PWM | Display backlight PWM control |
| K5 | ALT0 | I2C3_SCL | S139 | I2C_LCD_CK | I2C_ LCD_CK | I2C data – to read LCD display EDID EEPROMs |
| K6 | ALT0 | I2C3_SDA | S140 | I2C_LCK_DAT | I2C_ LCD_DAT | I2C data – to read LCD display EDID EEPROMs |

### 2.1.8 USB Interface

*SMARC 2.0* specification defines 6 instances of USB interfaces. Two of them (*USB 2:3*) can support *USB 3.0* super speed signals and two of them (*USB 0:1*) allow *USB OTG* functionality. Embedian *SMARC-FiMX7* module supports two USB ports (*USB 0:1*). Per the *SMARC* 2.0 specification, the module supports a USB "On-The-Go" (*OTG*) 2.0 port capable of functioning either as a client or host device, on the *SMARC USB0.* The *SMARC-FiMX67-D* module also supports one additional *USB2.0* host ports, on *SMARC* USB1. Please note that the solo core *SMARC-FiMX7-S* module only supports one *USB OTG* 2.0 on USB0 port.

The following figure shows the USB0 and USB1 block diagram.

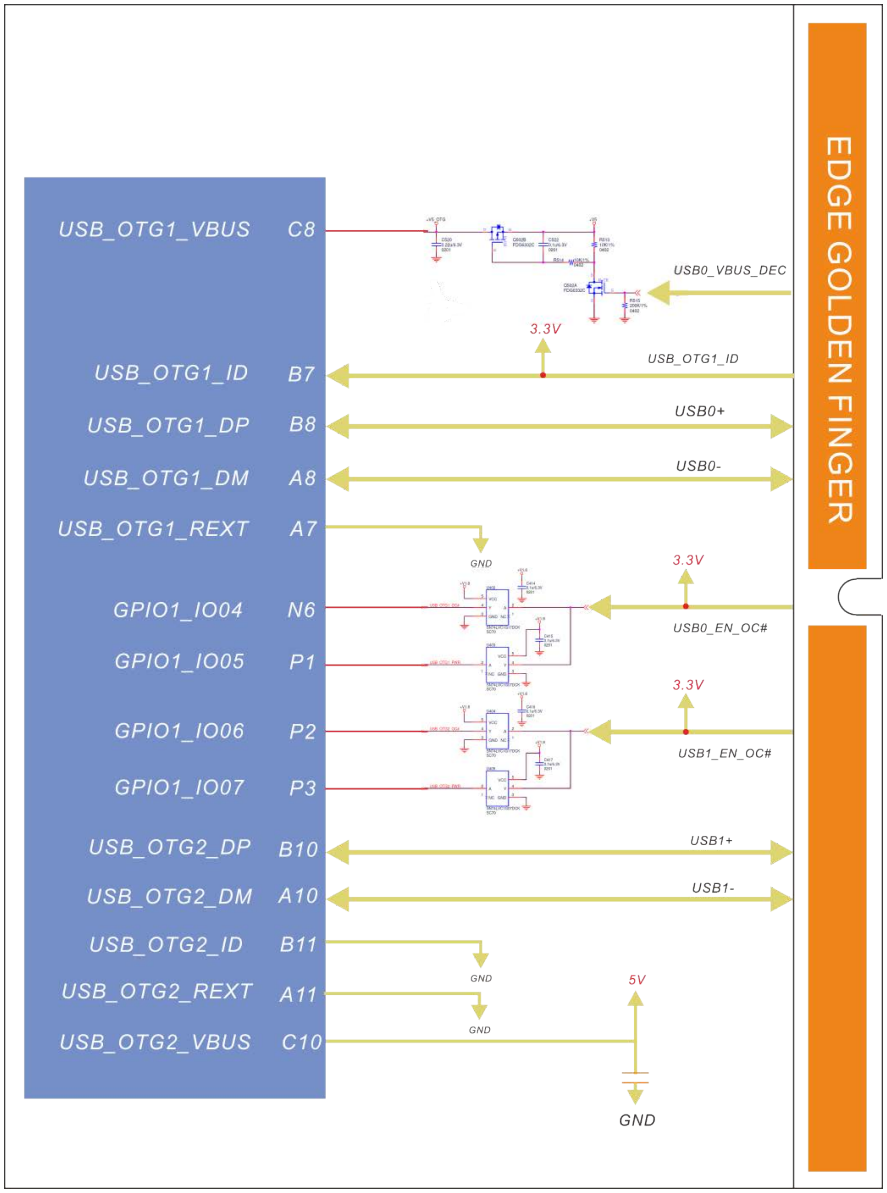



*Figure 3. USB0 and USB1 Block Diagram*

*USB* interface signals are exposed on the *SMARC-FiMX7* edge connector as shown below:

| NXP i.MX7 CPU | | | SMARC-FiMX7 Edge Golden Finger | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| USB0 Port (OTG) | | | | | | |
| B8 | | USB_OTG1_DP | P60 | USB0+ | USB0+ | USB0 port data pair |
| A8 | | USB_OTG1_DN | P61 | USB0- | USB0- | |
| N6 | ALT1 | GPIO1_IO04__ USB_OTG1_OC | P62 | USB0_EN_OC# | USB0_EN_OC# | USB Port0 power enable/over current indication signal |
| P1 | ALT1 | GPIO1_IO05__ USB_OTG1_PWR | | | | |
| C8 | | Turn on USB_OTG_VBUS | P63 | USB0_VBUS_DET | USB0_VBUS_DET | USB host power detection, when this port is used as a device. |
| B7 | | USB_OTG1_ID | P64 | USB0_OTG_ID | USB0_OTG_ID | USB OTG ID input, active high |
| USB1 Port (Host 2.0, dual core only) | | | | | | |
| B10 | | USB_OTG2_DP | P65 | USB1+ | USB1+ | USB1 port data pair |
| A10 | | USB_OTG2_DN | P66 | USB1- | USB1- | |
| P2 | ALT1 | GPIO1_IO06__ USB_OTG2_OC | P67 | USB1_EN_OC# | USB1_EN_OC# | USB Port1 power enable/over current indication signal |
| P3 | ALT1 | GPIO1_IO07__ USB_OTG2_PWR | | | | |

#### 2.1.8.1 USB0 Signals

The table below shows the *USB0* related signals.

| Edge Golden Finder Signal Name | Direction | Type Tolerance | Description |
|---|---|---|---|
| *USB0+*<br><br>*USB0-* | *Bi-Dir* | *USB* | *Differential USB0 Data Pair* |
| *USB0_EN_OC#* | *Bi-Dir*<br><br>*OD* | *CMOS*<br><br>*3.3V* | *Pulled low by Module OD driver to disable USB0 power.*<br><br>*Pulled low by Carrier OD driver to indicate over-current situation.*<br><br>*A 10k pull-up is present on the Module to a 3.3V rail. The pull-up rail may be switched off to conserve power if the USB port is not in use. Further details may be found in Section 2.1.12.3 USBx_EN_OC# Discussion below.* |
| *USB0_VBUS_DET* | *Input* | *USB VBUS 5V* | *USB host power detection, when this port is used as a device.* |
| *USB0_OTG_ID* | *Input* | *CMOS*<br><br>*3.3V* | *USB OTG ID input, active high.* |

### 2.1.8.2 USB1 Signals (Dual Core Only)

*USB1* port is a *USB 2.0* host port. The table below shows the *USB1* related signals.

| Edge Golden Finder Signal Name | Direction | Type Tolerance | Description |
|---|---|---|---|
| *USB1+*<br><br>*USB1-* | *Bi-Dir* | *USB* | *Differential USB1 Data Pair* |
| *USB1_EN_OC#* | *Bi-Dir*<br><br>*OD* | *CMOS*<br><br>*3.3V* | *Pulled low by Module OD driver to disable USB0 power.*<br><br>*Pulled low by Carrier OD driver to indicate over-current situation.*<br><br>*A 10k pull-up is present on the Module to a 3.3V rail. The pull-up rail may be switched off to conserve power if the USB port is not in use. Further details may be found in Section 2.1.12.3 USBx_EN_OC# Discussion below.* |

### 2.1.8.3 USBx_EN_OC# Discussion

The Module *USBx_EN_OC#* pins (where 'x' is 0 or 1 for use with *USB0* or *USB1*) are multi-function Module pins, with a 10k pull-up to a 3.3V rail on the Module, an OD driver on the Module, and, if the *OC#* (over-current) monitoring function is implemented on the Carrier, an OD driver on the Carrier. The use is as follows:

1) On the Carrier board, for external plug-in *USB* peripherals (*USB* memory sticks, cameras, keyboards, mice, etc.) USB power distribution is typically handled by *USB* power switches such as the Texas Instruments *TPS2052B* or the *Micrel MIC2026-1* or similar devices. The Carrier implementation is more straightforward if the Carrier USB power switches have active-high power enables and active low open drain *OC#* outputs (as the TI and Micrel devices referenced do). The USB power switch Enable and *OC#* pins for a given USB channel are tied together on the Carrier. The *USB* power switch enable pin must function with a low input current. The TI and Micrel devices referenced above require 1 microampere or less, at a 3.3V enable voltage level.
2) The Module drives *USBx_EN_OC#* low to disable the power delivery to the *USBx* device.
3) The Module floats *USBx_EN_OC#* to enable power delivery. The line is

pulled to 3.3V by the Module pull-up, enabling the Carrier board USB power switch.

4) If there is a USB over-current condition, the Carrier board USB power switch drives the *USBx_EN_OC#* line low. This removes the over-current condition (by disabling the USB switch enable input), and allows Module software to detect the over-current condition.
5) The Module software should look for a falling edge interrupt on *USBx_EN_OC#*, while the port is enabled, to detect the *OC#* condition. The *OC#* condition will not last long, as the USB power switch is disabled when the switch IC detects the OC# condition.
6) If the *USB* power to the port is disabled (*USBx_EN_OC#* is driven low by the Module) then the Module software is aware that the port is disabled, and the low input value on the port does not indicate an over-current condition (because the port power is disabled).

Carrier Board *USB* peripherals that are not removable often do not make use of *USB* power switches with current limiting and over-current detection. It is usually deemed un-necessary for non-removable devices. In these cases, the *USBx_EN_OC#* pins may be left unused, or they may be used as *USBx* power enables, without making use of the over-current detect Module input feature.

The *SMARC-FiMX7* Module *USB* power enable and over current indication logic implementation is shown in the following block diagram. There are 10k pull-up resistors on the Module on the *SMARC USBx_EN_OC#* lines. Outputs driving the *USBx_EN_OC#* lines are open-drain. The Carrier board USB power switch, if present, is enabled by *USBx_EN_OC#* after a device connection is detected on the *DP/DM* lines.

The Enable pin on the Carrier board *USB* power switch must be active – high and the Over-Current pin (*OC#*) must be open drain, active low (these are commonly available). No pull-up is required on the *USB* power switch Enable or *OC#* line on carrier board; they are tied together on the Carrier and fed to the Module *USBx_EN_OC#* pin.

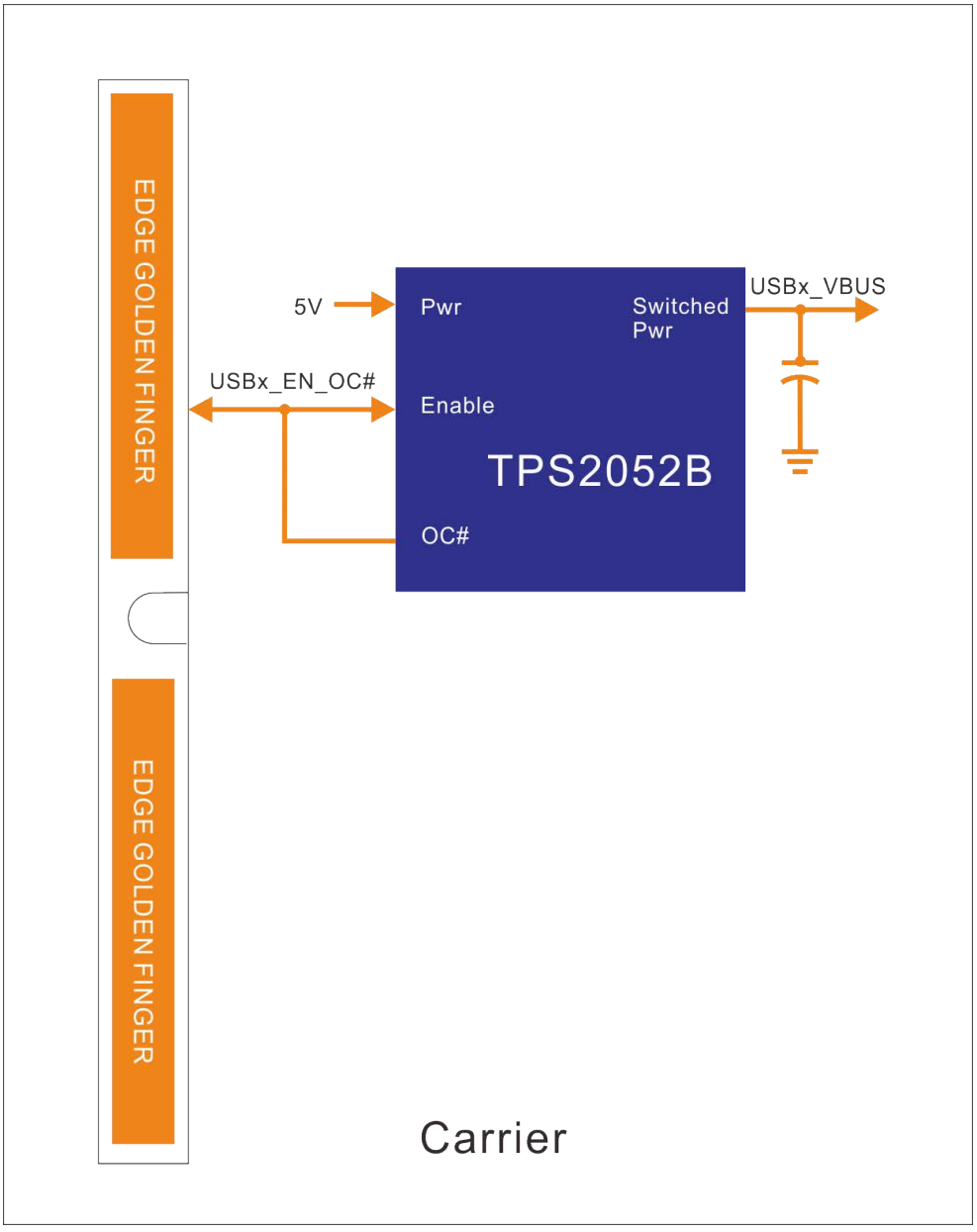



***Figure 4. USB Power Distribution Implementation on Carrier***

### 2.1.9. Gigabit Ethernet Controller (10/100/1000Mbps) Interface

The *SMARC* 2.0 pin-out supports two gigabit Ethernet capable ports. *SMARC-FiMX7-S* module supports one Gigabit Ethernet (10/100/1000Mbps) interfaces, and *SMARC-FiMX7-D* module supports two Gigabit Ethernet (10/100/1000Mbps) ports. The Gigabit Ethernet controller interfaces are accomplished by using the low-power Qualcomm Atheros *AR8035* physical layer (PHY) transceiver with variable I/O voltage that is compliant with the IEEE 802.3-2005 standards. The *AR803*5 supports communication with an Ethernet MAC via a standard RGMII interface.

The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from *GBE0_MDI0*± to *GBE0_MDI3*± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT *RJ45* connector with integrated or external isolation magnetics on the carrier board.

This is diagrammed below.

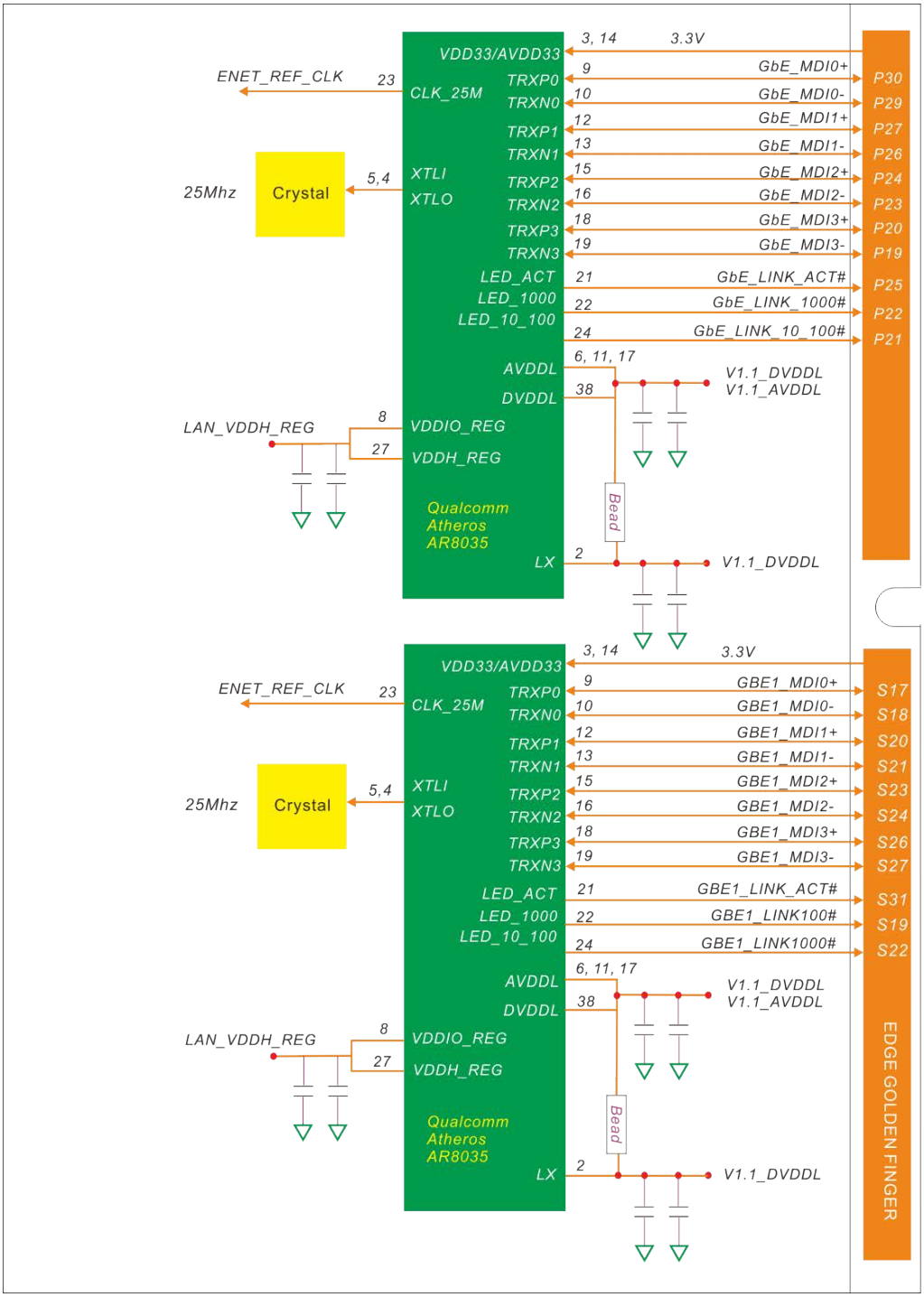



***Figure 5: Gigabit Ethernet Connection from i.MX7 to Qualcomm Atheros AR8035***

### 2.1.9.1. Path of Gigabit LAN1

*i.MX7* processor and the first Qualcomm Atheros *AR8035* implementation is shown in the following table:

| NXP i.MX7 CPU | | | Qualcomm AR8035 | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| Gigabit LAN1 | | | | | | |
| R5 | ALT2 | GPIO1_IO10__ ENET1_MDIO | 39 | MDIO | ENET_MDIO | Serial Management Interface data input/output |
| T1 | ALT2 | GPIO1_IO11__ ENET1_MDC | 40 | MDC | ENET_MDC | Serial Management Interface clock |
| E14 | ALT0 | RGMII1_RD0__ RGMII1_RD0 | 29 | RXD0 | RGMII_RD0 | Bit 0 of the 4 data bits that are sent by the transceiver on the receive path. |
| F14 | ALT0 | RGMII1_RD1__ RGMII1_RD1 | 28 | RXD1 | RGMII1_RD1 | Bit 1 of the 4 data bits that are sent by the transceiver on the receive path. |
| D13 | ALT0 | RGMII1_RD2__ RGMII1_RD2 | 26 | RXD2 | RGMII1_RD2 | Bit 2 of the 4 data bits that are sent by the transceiver on the receive path. |
| E13 | ALT0 | RGMII1_RD3__ RGMII1_RD3 | 25 | RXD3 | RGMII1_RD3 | Bit 3 of the 4 data bits that are sent by the transceiver on the receive path. |
| F15 | ALT0 | RGMII1_RXC__ RGMII1_RXC | 31 | RX_CLK | RGMII1_RXC | Reference clock |
| E15 | ALT0 | RGMII1_RX_CTL__ RGMII1_RX_CTL | 30 | RX_DV | RGMII1_RX_CTL | Indicates both the receive data valid (RXDV) and receive error (RXER) functions per the RGMII specification. |

| NXP i.MX7 CPU | | | Qualcomm AR8035 | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| Gigabit LAN1 | | | | | | |
| E16 | ALT0 | RGMII1_TX_CTL__ RGMII1_TX_CTL | 32 | TX_EN | RGMII1_TX_CTL | Indicates that valid transmission data is present on TXD[3:0]. |
| F17 | ALT0 | RGMII1_TD0__ RGMII1_TD0 | 34 | TXD0 | RGMII1_TD0 | The MAC transmits data to the transceiver using this signal. |
| E17 | ALT0 | RGMII1_TD1__ RGMII1_TD1 | 35 | TXD1 | RGMII1_TD1 | The MAC transmits data to the transceiver using this signal. |
| E18 | ALT0 | RGMII1_TD2__ RGMII1_TD2 | 36 | TXD2 | RGMII1_TD2 | The MAC transmits data to the transceiver using this signal. |
| D18 | ALT0 | RGMII1_TD3__ RGMII1_TD3 | 37 | TXD3 | RGMII1_TD3 | The MAC transmits data to the transceiver using this signal. |
| F16 | ALT0 | RGMII1_TXC__ RGMII1_TXC | 33 | GTX_CLK | RGMII1_TXC | Used to latch data from the MAC into the PHY.<br><br>1000BASE-T: 125MHz<br><br>100BASE-TX: 25MHz<br><br>10BASE-T: 2.5MHz |

The path from *AR8035* to the golden finger edge connector is show in the following table.

| Qualcomm AR8035 | | Golden Finger Edge Connector | | Net Names | Note |
|---|---|---|---|---|---|
| Pin | Pin Name | Pin# | Pin Name | | |
| AR8035 PHY1 | | | | | |
| 9 | TRXP0 | P30 | GbE1_MDI0+ | GBE0_MDI0+ | Differential Transmit/Receive Positive Channel 0 |
| 10 | TRXN0 | P29 | GbE1_MDI0- | GBE0_MDI0- | Differential Transmit/Receive Negative Channel 0 |
| | | P28 | GbE1_CTREF | GBE0_CTREF | Center tap reference voltage |
| 12 | TRXP1 | P27 | GbE1_MDI1+ | GBE0_MDI1+ | Differential Transmit/Receive Positive Channel 1 |
| 13 | TRXN1 | P26 | GbE1_MDI1- | GBE0_MDI1- | Differential Transmit/Receive Negative Channel 1 |
| 15 | TRXP2 | P24 | GbE1_MDI2+ | GBE0_MDI2+ | Differential Transmit/Receive Positive Channel 2 |
| 16 | TRXN2 | P23 | GbE1_MDI2- | GBE0_MDI2- | Differential Transmit/Receive Negative Channel 2 |
| 18 | TRXP3 | P20 | GbE1_MDI3+ | GBE0_MDI3+ | Differential Transmit/Receive Positive Channel 3 |
| 19 | TRXN3 | P19 | GbE1_MDI3- | GBE0_MDI3- | Differential Transmit/Receive Negative Channel 3 |

| Qualcomm AR8035 | | Golden Finger Edge Connector | | Net Names | Note |
|---|---|---|---|---|---|
| Pin | Pin Name | Pin# | Pin Name | | |
| AR8035 PHY1 | | | | | |
| 21 | LED_ACT | P25 | GbE1_LINK_ACT# | GBE0_LINK_ACT# | Link / Activity Indication LED<br><br>Driven low on Link (10, 100 or 1000 mbps)<br><br>Blinks on Activity<br><br>Could be able to sink 24mA or more Carrier LED current |
| 24 | LED_10_100 | P21 | GbE1_LINK100# | GBE0_LINK100# | Link Speed Indication LED for 100Mbps<br><br>Could be able to sink 24mA or more Carrier LED current |
| 22 | LED_1000 | P22 | GbE1_LINK1000# | GBE0_LINK1000# | Link Speed Indication LED for 1000Mbps<br><br>Could be able to sink 24mA or more Carrier LED current |

### 2.1.9.2. Path of Gigabit LAN2 (Dual Core Only)

*i.MX7* processor and the second Qualcomm Atheros *AR8035* implementation is shown in the following table:

| NXP i.MX7 CPU | | | Qualcomm AR8035 | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| Gigabit LAN 2 | | | | | | |
| R5 | ALT2 | GPIO1_IO10__ ENET1_MDIO | 39 | MDIO | ENET_MDIO | Serial Management Interface data input/output |
| T1 | ALT2 | GPIO1_IO11__ ENET1_MDC | 40 | MDC | ENET_MDC | Serial Management Interface clock |
| J21 | ALT2 | EPDC_SDCLK__ RGMII2_RD0 | 29 | RXD0 | RGMII2_RD0 | Bit 0 of the 4 data bits that are sent by the transceiver on the receive path. |
| J20 | ALT2 | EPDC_SDLE__ RGMII2_RD1 | 28 | RXD1 | RGMII2_RD1 | Bit 1 of the 4 data bits that are sent by the transceiver on the receive path. |
| H21 | ALT2 | EPDC_SDOE__ RGMII2_RD2 | 26 | RXD2 | RGMII2_RD2 | Bit 2 of the 4 data bits that are sent by the transceiver on the receive path. |
| H20 | ALT2 | EPDC_SDSHR__ RGMII2_RD3 | 25 | RXD3 | RGMII2_RD3 | Bit 3 of the 4 data bits that are sent by the transceiver on the receive path. |
| G24 | ALT2 | EPDC_SDCE1__ RGMII2_RXC | 31 | RX_CLK | RGMII2_RXC | Reference clock |
| G25 | ALT2 | EPDC_SDCE0__ RGMII2_RX_CTL | 30 | RX_DV | RGMII2_RX_CTL | Indicates both the receive data valid (RXDV) and receive error (RXER) functions per the RGMII specification. |

| NXP i.MX7 CPU | | | Qualcomm AR8035 | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| Gigabit LAN 2 | | | | | | |
| K21 | ALT2 | EPDC_GDRL__ RGMII2_TX_CTL | 32 | TX_EN | RGMII2_TX_CTL | Indicates that valid transmission data is present on TXD[3:0]. |
| H23 | ALT2 | EPDC_SDCE2__ RGMII2_TD0 | 34 | TXD0 | RGMII2_TD0 | The MAC transmits data to the transceiver using this signal. |
| H22 | ALT2 | EPDC_SDCE3__ RGMII2_TD1 | 35 | TXD1 | RGMII2_TD1 | The MAC transmits data to the transceiver using this signal. |
| J25 | ALT2 | EPDC_GDCLK__ RGMII2_TD2 | 36 | TXD2 | RGMII2_TD2 | The MAC transmits data to the transceiver using this signal. |
| J24 | ALT2 | EPDC_GDOE__ RGMII2_TD3 | 37 | TXD3 | RGMII2_TD3 | The MAC transmits data to the transceiver using this signal. |
| H25 | ALT2 | EPDC_GDSP__ RGMII2_TXC | 33 | GTX_CLK | RGMII2_TXC | Used to latch data from the MAC into the PHY.<br><br>1000BASE-T: 125MHz<br><br>100BASE-TX: 25MHz<br><br>10BASE-T: 2.5MHz |

The path from the second *AR8035* to the golden finger edge connector is show in the following table.

| Qualcomm AR8035 | | Golden Finger Edge Connector | | Net Names | Note |
|---|---|---|---|---|---|
| Pin | Pin Name | Pin# | Pin Name | | |
| AR8035 PHY 2 | | | | | |
| 9 | TRXP0 | S17 | GBE1_MDI0+ | GBE1_MDI0+ | Differential Transmit/Receive Positive Channel 0 |
| 10 | TRXN0 | S18 | GBE1_MDI0- | GBE1_MDI0- | Differential Transmit/Receive Negative Channel 0 |
| | | S28 | GBE1_CTREF | GBE1_CTREF | Center tap reference voltage |
| 12 | TRXP1 | S20 | GBE1_MDI1+ | GBE1_MDI1+ | Differential Transmit/Receive Positive Channel 1 |
| 13 | TRXN1 | S21 | GBE1_MDI1- | GBE1_MDI1- | Differential Transmit/Receive Negative Channel 1 |
| 15 | TRXP2 | S23 | GBE1_MDI2+ | GBE1_MDI2+ | Differential Transmit/Receive Positive Channel 2 |
| 16 | TRXN2 | S24 | GBE1_MDI2- | GBE1_MDI2- | Differential Transmit/Receive Negative Channel 2 |
| 18 | TRXP3 | S26 | GBE1_MDI3+ | GBE1_MDI3+ | Differential Transmit/Receive Positive Channel 3 |
| 19 | TRXN3 | S27 | GBE1_MDI3- | GBE1_MDI3- | Differential Transmit/Receive Negative Channel 3 |

| Qualcomm AR8035 | | Golden Finger Edge Connector | | Net Names | Note |
|---|---|---|---|---|---|
| Pin | Pin Name | Pin# | Pin Name | | |
| AR8035 PHY 2 | | | | | |
| 21 | LED_ACT | S31 | GBE1_LINK_ACT# | GBE1_LINK_ACT# | Link / Activity Indication LED<br><br>Driven low on Link (10, 100 or 1000 mbps)<br><br>Blinks on Activity<br><br>Could be able to sink 24mA or more Carrier LED current |
| 24 | LED_10_100 | S19 | GBE1_LINK100# | GBE1_LINK100# | Link Speed Indication LED for 100Mbps<br><br>Could be able to sink 24mA or more Carrier LED current |
| 22 | LED_1000 | S22 | GBE1_LINK1000# | GBE1_LINK1000# | Link Speed Indication LED for 1000Mbps<br><br>Could be able to sink 24mA or more Carrier LED current |

### 2.1.9.3. Gigabit LAN Signals

The table below shows the Gigabit LAN related signals.

| Edge Golden Finder Signal Name | Direction | Type Tolerance | Description |
|---|---|---|---|
| GBE0(1)_MDI0+<br>GBE0(1)_MDI0- | Bi-Dir | GBE_MDI | Bi-directional transmit/receive pair 0 to magnetics (Media Dependent Interface) |
| GBE0(1)_MDI1+<br>GBE0(1)_MDI1- | Bi-Dir | GBE_MDI | Bi-directional transmit/receive pair 1 to magnetics (Media Dependent Interface) |
| GBE0(1)_MDI2+<br>GBE0(1)_MDI2- | Bi-Dir | GBE_MDI | Bi-directional transmit/receive pair 2 to magnetics (Media Dependent Interface) |
| GBE0(1)_MDI3+<br>GBE0(1)_MDI3- | Bi-Dir | GBE_MDI | Bi-directional transmit/receive pair 3 to magnetics (Media Dependent Interface) |
| GBE0(1)_100# | Output<br>OD | CMOS<br>3.3V | Link Speed Indication LED for 100Mbps<br>Could be able to sink 24mA or more Carrier LED current |
| GBE0(1)_1000# | Output<br>OD | CMOS<br>3.3V | Link Speed Indication LED for 1000Mbps<br>Could be able to sink 24mA or more Carrier LED current |
| GBE0(1)_LINK_ACK# | Output<br>OD | CMOS<br>3.3V | Link / Activity Indication LED<br>Driven low on Link (10, 100 or 1000 mbps)<br>Blinks on Activity<br>Could be able to sink 24mA or more Carrier LED current |
| GBE0(1)_CTREF | Output | Reference Voltage | Center-Tap reference voltage for GBE0 Carrier board Ethernet magnetic (not required by the Module GBE PHY) |

### 2.1.9.4. Suggested Magnetics

Listed below are suggested magnetics.

For normal temperature (0°C ~70°C) products.

| Vendor | P/N | Package | Cores | Temp | Configuration |
|---|---|---|---|---|---|
| Halo | HFJ11-1G02E | Integrated RJ45 | 8 | 0°C~70°C | HP Auto-MDIX |
| UDE | RB1-BA6BT9WA | Integrated RJ45 | 8 | -40°C~85°C | HP Auto-MDIX |
| Halo | TG1G-S002NZRL | 24-pin SOIC-W | 8 | 0°C~70°C | HP Auto-MDIX |

For industrial temperature (-40°C ~85°C) products.

| Vendor | P/N | Package | Cores | Temp | Configuration |
|---|---|---|---|---|---|
| UDE | RB1-BA6BT9WA | Integrated RJ45 | 8 | -40°C~85°C | HP Auto-MDIX |
| Halo | TG1G-E012NZRL | 24-pin SOIC-W | 8 | -40°C~85°C | HP Auto-MDIX |

### 2.1.10. PCIe Interface (Dual Core Only)

The *SMARC-FiMX7-D* offers one *PCI* Express lane. The *PCIe* signals are routed from the NXP® *i.MX7* processor to the *PCI* Express port A of the *SMARC-FiMX7* edge finger. These signals support *PCI* Express Gen. 2.1 interfaces at 5 Gb/s and are backward compatible to Gen. 1.1 interfaces at 2.5 Gb/s. Only x1 *PCI Express* link configuration is possible.

The following figure shows the *PCIe* port A block diagram.

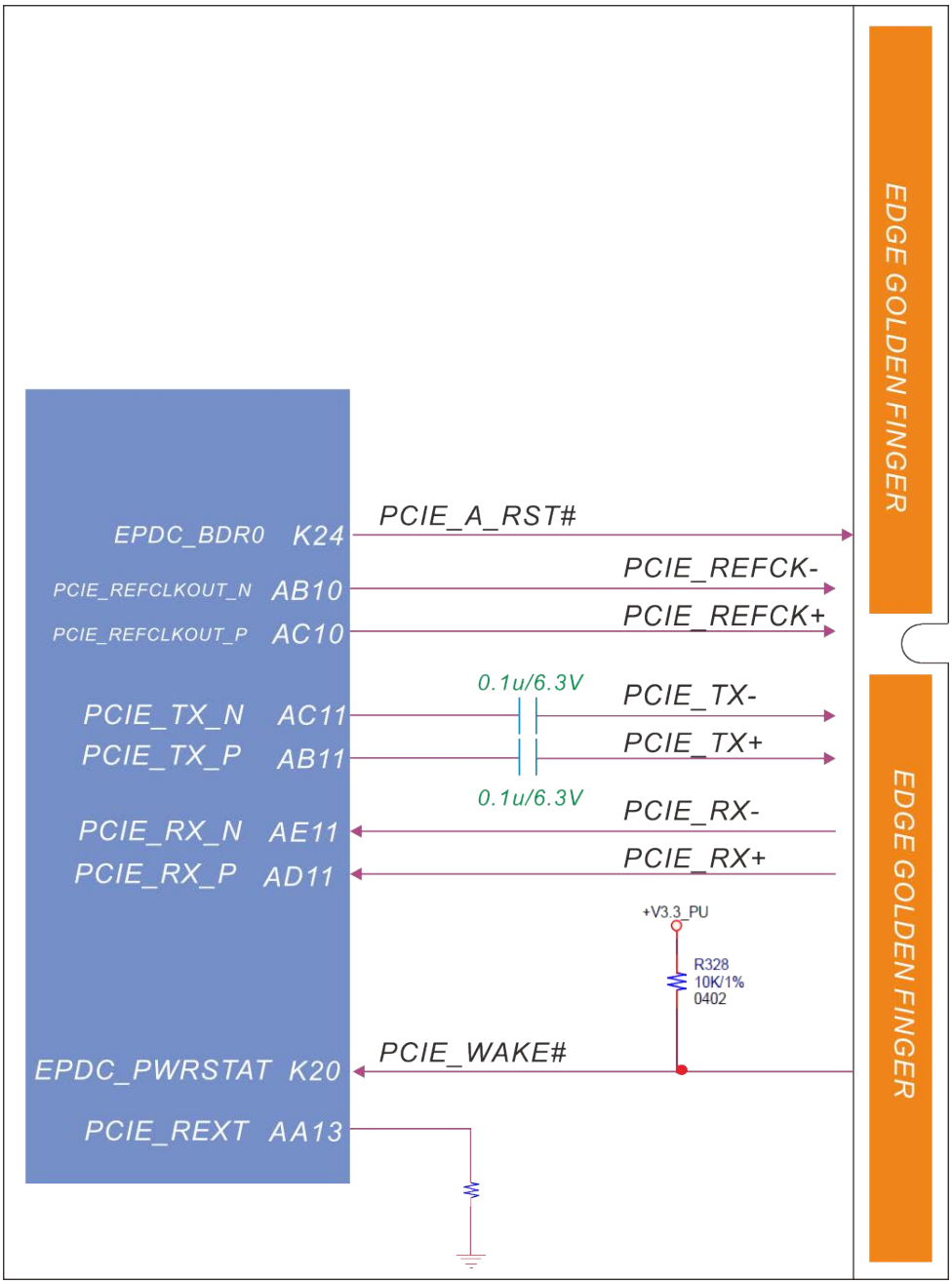



**Figure 6. PCI Express Block Diagram** *SMARC-*

*PCI* Express interface signals are exposed on the *SMARC-FiMX7* edge connector as shown below:

| NXP i.MX7 CPU | | | SMARC-FiMX7 Edge Golden Finger | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| PCI Express Port A | | | | | | |
| K24 | ALT5 | EPDC_BDR0__ GPIO2_IO28 | P75 | PCIE_A_RST# | PCIE_A_RST# | Reset Signal for external devices. |
| AC10 | | PCIE_ REFCLKOUT_P | P83 | PCIE_A_REFCK+ | PCIE_A_REFCK+ | Differential PCI Express Reference Clock Signals for Lanes A |
| AB10 | | PCIE_ REFCLKOUT_N | P84 | PCIE_A_REFCK- | PCIE_A_REFCK- | |
| AD11 | | PCIE_RX_P | P86 | PCIE_A_RX+ | PCIE_A_RX+ | Differential PCIe Link A receive data pair 0 |
| AE11 | | PCIE_RX_N | P87 | PCIE_A_RX- | PCIE_A_RX- | |
| AB11 | | PCIE_TX_P | P89 | PCIE_A_TX+ | PCIE_A_TX+ | Differential PCIe Link A transmit data pair 0 |
| AC11 | | PCIE_TX_N | P90 | PCIE_A_TX- | PCIE_A_TX- | |
| K20 | ALT5 | EPDC_PWRSTAT__ GPIO2_IO31 | S146 | PCIE_WAKE# | PCIE_WAKE# | PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup. |

#### 2.1.10.1. PCIe_Link A Signals

The table below shows the *PCIe_Link A* related signals.

| Edge Golden Finder Signal Name | Direction | Type Tolerance | Description |
|---|---|---|---|
| *PCIE_A_TX+*<br>*PCIE_A_TX-* | *Output* | *HCSL PCIe* | *Differential PCIe Link A transmit data pair 0*<br>*Series coupling caps is on the Module*<br>*Caps is 0402 package 0.1uF* |
| *PCIE_A_RX+*<br>*PCIE_A_RX-* | *Input* | *HCSL PCIe* | *Differential PCIe Link A receive data pair 0*<br>*No coupling caps on Module* |
| *PCIE_A_REFCK+*<br>*PCIE_A_REFCK-* | *Output* | *HCSL PCIe* | *Differential PCIe Link A reference clock output*<br>*DC coupled* |
| | | | |
| *PCIE_A_RST#* | *Output* | *CMOS 3.3V* | *PCIe Port A reset output* |
| | | | |

#### 2.1.10.2. PCIe Wake Signals

The table below shows the *PCIe Wake* signal.

| Edge Golden Finder Signal Name | Direction | Type Tolerance | Description |
|---|---|---|---|
| *PCIE_WAKE#* | *Input* | *CMOS 3.3V* | *PCIe wake up interrupt to host – common to PCIe links A, B, C – pulled up or terminated on Module* |

### 2.1.11. MIPI/CMOS Serial Camera Interface

The *NXP® i.MX7* processor provides connectivity to cameras via the *MIPI/ CSI-2* transmitter and maintains image manipulation and processing with adequate synchronization and control. The Camera Serial Interface (*CSI*) controls the camera port and provides interface to an image sensor or a related device. The role of the camera ports is to receive input from video sources and to provide support for time-sensitive signals to the camera. Non-time-sensitive controls such as configuration, reset are performed by the ARM platform through I2C interface or GPIO signals. There is one instance of *CSI-2* port in the i.MX7 Dual application processor. This interface support from 80 Mbps up to 1.5 Gbps speed per data lane. The CSI-2 Receiver core can manage one clock lane and up to two data lanes through the lane management and de-packetization, providing a maximum throughput of 3 Gbps transfer rate.

The camera interface on *SMARC-FiMX7* is designed as serial interfaces on CSI1 pin groups that can support 2 lanes. The *CSI0* interface is not connected on edge golden finger connector.

The following figure shows the serial camera interface block diagram.

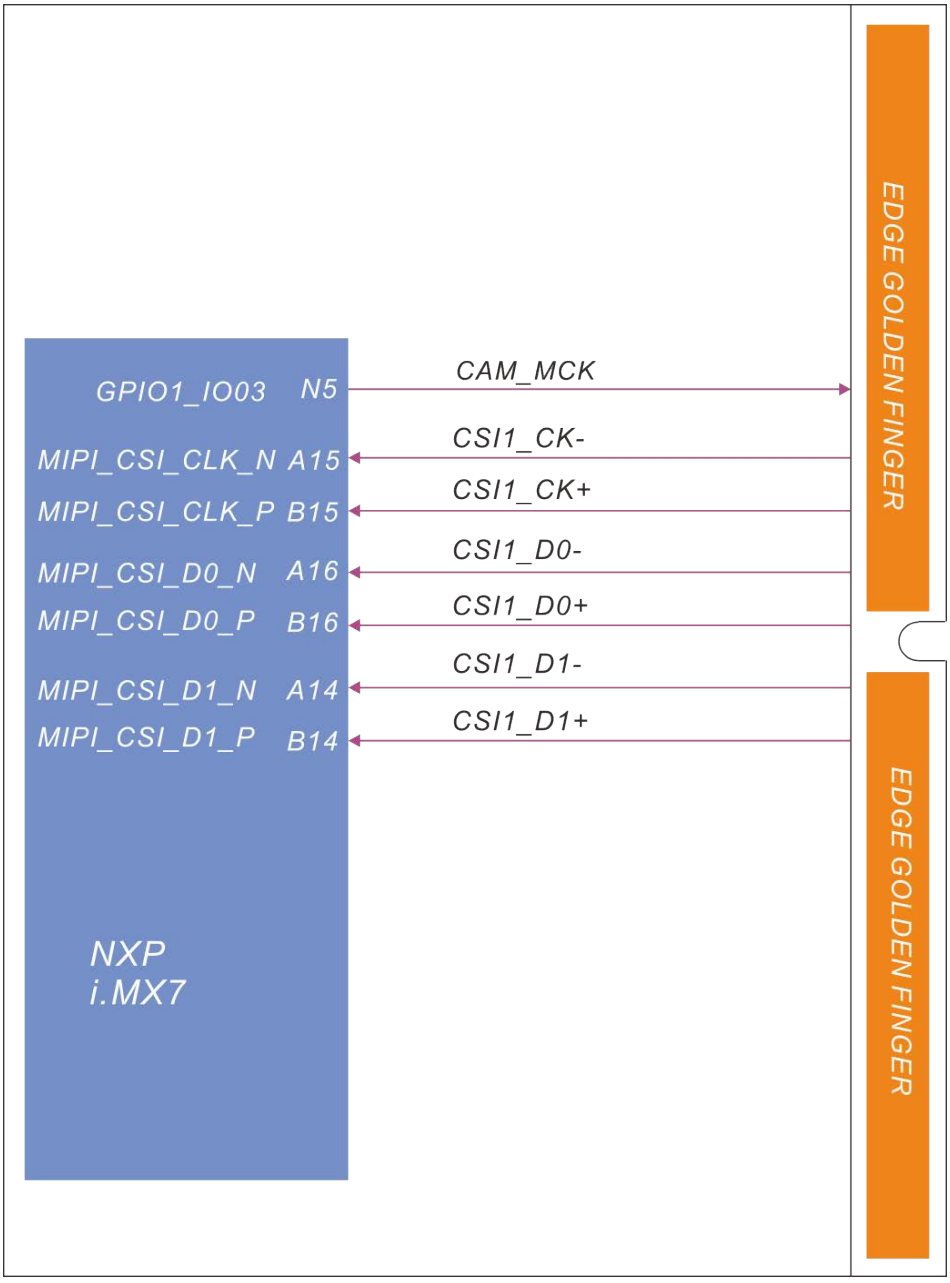



***Figure 7. MIPI/Serial Camera Interface Block Diagram***

MIPI/Serial Camera interface signals are exposed on the *SMARC-FiMX7* edge connector as shown below:

| NXP i.MX7 CPU | | | SMARC-FiMX7 Edge Golden Finger | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| MIPI/Serial Camera Interface | | | | | | |
| N5 | ALT5 | GPIO1_IO03__ CCM_CLKO2 | S6 | CAM_MCK | CAM_MCK | Master clock output for CSI camera support |
| A15 | | MIPI_CSI_CLK_N | P4 | CSI1_CK- | CSI1_CK- | CSI1 differential clock inputs |
| B15 | | MIPI_CSI_CLK_P | P3 | CSI1_CK+ | CSI1_CK+ | |
| A16 | | MIPI_CSI_D0_N | P8 | CSI1_RX0- | CSI1_D0- | |
| B16 | | MIPI_CSI_D0_P | P7 | CSI1_RX0+ | CSI1_D0+ | CSI1 differential data inputs |
| A14 | | MIPI_CSI_D1_N | P11 | CSI1_D1- | CSI1_D1- | |
| B14 | | MIPI_CSI_D1_P | P10 | CSI1_D1+ | CSI1_D1+ | |

#### 2.1.11.1. Camera I2C Support

The *I2C_CAM* port is intended to support serial and parallel cameras. Most contemporary cameras with *I2C* support allow a choice of two *I2C* address ranges.

| Edge Golden Finder Signal Name | Direction | Type Tolerance | Description |
|---|---|---|---|
| *I2C_CAM1_DAT* | *Bi-Dir OD* | *CMOS 1.8V* | *Serial / Parallel camera support link - I2C data* |
| *I2C_CAM1_CK* | *Bi-Dir OD* | *CMOS 1.8V* | *Differential SATA 0 transmit data*<br>*Series coupling caps is on the Module*<br>*Caps is 0402 package 0.1uF* |

### 2.1.11.2. Serial Camera In – CSI1

| Edge Golden Finder Signal Name | Direction | Type Tolerance | Description |
|---|---|---|---|
| CSI1_D[0:1]+ CSI1_D[0:1]- | Input | LVDS D-PHY | CSI1 differential data inputs |
| CSI1_CK+ CSI1_CK- | Input | LVDS D-PHY | CSI1 differential clock inputs |
| CAM_MCK | Output | CMOS 1.8V | Master clock output for CSI1 camera support |

### 2.1.12. SD/SDIO Interface

*SMARC-FiMX7* is configured to support two *MMC* controllers. One is used for on-module 8-bit *eMMC* support, and the other one is used for external SDHC/SDIO interface. The *SMARC-FiMX7* module supports one 4-bit *SDIO* interface, per the *SMARC* 2.0 specification. The *SDIO* interface uses 3.3V signaling, per the *SMARC* spec and for compatibility with commonly available *SDIO* cards.

The following figure shows the SDIO/eMMC block diagram.

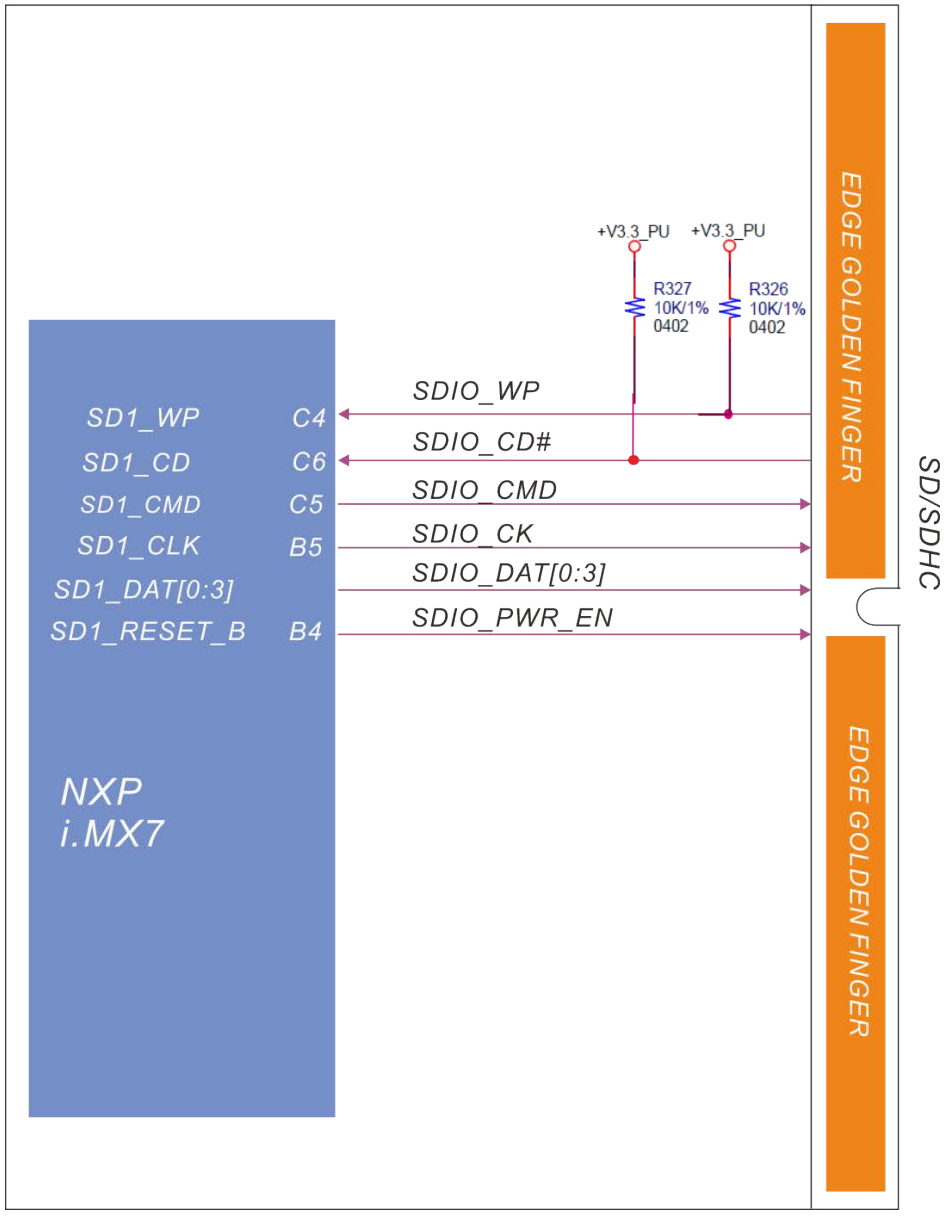



*Figure 8. SD/SDIO/eMMC Interface Block Diagram*

*SDIO* and *SDMMC* interface signals are exposed on the *SMARC* golden finger edge connector as shown below:

| NXP i.MX7 CPU | | | SMARC-FiMX7 Edge Golden Finger | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| SD/SDIO | | | | | | |
| A5 | ALT0 | SD1_DATA0__ SD1_DATA0 | P39 | SDIO_D0 | SDIO_D0 | SDIO Data 0 |
| D6 | ALT0 | SD1_DATA1__ SD1_DATA1 | P40 | SDIO_D1 | SDIO_D1 | SDIO Data 1 |
| A4 | ALT0 | SD1_DATA2__ SD1_DATA2 | P41 | SDIO_D2 | SDIO_D2 | SDIO Data 2 |
| D5 | ALT0 | SD1_DATA3__ SD1_DATA3 | P42 | SDIO_D3 | SDIO_D3 | SDIO Data 3 |
| C4 | ALT0 | SD1_WP__ SD1_WP | P33 | SDIO_WP | SDIO_WP | SDIO write protect signal |
| C5 | ALT0 | SD1_CMD__ SD1_CMD | P34 | SDIO_CMD | SDIO_CMD | SDIO Command signal |
| C6 | ALT0 | SD1_CD__ SD1_CD | P35 | SDIO_CD# | SDIO_CD# | SDIO card detect |
| B5 | ALT0 | SD1_CLK__ SD1_CLK | P36 | SDIO_CK | SDIO_CK | SDIO Clock Signal |
| B4 | ALT0 | SD1_RESET_B__ SD1_RESET_B | P37 | SDIO_PWR_EN | SDIO_PWREN | SD card power enable |

**Note:**

1. The *SDIO* card power should be switched on the Carrier board and the *SDIO* lines should be *ESD* protected. The *SMARC* Evaluation Carrier schematic is useful as an implementation reference.
2. **If *SD* boot up function is required, the pull-up resistor to 3.3V of *SDIO_PWR_EN* # should be 4.7k or less.**
3. *SDIO_WP* and *SDIO_CD#* are 10k pull up to 3.3V on module.

#### 2.1.12.1. SDIO Card (4 bit) Interface

The Carrier SDIO Card can be selected as the Boot Device (See section 4.3).

| Edge Golden Finder Signal Name | Direction | Type Tolerance | Description |
|---|---|---|---|
| SDIO_D[0:3] | Bi-Dir | CMOS 3.3V | 4 bit data path |
| SDIO_CMD | Bi-Dir | CMOS 3.3V | Command Line |
| SDIO_CK | Output | CMOS 3.3V | Clock |
| SDIO_WP | Input | CMOS 3.3V | Write Protect |
| SDIO_CD# | Input | CMOS 3.3V | Card Detect |
| SDIO_PWR_EN | Output | CMOS 3.3V | SD Card Power Enable |

**Note:**

SD Cards are not typically available with a 1.8V *I/O* voltage. The Module SD Card *I/O* level is specified as 3.3V and **not** *CMOS 1.8V*.

### 2.1.13. SPI Interface

The *SMARC-FiMX7* module supports two *NXP i.MX7 SPI* interfaces that are available off-Module for general purpose use. Each SPI channel has two chip-selects that can connect two SPI slave devices on each channel. Every device will share the "*SPI_DIN*", "*SPI_DO*" and "*SPI_CK*" pins, but each device will have its own chip select pin. The chip select signal is a low active signal.
The 4MB onboard *SPI NOR* flash uses an independent *SPI* interface with different chip select signal. The onboard *SPI NOR* flas h on *SMARC-FiMX7* is used as first stage bootloader device. The module will always boot up from *SPI NOR* flash (if *TEST#* pin is floating), and the firmware (first stage bootloader) in NOR flash will read the *BOOT_SEL* configuration and load the second stage bootloader from the user assigned Boot Device.

The SPI interface is diagramed below.

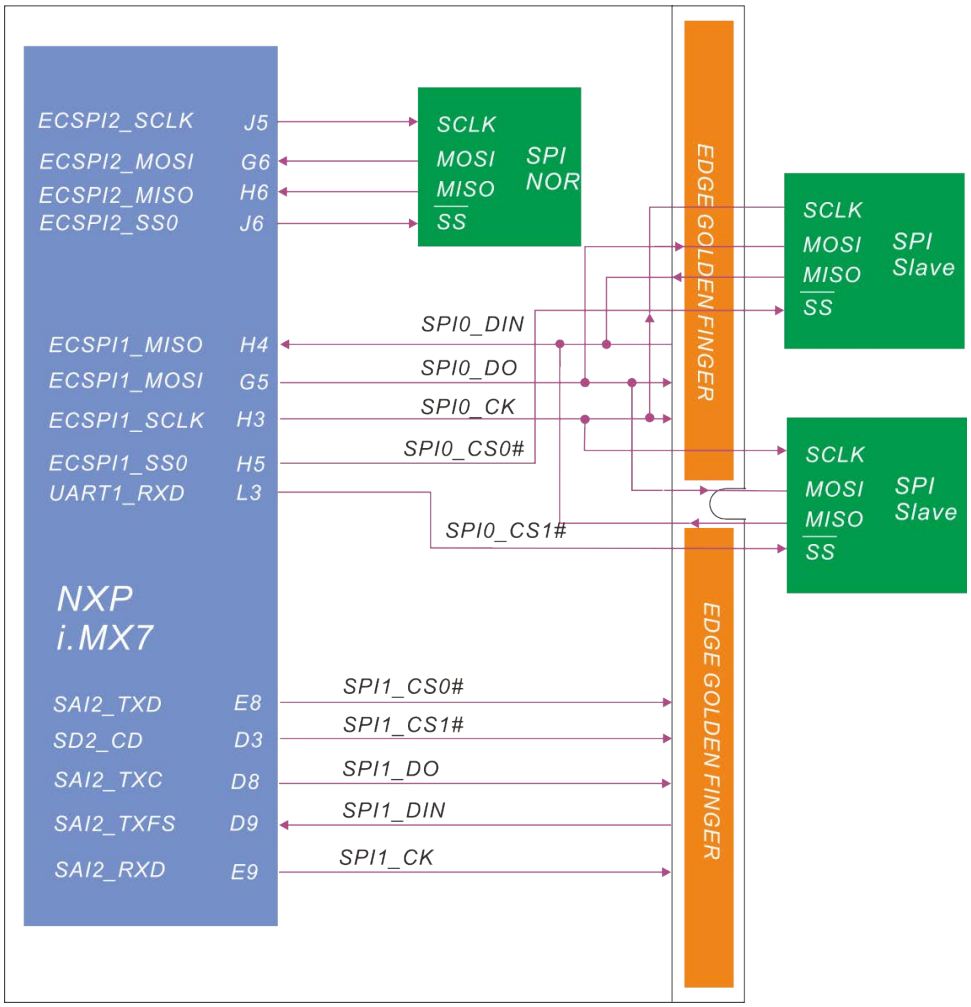



***Figure 9: SPI Serial Flash Schematics***

*SPI* interface signals are exposed on the SMARC golden finger edge connector as shown below:

| NXP i.MX7 CPU | | | SMARC-FiMX7 Edge Golden Finger | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| SPI NOR Flash | | | | | | |
| J6 | ALT0 | ECSPI2_SS0__ ECSPI2_SS0 | | | | Chip select for SPI NOR Flash |
| J5 | ATL0 | ECSPI2_SCLK__ ECSPI2_SCLK | | | | SPI_NOR Master Clock output |
| G6 | ALT0 | ECSPI2_MOSI__ ECSPI2_MOSI | | | | SPI_NOR Master Data input (input to CPU, output from SPI device) |
| H6 | ALT0 | ECSPI2_MISO__ ECSPI2_MISO | | | | SPI_NOR Master Data output (output from CPU, input to SPI device) |

| NXP i.MX7 CPU | | | SMARC-FiMX7 Edge Golden Finger | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| SPI0 Port | | | | | | |
| H5 | ALT0 | ECSPI1_SS0__ ECSPI1_SS0 | P43 | SPI0_CS0# | SPI0_CS0# | SPI0 Master Chip Select 0 output |
| L3 | ALT3 | UART1_RXD__ ECSPI1_SS1 | P31 | SPI0_CS1# | SPI0_CS1# | SPI0 Master Chip Select 1 output |
| H3 | ALT0 | ECSPI1_SCLK_ ECSPI1_SCLK | P44 | SPI0_CK | SPI0_SCLK | SPI0 Master Clock output |
| H4 | ALT0 | ECSPI1_MISO__ ECSPI1_MISO | P45 | SPI0_DIN | SPI0_DIN | SPI0 Master Data input (input to CPU, output from SPI device) |
| G5 | ALT0 | ECSPI1_MOSI__ ECSPI1_MOSI | P46 | SPI0_DO | SPI0_DO | SPI0 Master Data output (output from CPU, input to SPI device) |
| SPI1 Port | | | | | | |
| E8 | ALT1 | SAI2_TXD__ ECSPI1_SS0 | P54 | ESPI1_CS0# | ESPI1_CS0# | SPI1 Master Chip Select 0 output |
| D3 | ALT3 | SD2_CD_B__ ECSP3_SS2 | P55 | ESPI1_CS1# | ESPI1_CS1# | SPI1 Master Chip Select 1 output |
| E9 | ALT1 | SAI2_RXD__ ECSPI1_SCLK | P56 | ESPI1_CK | ESPI1_SCLK | SPI1 Master Clock output |
| D9 | ALT1 | SAI2_TXFS__ ECSPI3_MISO | P57 | ESPI1_IO_0 | ESPI1_IO_0 | SPI1 Master Data input (input to CPU, output from SPI device) |
| D8 | ALT1 | SAI2_TXC__ ECSPI3_MOSI | P58 | ESPI1_IO_1 | ESPI1_IO_1 | SPI1 Master Data output (output from CPU, input to SPI device) |

#### 2.1.13.1. SPI0 Signals

The Carrier SPI0 device may be selected as the Boot Device – see Section 4.3 Boot Select.

| Edge Golden Finder Signal Name | Direction | Type Tolerance | Description |
|---|---|---|---|
| SPI0_CS0# | Output | CMOS 1.8V | SPI0 Master Chip Select 0 output |
| SPI0_CS1# | Output | CMOS 1.8V | SPI0 Master Chip Select 1 output |
| SPI0_CK | Output | CMOS 1.8V | SPI0 Master Clock output |
| SPI0_DIN | Input | CMOS 1.8V | SPI0 Master Data input (input to CPU, output from SPI device) |
| SPI0_DO | Output | CMOS 1.8V | SPI0 Master Data output (output from CPU, input to SPI device) |

### 2.1.13.2. eSPI/SPI1 Signals

| Edge Golden Finder Signal Name | Direction | Type Tolerance | Description |
|---|---|---|---|
| SPI1_CS0# | Output | CMOS 1.8V | SPI1 Master Chip Select 0 output |
| SPI1_CS1# | Output | CMOS 1.8V | SPI1 Master Chip Select 1 output |
| SPI1_CK | Output | CMOS 1.8V | SPI1 Master Clock output |
| SPI1_DIN | Input | CMOS 1.8V | SPI1 Master Data input (input to CPU, output from SPI device) |
| SPI1_DO | Output | CMOS 1.8V | SPI1 Master Data output (output from CPU, input to SPI device) |

### 2.1.14. I2S Interface

The *SMARC-FiMX7* module uses *I2S* format for Audio signals. These signals are derived from the Synchronous Audio Interface (*SAI*) of the *NXP® i.MX7* processor. The *SAI* is a full duplex serial port that allows communication with external devices using a variety of serial protocols. The *I2S* protocol is part of the protocols supported by the *NXP® i.MX7* Cortex A7 processor.

*I2S* interface signals are exposed on the *SMARC-FiMX7* golden finger edge connector as shown below:

| NXP i.MX7 CPU | | | SMARC-FiMX7 Edge Golden Finger | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| E10 | ALT0 | SAI1_MCLK__ SAI1_MCLK | S38 | Audio_MCK | AUD_MCLK | Master clock output to Audio codecs |
| D11 | ALT0 | SAI1_TXFS__ SAI1_TXFS | S39 | I2S0_LRCK | I2S0_LRCK | Left& Right audio synchronization clock |
| E11 | ALT0 | SAI1_TXD__ SAI1_TXD | S40 | I2S0_SDOUT | I2S0_SDOUT | Digital audio Output |
| E12 | ALT0 | SAI1_RXD__ SAI1_RXD | S41 | I2S0_SDIN | I2S0_SDIN | Digital audio Input |
| C11 | ALT0 | SAI1_TXC__ SAI1_TXC | S42 | I2S0_CK | I2S0_CK | Digital audio clock |

**Note:**

*SMARC-FiMX7* currently supports only *I2S* format.

*SGTL5000 I2S* audio codec is used in *EVK-STD-CARRIER* and *EVKS2-STD-CARRIER* evaluation carrier board. An external 24.576 Mhz crystal is used as a reference clock output to audio codec instead of Pin S38. Theoretically, both ways will work.

### 2.1.14.1 I2S0 Signals

| Edge Golden Finder Signal Name | Direction | Type Tolerance | Description |
|---|---|---|---|
| I2S0_LRCK | Bi-Dir | CMOS 1.8V | Left& Right audio synchronization clock |
| I2S0_SDOUT | Output | CMOS 1.8V | Digital audio Output |
| I2S0_SDIN | Input | CMOS 1.8V | Digital audio Input |
| I2S0_CK | Bi-Dir | CMOS 1.8V | Digital audio clock |
| I2S0_MCK | Output | CMOS 1.8V | Master clock output to Audio codecs |

### 2.1.15. Asynchronous Serial Port

The *SMARC-FiMX7* module supports four *UARTs* (*SER0:3*). *SER0* and *SER2* support flow control signals (*RTS#, CTS#*). *SER1* and *SER3* do not support flow control (*TX, RX* only). When working with software, *SER 3* is used for *SMARC-FiMX7* debugging console port.

The module asynchronous serial port signals have a *VDDIO* (1.8V) level signal swing. They can be converted to RS232 level and polarity signals by using a suitable RS232 transceiver. Almost all transceivers available accept a 3.3V signal level: example include the Texas Instruments *MAX3243*. Note that RS232 transceivers invert the signal; a logic '1' is a negative voltage (-3.0V to -15V) and a logic '0' a positive voltage (3.0V to 15V) on the *RS232* line. Since *SMARC 2.0* specification defines 1.8V *VDDIO* module, a level-shift IC from 1.8V to 3.3V might be required.

Asynchronous serial ports interface signals are exposed on the *SMARC* golden finger edge connector as shown below:

| NXP i.MX7 CPU | | | SMARC-FiMX7 Edge Golden Finger | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| SER0 Port | | | | | | |
| L25 | ALT3 | EPDC_DATA09__ UART6_TX_DATA | P129 | SER0_TX | SER0_TX | Asynchronous serial port data out |
| M23 | ALT3 | EPDC_DATA08__ UART6_RX_DATA | P130 | SER0_RX | SER0_RX | Asynchronous serial port data in |
| L24 | ALT3 | EPDC_DATA10__ UART6_RTS_B | P131 | SER0_RTS# | SER0_RTS# | Request to Send handshake line for SER0 |
| L23 | ALT3 | EPDC_DATA11__ UART6_CTS_B | P132 | SER0_CTS# | SER0_CTS# | Clear to Send handshake line for SER0 |
| SER1 Port | | | | | | |
| L6 | ALT0 | UART2_TX_DATA__ UART2_TX_DATA | P134 | SER1_TX | SER1_TX | Asynchronous serial port data out |
| L5 | ALT0 | UART2_RX_DATA__ UART2_RX_DATA | P135 | SER1_RX | SER1_RX | Asynchronous serial port data in |
| SER2 Port | | | | | | |
| L21 | ALT3 | EPDC_DATA13__ UART7_TX_DATA | P136 | SER2_TX | SER2_TX | Asynchronous serial port data out |
| L22 | ALT3 | EPDC_DATA12__ UART7_RX_DATA | P137 | SER2_RX | SER2_RX | Asynchronous serial port data in |
| L20 | ALT3 | EPDC_DATA14__ UART7_RTS_B | P138 | SER2_RTS# | SER2_RTS# | Request to Send handshake line for SER2 |
| K25 | ALT3 | EPDC_DATA15__ UART7_CTS_B | P139 | SER2_CTS# | SER2_CTS# | Clear to Send handshake line for SER2 |
| SER3 Port (Debugging Port) | | | | | | |
| M2 | ALT0 | UART3_TX_DATA__ UART3_TX_DATA | P140 | SER3_TX | SER3_TX | Asynchronous serial port data out |
| M1 | ALT0 | UART3_RX_DATA__ UART3_RX_DATA | P141 | SER3_RX | SER3_RX | Asynchronous serial port data in |

#### 2.1.15.1. UART Signals

Module pins for up to four asynchronous serial ports are defined. The ports are designated *SER0 – SER3*. Ports *SER0* and *SER2* are 4 wire ports (2 data lines and 2 handshake lines). Ports *SER1* and *SER3* are 2 wire ports (data only).

| Edge Golden Finder Signal Name | Direction | Type Tolerance | Description |
|---|---|---|---|
| *SER[0:3]_TX* | *Output* | *CMOS 1.8V* | *Asynchronous serial port data out* |
| *SER[0:3]_RX* | *Input* | *CMOS 1.8V* | *Asynchronous serial port data in* |
| *SER[0]_RTS#* | *Output* | *CMOS 1.8V* | *Request to Send handshake line for SER0* |
| *SER[0]_CTS#* | *Input* | *CMOS 1.8V* | *Clear to Send handshake line for SER0* |
| *SER[2]_RTS#* | *Output* | *CMOS 1.8V* | *Request to Send handshake line for SER2* |
| *SER[2]_CTS#* | *Input* | *CMOS 1.8V* | *Clear to Send handshake line for SER2* |

### 2.1.16. I2C Interface

There is a minimum configuration of I2C ports up to a maximum of 5 ports defined in the *SMARC* specification: *PM* (Power Management), *LCD* (Liquid Crystal Display), *GP* (General Purpose), *CAM* (Camera) and *HDMI.* Because *SMARC-FiMX7* does not have *HDMI* interface, it defines four out of the five *I2C* buses and supports multiple masters and slaves in fast mode (400 KHz operation).
The *I2C_PM* is implemented directly from *NXP i.MX7 I2C1* interfaces. The *I2C_HDMI* is not implemented. The *I2C_GP* is implemented directly from *NXP i.MX7 I2C2* interfaces. The *I2C_LCD* i s implemented directly from *NXP i.MX7 I2C3* interfaces and *I2C_CAM* is implemented directly from *NXP i.MX7 I2C4* interfaces.

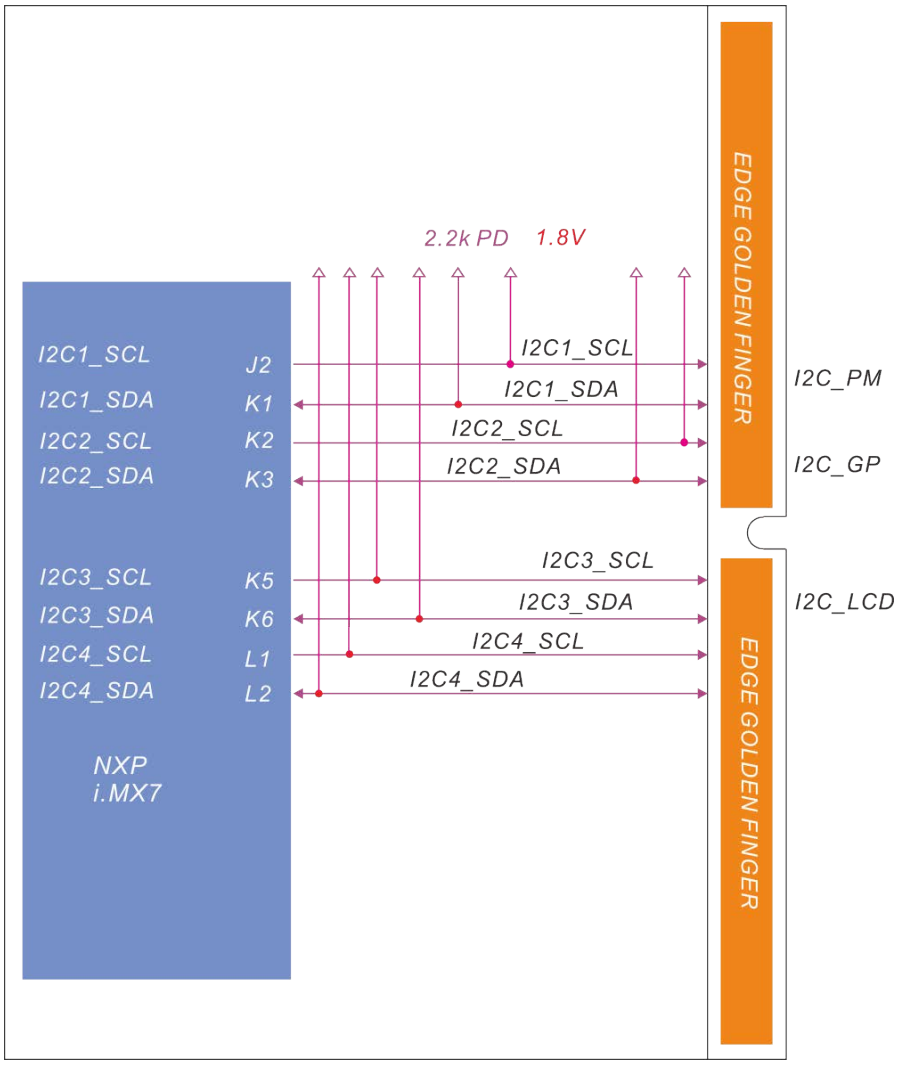



*Figure 10. I2C Interface Block Diagram*

This will be summarized below.

| I2C Port | | Primary Purpose | Alternative Use | I/O Voltage Level |
|---|---|---|---|---|
| Golden Finger Connector | i.MX7 CPU | | | |
| I2C_PM | I2C1 | Power Management support | System configuration management | CMOS<br>1.8V |
| I2C_GP | I2C2 | General purpose use | | CMOS<br>1.8V |
| I2C_LCD | I2C3 | LCD display support, to read LCD display EDID EEPROMs<br>(for parallel and LVDS LCD,) | General Purpose | CMOS<br>1.8V |
| I2C_CAM | I2C4 | Serial camera | General Purpose | CMOS<br>1.8V |

**Note:**

The 2.2k pull-up resistors for *I2C_SCL* and *I2C_SDA* signals are on module.

The *I2C* interface signals are exposed on the *SMARC* golden finger edge connector as shown below:

| NXP i.MX7 CPU | | | SMARC-FiMX7 Edge Golden Finger | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| I2C_PM | | | | | | |
| J2 | ALT0 | I2C1_SCL__ I2C1_SCL | P121 | I2C_PM_CK | I2C_PM_CK | Power management I2C bus clock |
| K1 | ALT0 | I2C1_SDA__ I2C1_SDA | P122 | I2C_PM_DAT | I2C_PM_SDA | Power management I2C bus data |
| I2C_GP | | | | | | |
| K2 | ALT0 | I2C2_SCL__ I2C2_SCL | S48 | I2C_GP_CK | I2C_GP_CK | General purpose I2C bus clock |
| K3 | ALT0 | I2C2_SDA__ I2C2_SDA | S49 | I2C_GP_DAT | I2C_GP_DAT | General purpose I2C bus data |
| I2C_LCD | | | | | | |
| K5 | ALT0 | I2C3_SCL__ I2C3_SCL | S139 | I2C_LCD_CK | I2C_LCD_CK | LCD display I2C bus clock |
| K6 | ATL0 | I2C3_SDA__ I2C3_SDA | S140 | I2C_LCD_DAT | I2C_LCD_DAT | LCD display I2C bus data |
| I2C_CAM | | | | | | |
| L1 | ALT0 | I2C4_SCL__ I2C4_SCL | S1 | I2C_CAM1_CK | I2C_CAM1_CK | Camera I2C bus clock |
| L2 | ALT0 | I2C4_SDA__ I2C4_SDA | S2 | I2C_CAM1_DAT | I2C_CAM1_DAT | Camera I2C bus data |

**Note:**
All *I2C* bus and are operated at 1.8V. The slave devices and their address details are listed in the following table:

| # | Device | Description | Address (7-bit) | Address (8-bit) | | Notes |
|---|---|---|---|---|---|---|
| | | | | Read | Write | |
| *I2C_PM (I2C1) Bus* | | | | | | |
| 1 | Pericom PI6CFGL201BZDIE | PCIe Gen 1-2-3 Clock Generator | 0x68 | 0xA1 | 0xA0 | General purpose parameter EEPROM, Serial number, etc in PICMG EEEP format |
| 2 | NXP MC32PF3000A1EP | PMIC | 0x08 | | | |
| 3 | Seiko S-35390A | Real-time clock IC | 0x30 | 0x61 | 0x60 | General purpose parameter with INT1 register access |
| *I2C_GP* | | | | | | |
| 1 | On Semiconductor CAT24C32 | EEPROM | 0x50 | 0xA1 | 0xA0 | General purpose parameter EEPROM, Serial number, etc in PICMG EEEP format |

**Note:**
On-module *EEPROM* has been moved from *I2C_PM* to *I2C_GP* at *SMARC 2.0*.

### 2.1.17. CAN Bus Interface

The Controller Area Network (*CAN*) is a serial communications protocol which efficiently supports distributed real-time control with a high level of security. The *SMARC-FiMX7* module supports two CAN bus interfaces.
*CAN* interface signals are exposed on the *SMARC* golden finger edge connector as shown below:

| NXP i.MX7 CPU | | | SMARC-FiMX7 Edge Golden Finger | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| CAN0 BUS | | | | | | |
| T3 | ALT3 | GPIO1_IO13__ FLEXCAN1_TX | P143 | CAN0_TX | CAN0_TX | CAN0 Transmit output |
| T2 | ALT3 | GPIO1_IO12__ FLEXCAN1_RX | P144 | CAN0_RX | CAN0_RX | CAN0 Receive input |
| CAN1 BUS | | | | | | |
| T6 | ALT3 | GPIO1_IO15__ FLEXCAN2_TX | P145 | CAN1_TX | CAN1_TX | CAN1 Transmit output |
| T5 | ALT3 | GPIO2_IO14__ FLEXCAN2_RX | P146 | CAN1_RX | CAN1_RX | CAN1 Receive input |

By *SMARC* hardware specification, *CAN0* bus error condition signaling should be supported on the Module *GPIO8* (*P116*) pin. This is an active low input to the Module from the CAN bus transceiver. CAN1 bus error condition signaling should be supported on the Module *GPIO9* (*P117*) pin. This is an active low input to the Module from the CAN bus transceiver
A CAN transceiver on carrier is necessary to adapt the signals from *SMARC* golden finger edge connector, which is TTL levels, to the physical layer used. Because the CAN bus system is typically used to connect multiple systems and is often run over very long distances, both power supply and signal path must be electrically isolated to meet a certain isolation level. Users can refer the "***SMARC Carrier Board Hardware Design Guide***" or CAN transceiver application note such as TI ISO1050 for more details.

### 2.1.17.1. CAN0 BUS Signals

| Edge Golden Finder Signal Name | Direction | Type Tolerance | Description |
|---|---|---|---|
| CAN0_TX | Output | CMOS 1.8V | CAN0 Transmit output |
| CAN0_RX | Input | CMOS 1.8V | CAN0 Receive input |

### 2.1.17.2. CAN1 BUS Signals

| Edge Golden Finder Signal Name | Direction | Type Tolerance | Description |
|---|---|---|---|
| CAN1_TX | Output | CMOS 1.8V | CAN1 Transmit output |
| CAN1_RX | Input | CMOS 1.8V | CAN1 Receive input |

### 2.1.18. GPIOs

The *SMARC-FiMX7* module supports 12 *GPIO*s, per the *SMARC* specification. Specific alternate functions are assigned to some *GPIO*s such as PWM / Tachometer capability, Camera support, *CAN* Error Signaling and HD Audio reset. All pins are capable of bi-directional operation. A default direction of operation is assigned, with half of them (*GPIO0 – GPIO5*) for use as outputs and the remainder (*GPIO6 – GPIO11*) as inputs by *SMARC* hardware specification.

GPIO signals are exposed on the *SMARC* golden finger edge connector as shown below:

| NXP i.MX7 CPU | | | SMARC-FiMX7 Edge Golden Finger | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| GPIOs | | | | | | |
| P20 | ALT5 | EPDC_DATA00__ GPIO2_IO00 | P108 | GPIO0/CAM0_PWR# | GPIO0 | Camera 0 Power Enable, active low output |
| P21 | ALT5 | EPDC_DATA01__ GPIO2_IO01 | P109 | GPIO1/CAM1_PWR# | GPIO1 | Camera 1 Power Enable, active low output |
| N20 | ALT5 | EPDC_DATA02__ GPIO2_IO02 | P110 | GPIO2/CAM0_RST# | GPIO2 | Camera 0 Reset, active low output |
| N21 | ALT5 | EPDC_DATA03__ GPIO2_IO03 | P111 | GPIO3/CAM1_RST# | GPIO3 | Camera 1 Reset, active low output |
| N22 | ALT5 | EPDC_DATA04__ GPIO2_IO04 | P112 | GPIO4/HDA_RST# | GPIO4 | HD Audio Reset, active low output |
| N2 | ALT1 | GPIO1_IO01__ PWM1 | P113 | GPIO5/PWM_OUT | GPIO5 | PWM output |
| M20 | ALT5 | EPDC_DATA05__ GPIO2_IO05 | P114 | GPIO6/TACHIN | GPIO6 | Tachometer input (used with the GPIO5 PWM) |
| M22 | ALT5 | EPDC_DATA07__ GPIO2_IO07 | P115 | GPIO7/PCAM_FLD | GPIO7 | PCAM_FLD (Field) signal input |
| M21 | ALT5 | EPDC_DATA06__ GPIO2_IO06 | P116 | GPIO8/CAN0_ERR# | GPIO8 | CAN0 Error signal, active low input |
| L4 | ALT5 | UART1_TXD__ GPIO4_IO01 | P117 | GPIO9/CAN1_ERR# | GPIO9 | CAN1 Error signal, active low input |
| M5 | ALT5 | UART3_RTS__ GPIO4_IO06 | P118 | GPIO10 | GPIO10 | |
| M6 | ALT5 | UART3_CTS__ GPIO4_IO07 | P119 | GPIO11 | GPIO11 | |

#### 2.1.18.1. GPIO Signals

Twelve Module pins are allocated for GPIO (general purpose input / output) use. All pins are capable of bi-directional operation. By *SMARC* specification, *GPIO0 – GPIO5* are recommended for use as outputs and the remainder (*GPIO6 – GPIO11*) as inputs.
At Module power-up, the state of the GPIO pins may not be defined, and may briefly be configured in the “wrong” state, before boot loader code corrects them. Carrier designers should be aware of this and plan accordingly.
All GPIO pins are capable of generating interrupts. The interrupt characteristics (edge or level sensitivity, polarity) are generally configurable in the *i.MX7* register set.

| Edge Golden Finder Signal Name | Preferred Direction | Type Tolerance | Description |
|---|---|---|---|
| GPIO0/CAM0_PWR# | Output | CMOS 1.8V | Camera 0 Power Enable, active low output |
| GPIO1/CAM1_PWR# | Output | CMOS 1.8V | Camera 1 Power Enable, active low output |
| GPIO2/CAM0_RST# | Output | CMOS 1.8V | Camera 0 Reset, active low output |
| GPIO3/CAM1_RST# | Output | CMOS 1.8V | Camera 1 Reset, active low output |
| GPIO4/HDA_RST# | Output | CMOS 1.8V | HD Audio Reset, active low output |
| GPIO5/PWM_OUT | Output | CMOS 1.8V | PWM output |
| GPIO6/TACHIN | Input | CMOS 1.8V | Tachometer input (used with the GPIO5 PWM) |
| GPIO7/PCAM_FLD | Input | CMOS 1.8V | PCAM_FLD (Field) signal input |
| GPIO8/CAN0_ERR# | Input | CMOS 1.8V | CAN0 Error signal, active low input |
| GPIO9/CAN1_ERR# | Input | CMOS 1.8V | CAN1 Error signal, active low input |
| GPIO10 | Input | CMOS 1.8V | |
| GPIO11 | Input | CMOS 1.8V | |

### 2.1.19. Other Control Pins

SMARC specification defines some special control signals for power management. They are especially useful for mobile devices. The *SMARC-FiMX7* module supports all those signals.

The power management signals are exposed on the *SMARC* golden finger edge connector as shown below:

| NXP i.MX7 CPU | | | SMARC-FiMX7 Edge Golden Finger | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| Special Control Pin | | | | | | |
| AC8 | | ONOFF | P128 | POWER_BTN# | POWER_BTN# | Power-button input from Carrier board. |
| C3 | ALT5 | SD2_WP__GPIO5_IO10 | S148 | LID# | LID# | Lid open/close indication to Module. Low indicates lid closure. |
| E4 | ALT5 | SD2_DATA00__GPIO5_IO14 | S149 | SLEEP# | SLEEP# | Sleep indicator from Carrier board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. |
| R1 | ALT0 | GPIO1_IO08__GPIO1_IO08 | S151 | CHARGING# | CHARGING# | Held low by Carrier during battery charging. |

| NXP i.MX7 CPU | | | SMARC-FiMX7 Edge Golden Finger | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| Special Control Pin | | | | | | |
| R2 | ALT0 | GPIO1_IO09__ GPIO1_IO09 | S152 | CHARGER_ PRSNT# | CHARGER_ PRSNT# | Held low by Carrier if DC input for battery charger is present. |
| C12 | ALT5 | SAI1_RXFS__ GPIO6_IO16 | S153 | CARRIER_STBY# | CARRIER_ STBY# | The Module shall drive this signal low when the system is in a standby power state. |
| | | | S154 | CARRIER_ PWR_ON | CARRIER_ PWR_ON | Carrier board circuits should not be powered up until the Module asserts the CARRIER_PWR _ON signal. |
| G3 | ALT5 | SD2_RESET__ GPIO5_IO011 | S156 | BATLOW# | BAT_LOW# | Battery low indication to Module. |

#### 2.1.19.1. Other Control Signals

| Edge Golden Finder Signal Name | Preferred Direction | Type Tolerance | Description |
|---|---|---|---|
| POWER_BTN# | Input | CMOS 1.8V | Power-button input from Carrier board. |
| LID# | Input | CMOS 1.8V | Lid open/close indication to Module. Low indicates lid closure. |
| SLEEP# | Input | CMOS 1.8V | Sleep indicator from Carrier board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. |
| CHARGING# | Input | CMOS 1.8V | Held low by Carrier during battery charging. |
| CHARGER_ PRSNT# | Input | CMOS 1.8V | Held low by Carrier if DC input for battery charger is present. |
| CARRIER_STBY# | Output | CMOS 1.8V | The Module shall drive this signal low when the system is in a standby power state. |
| CARRIER_ PWR_ON | Output | CMOS 1.8V | Carrier board circuits should not be powered up until the Module asserts the CARRIER_PWR_ON signal. |
| BATLOW# | Input | CMOS 1.8V | Battery low indication to Module. |

### 2.1.20. Watchdog Timer Interface

*i.MX7* features an internal WDT. Embedian's Linux kernel enables the internal *i.MX7* WDT and makes this functionality available to users through the standard Linux Watchdog API.
A description of the API is available following the link below:
http://www.kernel.org/doc/Documentation/watchdog/watchdog-api.txt

*WDT* signals are exposed on the *SMARC* golden finger edge connector as shown below:

| NXP i.MX7 CPU | | | SMARC-FiMX7 Edge Golden Finger | | Net Names | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| Watchdog Timer | | | | | | |
| E19 | ALT1 | ENET1_CRS__ WDOG2_RST_B_DEB | S145 | WDT_TIME_OUT# | WDT_TIME_OUT# | Watchdog-Timer Output |

**Note:**

*GPIO1_IO00__WDOG1_B* signal connects *PWRON* of *MC32PF3000A1EP PMIC* on module.

### 2.1.21. JTAG

Figure 11 shows the *SMARC-FiMX7 JTAG* connectors location and pin out.

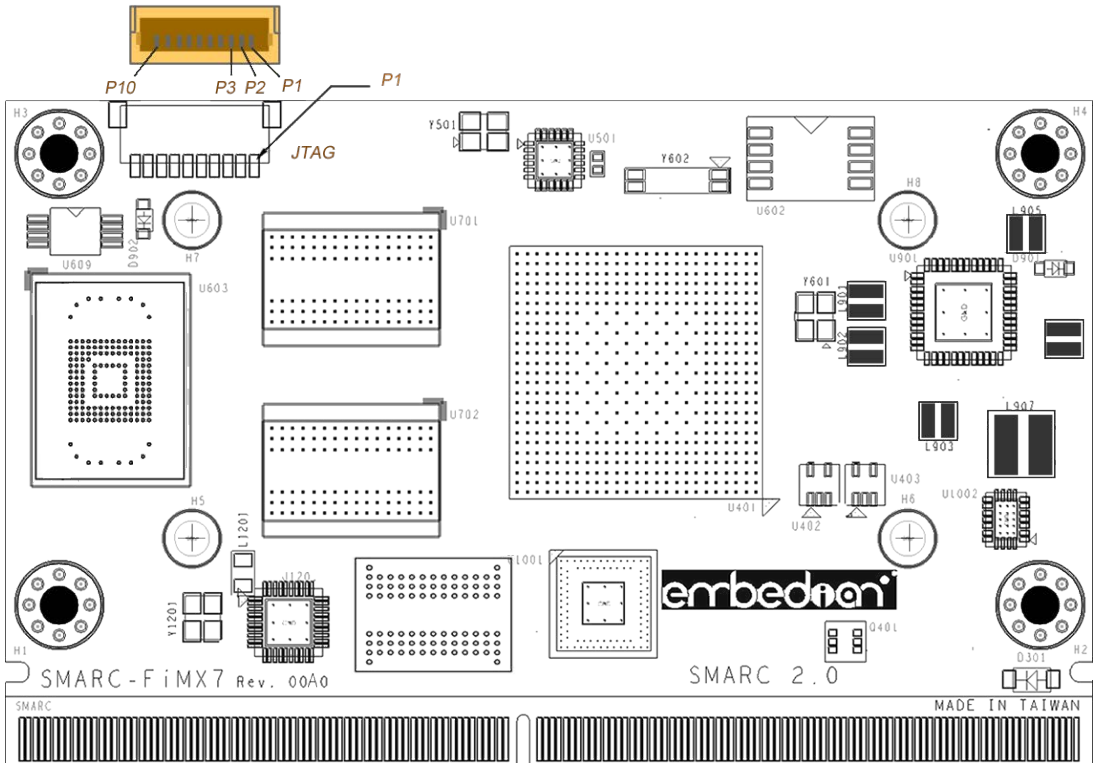



*Figure 11: JTAG Connector Location and Pinout*

*JTAG* functions for CPU debug and test are implemented on separate small form factor connector (CN3: *JST SM10B-SRSS-TB*, 1mm pitch R/A SMD Header). The *JTAG* pins are used to allow test equipment and circuit emulators to have access to the Module CPU. The pin-outs shown below are used:

| NXP i.MX7 CPU | | | JTAG(Connector: JST SM10B-SRSS-TB, 1mm pitch R/A SMD Header) | | Type | Note |
|---|---|---|---|---|---|---|
| Ball | Mode | Pin Name | Pin# | Pin Name | | |
| JTAG | | | | | | |
| | | | 1 | VDD_18A | Power | JTAG I/O Voltage (sourced by Module) |
| U2 | ATL0 | JTAG_TRST_B | 2 | nTRST | I | JTAG Reset, active low |
| U4 | ALT0 | JTAG_TMS | 3 | TMS | I | JTAG mode select |
| U6 | ALT0 | JTAG_TDO | 4 | TDO | O | JTAG data out |
| U3 | ALT0 | JTAG_TDI | 5 | TDI | I | JTAG data in |
| U5 | ALT0 | JTAG_TCK | 6 | TCK | I | JTAG clock |
| | | | 7 | RTCK | I | JTAG return clock |
| | | | 8 | GND | Ground | Ground |
| | | | 9 | MFG_Mode# | I | Pulled low to allow in-circuit SPI ROM update |
| | | | 10 | GND | Ground | Ground |

### 2.1.22. Boot ID EEPROM

The *SMARC-FiMX7* module includes an *I2C* serial *EEPROM* available on the *I2C_PM* bus. An On Semiconductor *24C32* or equivalent *EEPROM* is used in the module. The device operates at 1.8V. The Module serial *EEPROM* is placed at I2C slave addresses A2 A1 A0 set to 0 (I2C slave address 50 hex, 7 bit address format or A0 / A1 hex, 8 bit format) (for I2C EEPROMs, address bits A6 A5 A4 A3 are set to binary 0101 convention).

The module serial *EEPROM* is intended to retain module parameter information, including serial number. The module serial *EEPROM* data structure conforms to the PICMG® *EEEP* Embedded *EEPROM* Specification.

**Note:**

The *EEPROM ID* memory layout is now follow the mainline and as follows.

| Name | Size (Bytes) | Contents |
|---|---|---|
| **Header** | 4 | MSB 0xEE3355AA LSB |
| **Board Name** | 8 | Name for Board in ASCII "SMCMX7D1" = Embedian SMARC-FiMX7 Computer on Module with Dual Core and 1GB DDR3L Configuration<br>"SMCMX7S0" = Embedian SMARC-FiMX7 Computer on Module with solo Core and 512MB DDR3L Configuration |
| **Version** | 4 | Hardware version code for version in ASCII "00A0" = rev. A0 |
| **Serial Number** | 12 | Serial number of the board. This is a 12 character string which is: WWYYMSD1nnnn<br>Where: WW = 2 digit week of the year of production<br>YY = 2 digit year of production<br>MS = Module Serial Number<br>D1/S0 = CPU Core and DDR Configuration Variants<br>nnnn = incrementing board number |
| **Configuration Option** | 32 | Codes to show the configuration setup on this board. For the available module variants supported, the following codes are used:<br>ASCII = "SMCMX7D1" = default configuration<br>Remaining 24 bytes are reserved |
| **MAC Address** | 6 | Ethernet MAC Address (10:0D:32:XX:XX:XX) |
| **MAC Address** | 6 | Ethernet MAC Address for 2nd LAN (10:0D:32:XX:XX:XX) |
| **Available** | 32720 | Available space for other non-volatile codes/data |

## 2.2 SMARC-FiMX7 Debug

### 2.2.1. Serial Port Debug

*SMARC* module has 4 serial output ports, *SER0, SER1, SER2 and SER3*. Out of these 4 serial ports, *SER3* is set as the serial debug port use for *i.MX7* from Embedian. Users can change to any port they want to. *SER3* is exposed (along with all other serial ports available on the module) in the *SMARC-FiMX7* Evaluation Carrier. The default baud rate setting is *115,200 8N1*.
*SER3* pin out of the *SMARC-FiMX7* is shown below:

| NXP i.MX7 CPU | | SMARC-FiMX7 Edge Golden Finger | | Net Names | Notes |
|---|---|---|---|---|---|
| mode | Pin Name | Pin# | Pin Name | | |
| SER3 (Debugging Port) | | | | | |
| ALT0 | UART3_TX_DATA_ _UART3_TX_DATA | P140 | SER3_TX | SER3_TX | Asynchronous serial port data out |
| ALT0 | UART3_RX_DATA_ _UART3_RX_DATA | P141 | SER3_RX | SER3_RX | Asynchronous serial port data in |

## 2.3 Mechanical Specifications

### 2.3.1. Module Dimensions

The *SMARC-FiMX7* complies with *SMARC* Hardware Specification in an 82mm x 50 mm form factor.

### 2.3.2. Height on Top

2.9mm maximum (without PCB) complied with *SMARC* specification defines as 3mm as the maximum.

### 2.3.3. Height on Bottom

0.9mm maximum (without PCB) complied with *SMARC* specification defines as 1.3mm as the maximum.

### 2.3.4. Mechanical Drawings

The mechanical information is shown in Figure 12: *SMARC-FiMX7* Mechanical Drawings (Top View) and Figure 13: *SMARC-FiMX7* Mechanical Drawings (Bottom View))

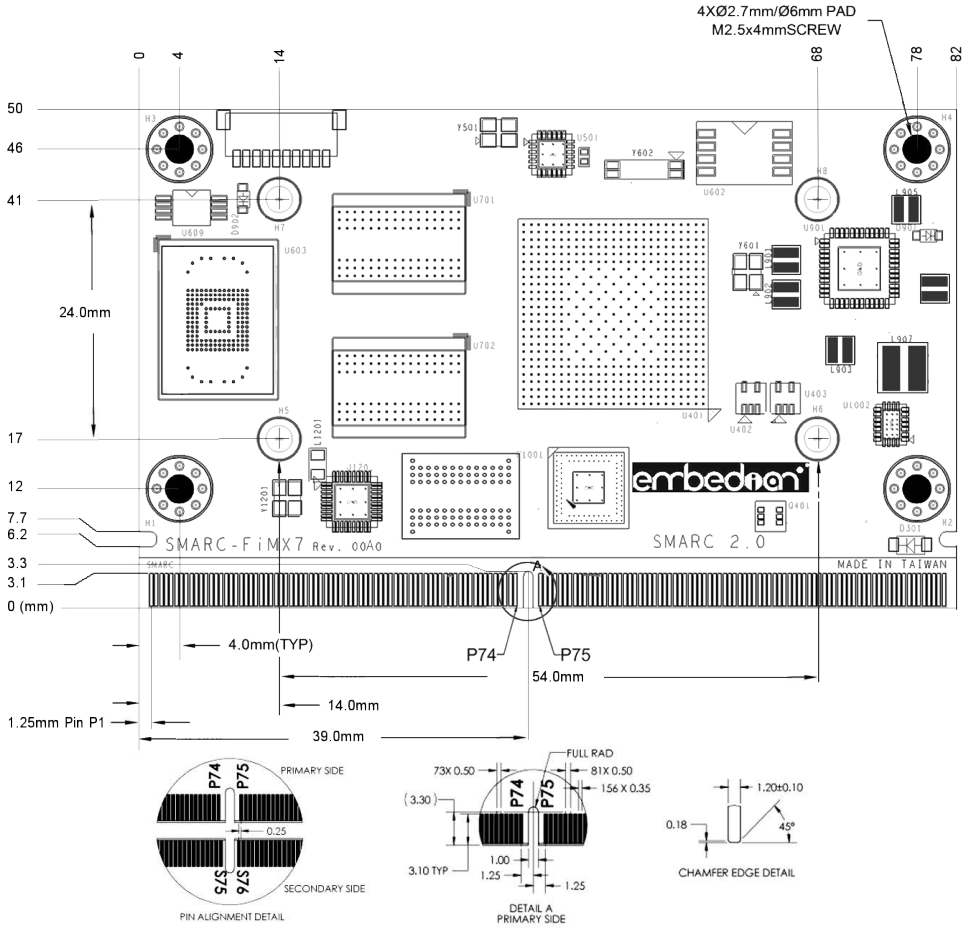



*Figure 12. SMARC-FiMX7 Mechanical Drawings (Top View)*

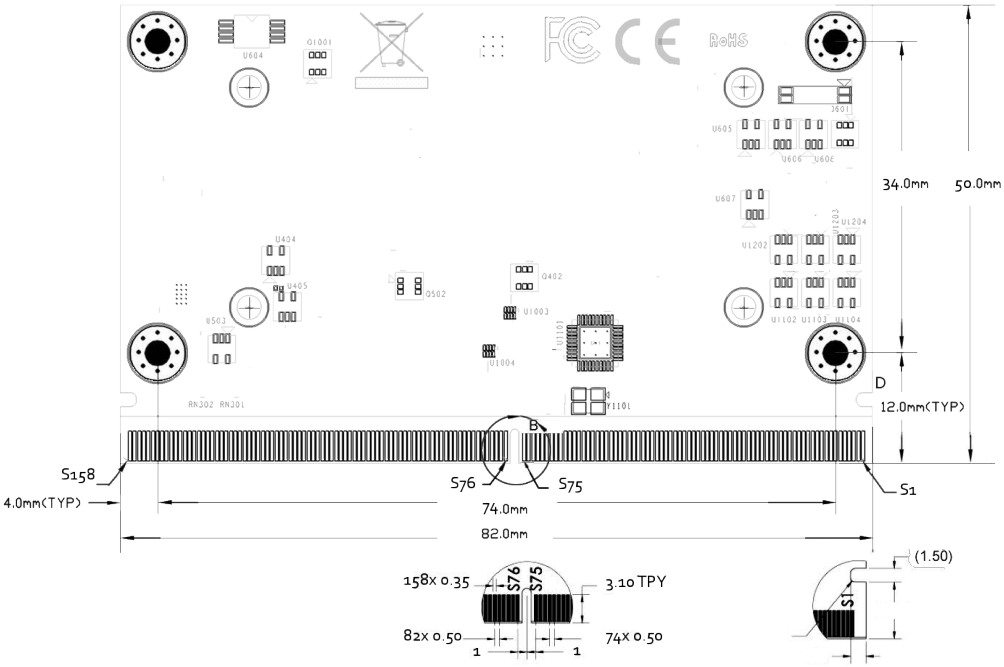



*Figure 13. SMARC-FiMX7 Mechanical Drawings (Bottom View)*

The figure on the following page details the 82mm x 50mm Module mechanical attributes, including the pin numbering and edge finger pattern.

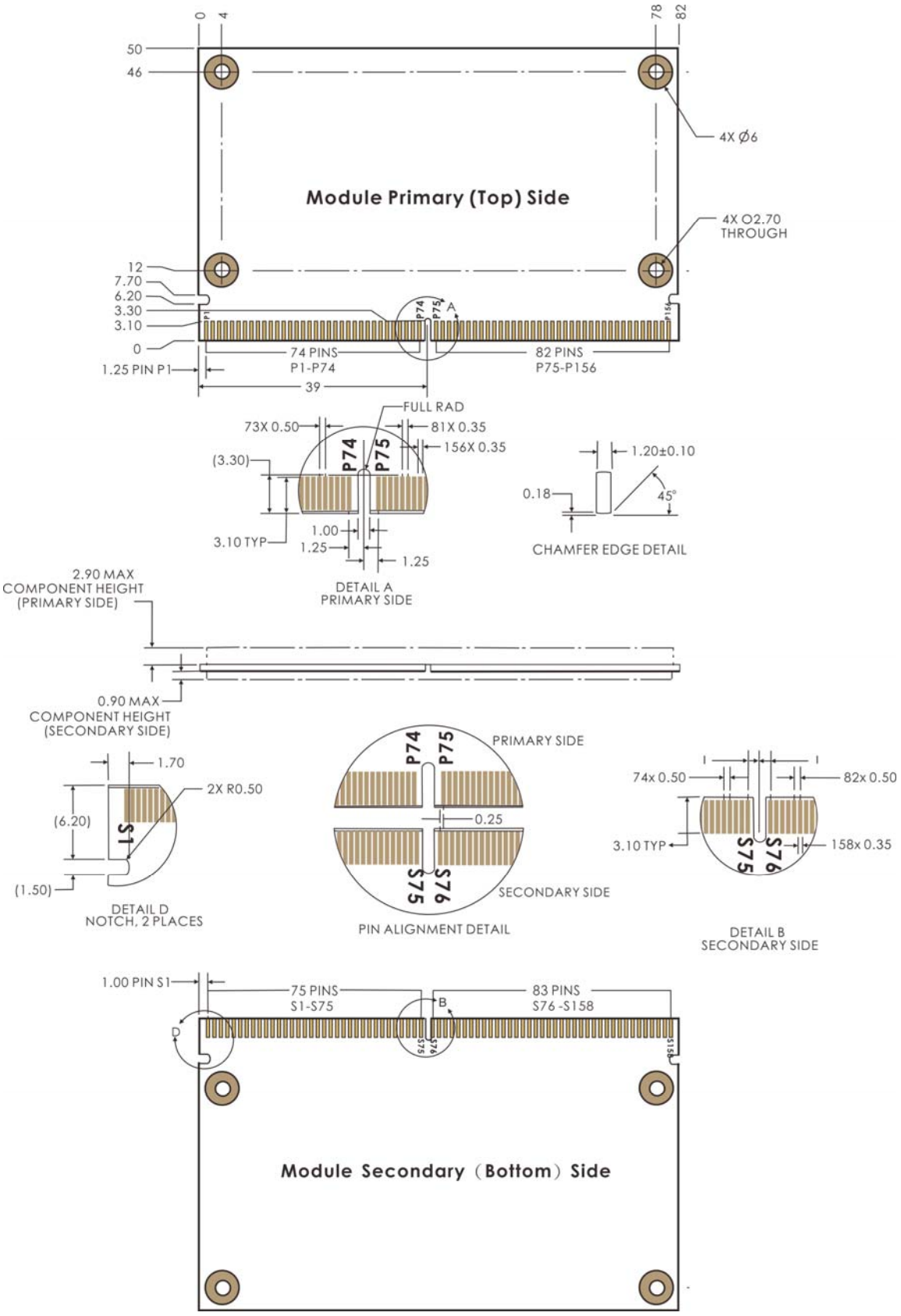



*Figure 14: SMARC-FiMX7 Module Mechanical Outline*

Top side major component (IC and Connector) information is shown in Figure 15: *SMARC-FiMX7* Top side components.

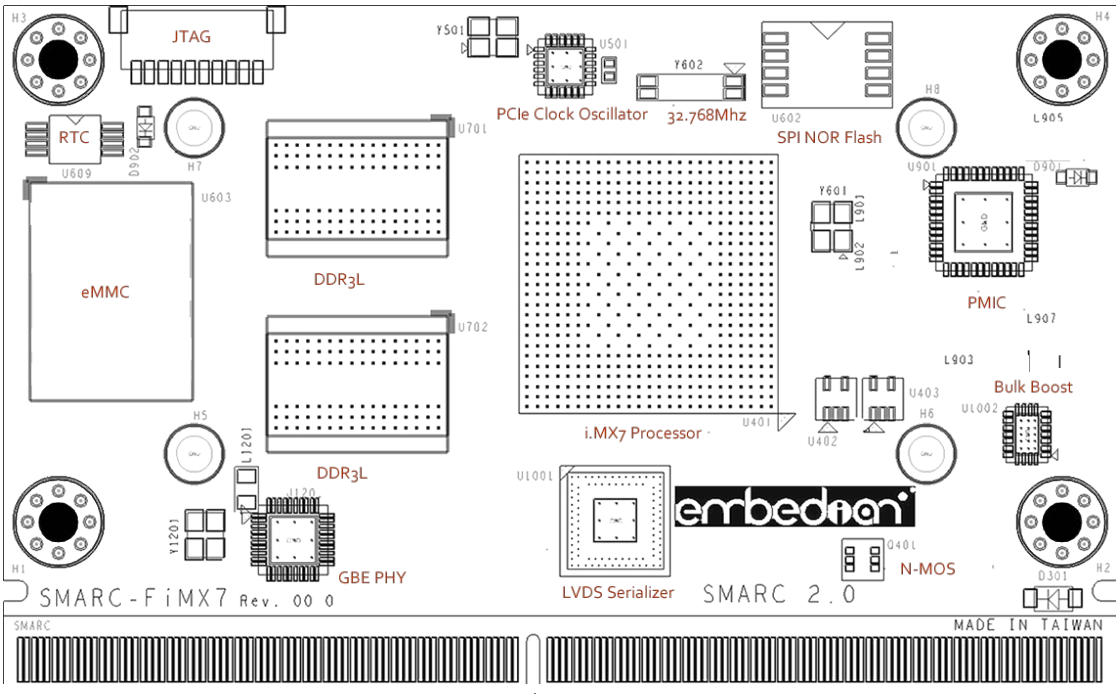



***Figure 15. SMARC-FiMX7 Top Side Components***

Bottom side major component (IC and Connector) information is shown in Figure 16: *SMARC-FiMX7* Bottom side components.

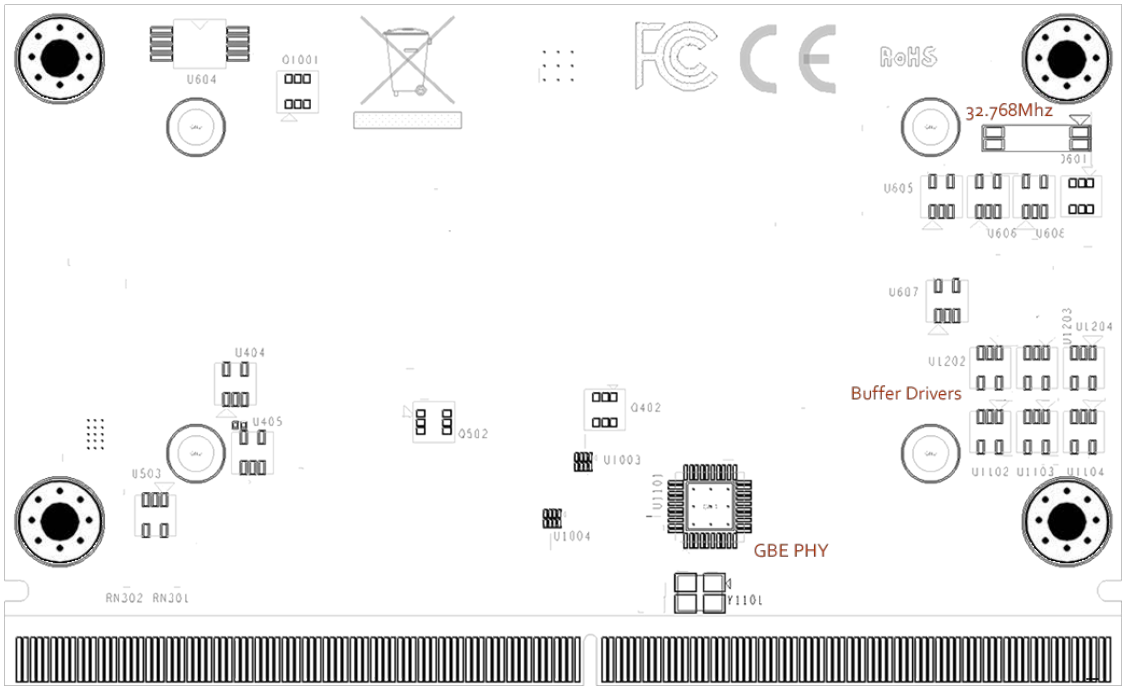



*Figure 16. SMARC-FiMX7 Bottom Side Components*

*SMARC-FiMX7* height information from Carrier board Top side to tallest Module component is shown in Figure 17: *SMARC-FiMX7* Minimum "Z" Height:

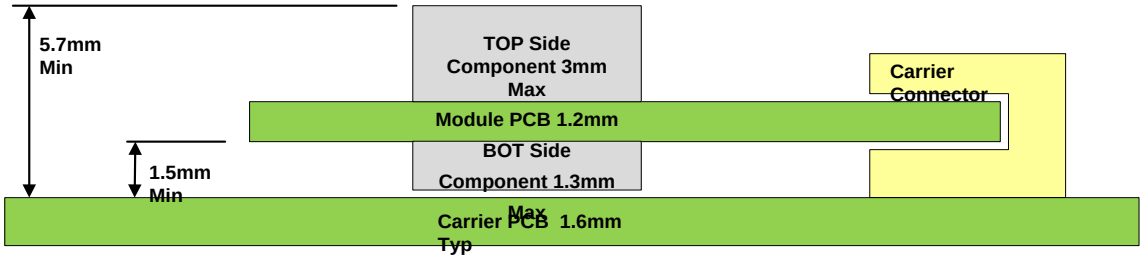



***Figure 17. SMARC-FiMX7 Minimum "Z" Height***

The *SMARC* connector board-to-board stack heights that are available may result in the use of non-standard spacer lengths. The board-to-board stack heights available include 1.5mm, 2.7mm and 5mm. Of these three, only the spacer for the 5mm stack would likely be a standard length.
When a 1.5mm stack height Carrier board connector is used, there shall not be components on the Carrier board Top side in the Module region. Additionally, when 1.5mm stack height connectors are used, there should not be PCB traces on the Carrier top side in the Module shadow. This is to prevent possible problems with metallic Module heat sink attachment hardware that may protrude through the Module.
If Carrier board components are required in this region, then the Carrier components must be on the Carrier Bottom side, or a taller Module-to-Carrier connector may be used. Stack heights of 2.7mm,
3mm, 5mm and up are available.

### 2.3.5. Carrier Board Connector PCB Footprint

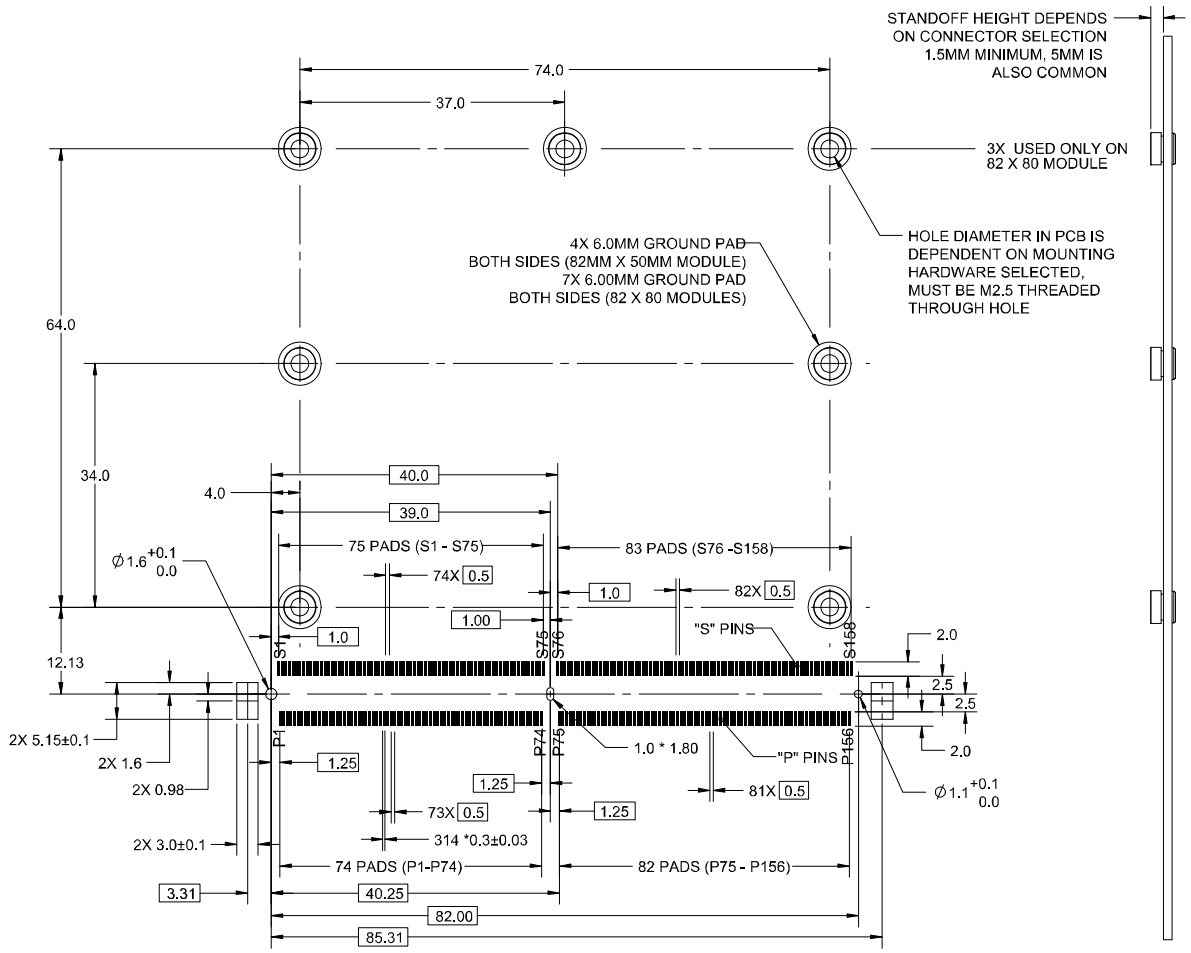



*Figure 18: Carrier Board Connector PCB Footprint*

#### Note:

The hole diameter for the 4 holes (82mm x 50mm Module) or 7 holes (82mm x 80mm Module) depends on the spacer hardware selection. See the section below for more information on this.

### 2.3.6. Module Assembly Hardware

The *SMARC-FiMX7* module is attached to the carrier with four M2.5 screws. A 4mm length screw is usually used. The attachment holes are located on the corners of the module. Attachment holes have a 6mm diameter pad, 2.7

mm dia drill hole as shown Figure 12: *SMARC-FiMX7* Mechanical Drawings (Top View)

### 2.3.7. Carrier Board Standoffs

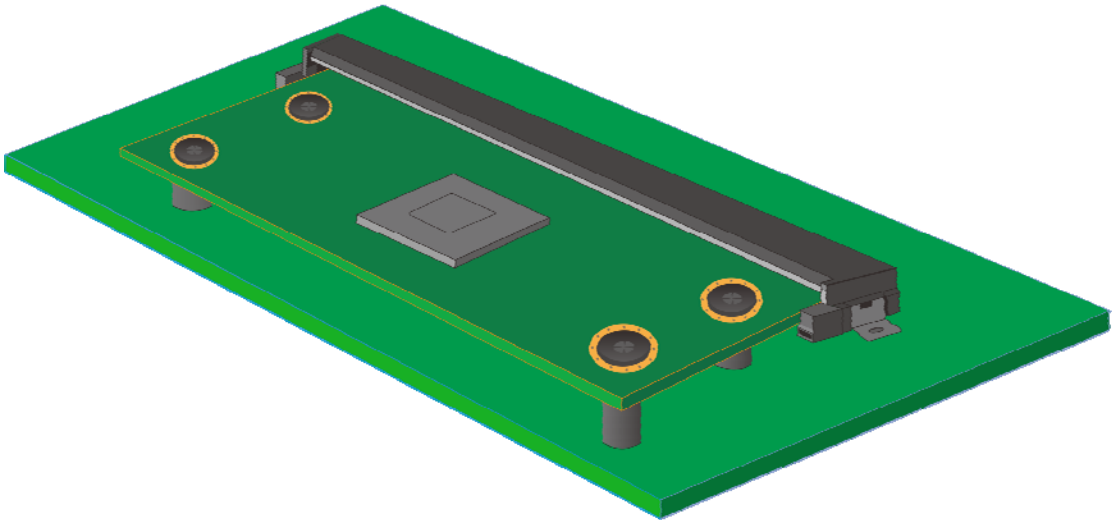


*Figure 19: Screw Fixation*

Standoffs secured to the Carrier board are expected. The standoffs are to be used with M2.5 hardware. Most implementations will use Carrier board standoffs that have M2.5 threads (as opposed to clearance holes). A short M2.5 screw and washer, inserted from the Module top side, secures the Module to the Carrier board threaded standoff.

The *SMARC* connector board-to-board stack heights that are available may result in the use of non-standard spacer lengths. The board-to-board stack heights available include 1.5mm, 2.7mm and 5mm. Of these three, only the spacer for the 5mm stack would likely be a standard length.

Penn Engineering and Manufacturing (PEM) (www.pemnet.com) makes surface mount spacers with M2.5 internal threads. The product line is called SMTSO (“surface mount technology stand offs”). The shortest standard length offered is 2mm. A custom part with 1.5mm standoff length, M2.5 internal thread, and 5.56mm standoff OD is available from PEM. The Carrier PCB requires a 4.22mm hole and 6.2mm pad to accept these parts.

Other vendors such as RAF Electronic Hardware (www.rafhdwe.com) offer M2.5 compatible swaged standoffs. Swaged standoffs require the use of a press and anvil at the CM. Their use is common in the industry. The standoff OD and Carrier PCB hole size requirements are different from the PEM SMTSO standoffs described above.

### 2.3.8. Carrier Connector

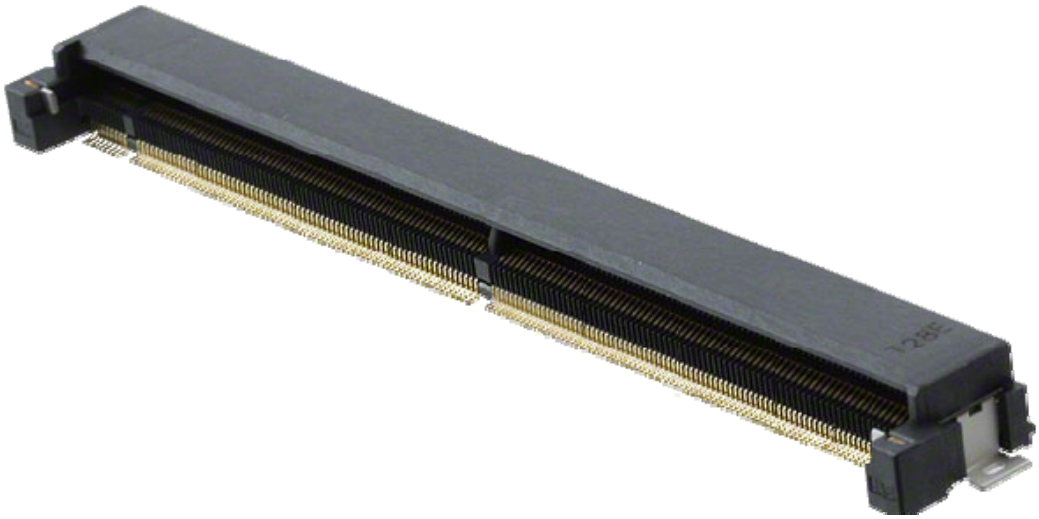


*Figure 20: MXM3 Carrier Connector*

The Carrier board connector is a 314 pin 0.5mm pitch right angle part designed for use with 1.2mm thick mating PCBs with the appropriate edge finger pattern. The connector is commonly used for MXM3 graphics cards. The *SMARC* Module uses the connector in a way quite different from the MXM3 usage.

| Vender | Vendor P/N | Stack Height | Body Height | Contact Plating | Pin Style | Body Color |
|---|---|---|---|---|---|---|
| Foxconn | AS0B821-S43B - *H | 1.5mm | 4.3mm | Flash | Std | Black |
| Foxconn | AS0B821-S43N - *H | 1.5mm | 4.3mm | Flash | Std | Ivory |
| Foxconn | AS0B826-S43B - *H | 1.5mm | 4.3mm | 10 u-in | Std | Black |
| Foxconn | AS0B826-S43N - *H | 1.5mm | 4.3mm | 10 u-in | Std | Ivory |
| | | | | | | |
| Lotes | AAA-MXM-008-P04_A | 1.5mm | 4.3mm | Flash | Std | Tan |
| Lotes | AAA-MXM-008-P03 | 1.5mm | 4.3mm | 15 u-in | Std | Tan |
| | | | | | | |
| Speedtech | B35P101-02111-H | 1.56mm | 4.0mm | Flash | Std | Black |
| Speedtech | B35P101-02011-H | 1.56mm | 4.0mm | Flash | Std | Tan |
| Speedtech | B35P101-02112-H | 1.56mm | 4.0mm | 10 u-in | Std | Black |
| Speedtech | B35P101-02012-H | 1.56mm | 4.0mm | 10 u-in | Std | Tan |
| Speedtech | B35P101-02113-H | 1.56mm | 4.0mm | 15 u-in | Std | Black |
| Speedtech | B35P101-02013-H | 1.56mm | 4.0mm | 15 u-in | Std | Tan |
| | | | | | | |
| Aces | 91781-314 2 8-001 | 2.7mm | 5.2mm | 3 u-in | Std | Black |
| | | | | | | |

| Vender | Vendor P/N | Stack Height | Body Height | Contact Plating | Pin Style | Body Color |
|---|---|---|---|---|---|---|
| Foxconn | AS0B821-S55B - *H | 2.7mm | 5.5mm | Flash | Std | Black |
| Foxconn | AS0B821-S55N - *H | 2.7mm | 5.5mm | Flash | Std | Ivory |
| Foxconn | AS0B826-S55B - *H | 2.7mm | 5.5mm | 10 u-in | Std | Black |
| Foxconn | AS0B826-S55N - *H | 2.7mm | 5.5mm | 10 u-in | Std | Ivory |
| | | | | | | |
| Speedtech | B35P101-02121-H | 2.76mm | 5.2mm | Flash | Std | Black |
| Speedtech | B35P101-02021-H | 2.76mm | 5.2mm | Flash | Std | Tan |
| Speedtech | B35P101-02122-H | 2.76mm | 5.2mm | 10 u-in | Std | Black |
| Speedtech | B35P101-02022-H | 2.76mm | 5.2mm | 10 u-in | Std | Tan |
| Speedtech | B35P101-02123-H | 2.76mm | 5.2mm | 15 u-in | Std | Black |
| Speedtech | B35P101-02023-H | 2.76mm | 5.2mm | 15 u-in | Std | Tan |
| | | | | | | |
| Foxconn | AS0B821-S78B - *H | 5.0mm | 7.8mm | Flash | Std | Black |
| Foxconn | AS0B821-S78N - *H | 5.0mm | 7.8mm | Flash | Std | Ivory |
| Foxconn | AS0B826-S78B - *H | 5.0mm | 7.8mm | 10 u-in | Std | Black |
| Foxconn | AS0B826-S78N - *H | 5.0mm | 7.8mm | 10 u-in | Std | Ivory |
| | | | | | | |
| Yamaichi (1) | CN113-314-2001 | 5.0mm | 7.8mm | 0.3 u-meter | Std | Black |

Other, taller stack heights may be available from these and other vendors. Stack heights as tall as 11mm are shown on the Aces web site.

**Note:**

1. *Yamaichi CN113-314-2001* is automotive grade.
2. The vendor drawings for the connectors listed above show a PCB footprint pattern for use with an MXM3 graphics card. This footprint, and the associated pin numbering, is not suitable for *SMARC* use. The

MXM3 standard gangs large groups of pins together to provide ~80W capable power paths needed for X86 graphics cards. The *SMARC* module “ungangs” these pins to allow more signal pins. Footprint and pin numbering information for application of this 314 pin connector to *SMARC* is given in the sections below.

### 2.3.9. Module Cooling Solution—Heat Spreader

A standard heat-spreader plate for use with the *SMARC* 82mm x 50mm form factor is described below. A standard heat spreader plate definition allows the customer to use a Module from multiple vendors.

The heat spreader plate is sized at 82mm x 42mm x 3mm, and sits 3mm above the *SMARC* Module. The heat spreader plate ‘Y’ dimension is deliberately set at 42mm and not 50mm, to allow the plate to clear the *SMARC* MXM3 connector. The plate is shown in the figures below.

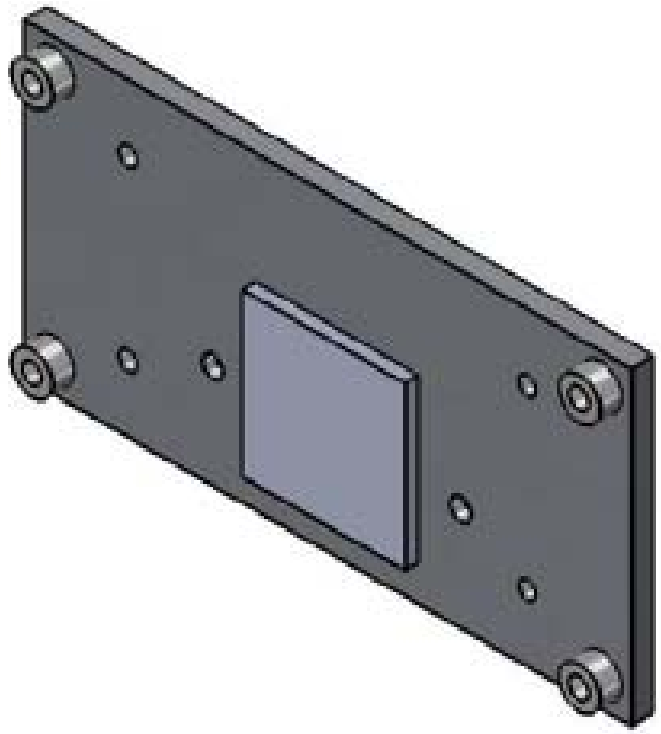


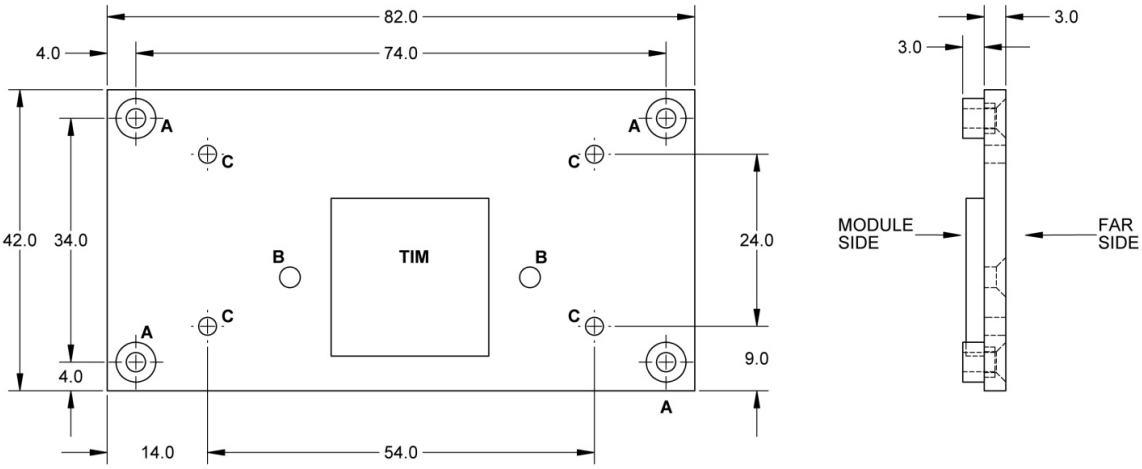
*Figure 21: Heat Spreader*

The internal square in the figure above is a thermally conductive and mechanically compliant Thermal Interface Material (or "*TIM*"). The exact X-Y position and Z thickness details of the TIM vary from design to design.

The two holes immediately adjacent to the *TIM* serve to secure the PCB in the SOC area and compress the *TIM*.

The four interior holes that are further from the center allow a heat sink to be attached to the heat spreader plate, or they can be used to secure the heat spreader plate to a chassis wall that serves as a heat sink.

Dimensions and further details may be found in the following figure.




Dimensions in the figure above are in millimeters. "*TIM*" stands for "Thermal Interface Material". The *TIM* takes up the small gap between the SOC top and the Module - facing side of the heat spreader.

| Hole Reference | Description | Size |
|---|---|---|
| **A** | *SMARC Module corner mounting holes Spacing determined by SMARC specification for 82mm x 50mm Modules.*<br><br>*Typically these holes have 3mm length press fit or swaged clearance standoffs on the Module side.*<br><br>*These holes are typically countersunk on the far side of the plate, to allow the heat spreader plate to be flush with a secondary heat sink.* | *Hole size depends on standoffs used. Standoff diameter must be compatible with SMARC Module mounting hole pad and hole size (6.0mm pads, 2.7mm holes on the Module). The holes and standoffs are for use with M2.5 screw hardware.*<br><br>*The far side of these holes are counter-sunk to allow the attachment screw to be flush with the far side heat spreader surface.* |
| **B** | *Not Defined* | |
| **C** | *Fixed location holes to allow the attachment of a heat sink to the heat spreader, or to allow the heat spreader to be secured to a chassis wall that can serve as a heat sink.* | *M3 threaded holes* |

## 2.4 Electrical Specifications

### 2.4.1. Supply Voltage

The *SMARC-FiMX7* module operates over an input voltage range of 3.0V to 5.25V. Power is provided from the carrier through 10 power pins as defined by the *SMARC* specification.

***Caution!*** A single *5V DC* input is recommended.

### 2.4.2. RTC/Backup Voltage

3.0V RTC backup power is provided through the VDD_RTC pin from the carrier board. This connection provides back up power to the module PMIC. The RTC is powered via the primary system 3.3V supply during normal operation and via the VBAT power input, if it is present, during power-off.

### 2.4.3. No Separate Standby Voltage

The *SMARC-FiMX7* does not have a standby power rail. Standby operation is powered through the main supply voltage rail, as defined in the *SMARC* specification.

### 2.4.4. Module I/O Voltage

The *SMARC-FiMX7* module supports 1.8V (*SMARC* v2.0 compliant) level I/O voltage depending on the part number that users selected.

### 2.4.5. MTBF

The *SMARC-FiMX7* System *MTBF* (hours) : >100,000 hours

The above MTBF (Mean Time Between Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and a Bellcore calculation for the remaining parts. The Bellcore calculation used is "Method 1 Case 1". In that particular method the components are assumed to be operating at a 50 % stress level in a 40° C ambient environment and the system is assumed to have not been burned in. Manufacturer's data has been used wherever possible. The manufacturer's data, when used, is specified at 50°C, so in that sense the following results are slightly conservative. The MTBF values shown below are for a 40°C in an office or telecommunications environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, salt water exposure, etc.) lower MTBF values.

### 2.4.6. Power Consumption

The power consumption values listed in this document were measured under a controlled environment. The hardware used for testing includes an *SMARC-FiMX7* module, carrier board for *SMARC* ARM, TFT monitor, micro-SD card and USB keyboard. The carrier board was powered externally by a power supply unit so that it does not influence the power consumption value that is measured for the module. The USB keyboard was detached once the module was configured within the OS. All recorded values were averaged over a 30 second time period. The modules were cooled by the heatspreader specific to the module variants.

Each module was measured while running 32 bit Linaro Ubuntu 14.04. To measure the worst case power consumption, the cooling solution was removed and the CPU core temperature was allowed to run between 95° and 100°C at 100% workload. The peak current value was then recorded. This value should be taken into consideration when designing the system's power supply to ensure that the power supply is sufficient during worst case scenarios.

Power consumption values were recorded during the following stages:
Linaro Ubuntu 14.04 (32 bit)

- Desktop Idle
- 100% CPU workload
- 100% CPU workload at approximately 100°C peak power consumption

***Note:*** With the linux stress tool, we stressed the CPU to maximum frequency.

The table below provides additional information about the different variants offered by the *SMARC-FiMX7*.

#### 2.4.6.1. NXP i.MX7 Cortex A7 800MHz Solo Core 512KB L2 Cache

With 4GB onboard eMMC.

| P/N: SMARC-FiMX7-S | NXP i.MX7 Cortex A7 800MHz Solo Core 512KB L2 Cache | | |
|---|---|---|---|
| Memory Size | 512MB | | |
| Operating System | Ubuntu 14.04 | | |
| Power States | Desktop Idle | 100% workload | Max. power consumption |
| Power Consumption (Amp/Watts) | 015A/0.74W | 0.18A/0.9W | 0.29A/1.45W |

#### 2.4.6.2. NXP i.MX7 Cortex A7 1.2GHz Dual Core 512KB L2 Cache

With 4GB onboard eMMC.

| P/N: SMARC-FiMX7-U | NXP i.MX7 Cortex A7 1.2GHz Dual Lite Core 512KB L2 Cache | | |
|---|---|---|---|
| Memory Size | 1GB | | |
| Operating System | Ubuntu 14.04 | | |
| Power States | Desktop Idle | 100% workload | Max. power consumption |
| Power Consumption (Amp/Watts) | 0.16A/0.8W | 0.22A/1.1W | 0.44A/2.2W |

## 2.5 Environmental Specifications

### 2.5.1. Operating Temperature

The *SMARC-FiMX7* module operates from *-20°C to 85°C* air temperature (so-called “extended temperature”), without a passive heat sink arrangement.

### 2.5.2. Humidity

Operating: 10% to 90% *RH* (non-condensing).
Non-operating: 5% to 95% *RH* (non-condensing).

### 2.5.3. ROHS/REACH Compliance

The *SMARC-FiMX7* module is compliant to the 2002/95/EC *RoHS* directive and *REACH* directive.


# Connector PinOut

This Chapter gives detail pinout of *SMARC-FiMX7* golden finger edge connector.

Section include：

- *SMARC-FiMX7* Connector Pin Mapping

# Chapter 3 Connector Pinout

The Module pins are designated as *P1 – P156* on the Module Primary (Top) side, and *S1 – S158* on the Module Secondary (Bottom) side. There are total of 314 pins on the Module. The connector is sometimes identified as a 321 pin connector, but 7 pins are lost to the key (4 on the primary side and 3 on secondary side).

The Secondary (Bottom) side faces the Carrier board when a normal or standard Carrier connector is used.

The *SMARC-FiMX7* module pins are deliberately numbered as *P1 – P156* and *S1 – S158* for clarity and to differentiate the *SMARC* Module from MXM3 graphics modules, which use the same connector but use the pins for very different functions. *MXM*3 cards and *MXM3* baseboard connectors use different pin numbering scheme.

## 3.1 SMARC-FiMX7 Connector Pin Mapping

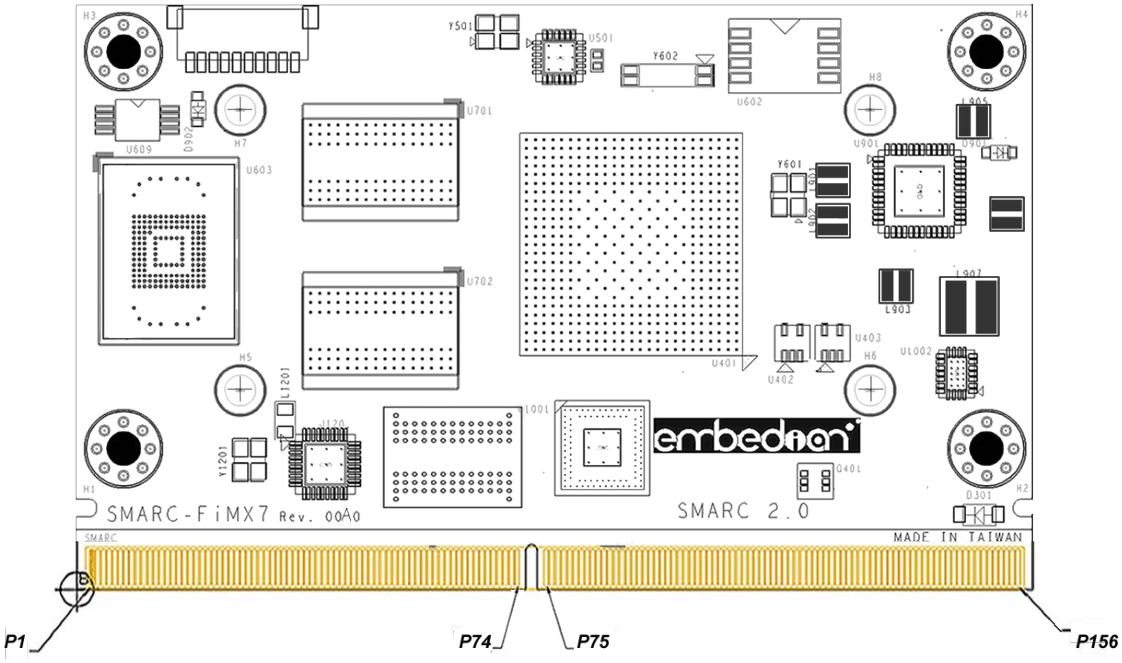



*Figure 22: SMARC-FiMX7 edge finger primary pins*

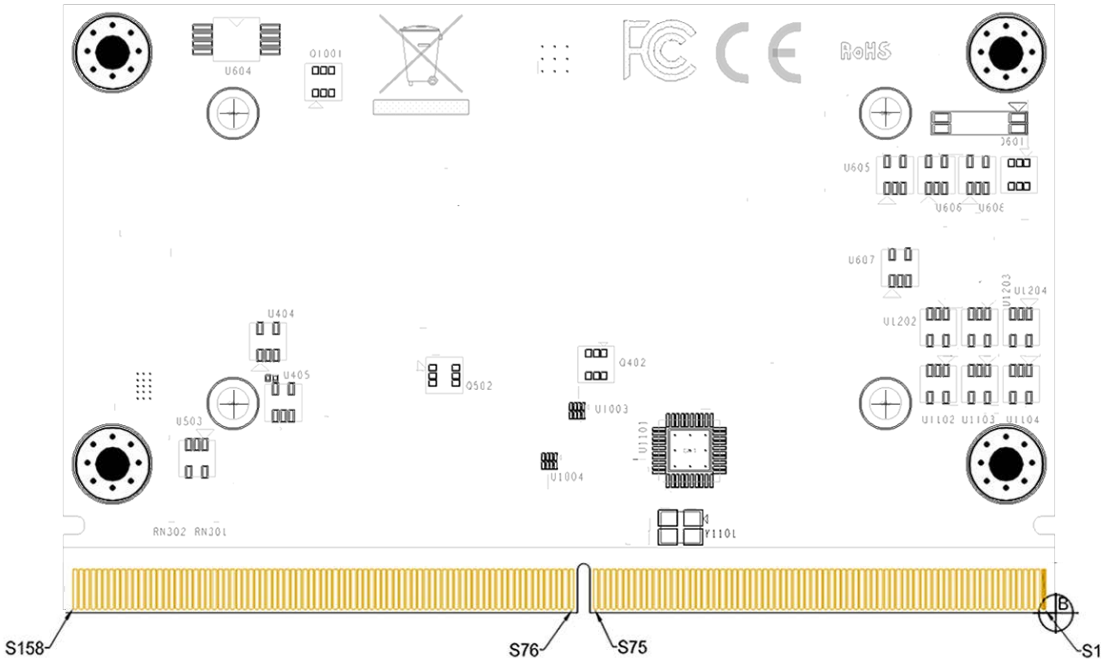



*Figure 23: SMARC-FiMX7 edge finger secondary pins*

The next tables describe each pin, its properties, and its use on the module and development board.

The "*SMARC Edge Finger*" column shows the connection of the signals defined in the *SMARC* specification. The "*NXP i.MX7 CPU*" column shows the connection of the CPU signals on the module. The format of this column is "*Ball/Mode/Signal Name*" where "*Signal Name*" is the chip where the signals are connected, and "*Ball*" is the name of the pad where the signals are connected as they are defined in the *i.MX7* processor datasheet. The grey text stands for the pins are not connected from *SMARC-FiMX7* module.

### Pinout Legend

| | |
|---|---|
| ***I*** | *Input* |
| ***O*** | *Output* |
| ***I/O*** | *Input or output* |
| ***P*** | *Power* |
| ***AI*** | *Analogue input* |
| ***AO*** | *Analogue output* |
| ***AIO*** | *Analogue Input or analogue output* |
| ***OD*** | *Open Drain Signal* |
| ***#*** | *Low level active signal* |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| P1 | SMB_ALERT_1V8# | | | | | Not used |
| P2 | GND | | | | P | Ground |
| P3 | CSI1_CK+ | B15 | | MIPI_CSI_CLK_P | I | CSI1 differential clock inputs |
| P4 | CSI1_CK- | A15 | | MIPI_CSI_CLK_N | I | CSI1 differential clock inputs |
| P5 | GBE1_SDP | | | | | Not used |
| P6 | GBE0_SDP | | | | | Not used |
| P7 | CSI1_RX0+ | B16 | | MIPI_CSI_D0_P | I | CSI1 differential data inputs 0 |
| P8 | CSI1_RX0- | A16 | | MIPI_CSI_D0_N | I | CSI1 differential data input 0 |
| P9 | GND | | | | P | Ground |
| P10 | CSI1_RX1+ | B14 | | MIPI_CSI_D1_P | I | CSI1 differential data input 1 |
| P11 | CSI1_RX1- | A14 | | MIPI_CSI_D1_N | I | CSI1 differential data inputs 1 |
| P12 | GND | | | | P | Ground |
| P13 | CSI1_RX2+ | | | | | Not used |
| P14 | CSI1_RX2- | | | | | Not used |
| P15 | GND | | | | P | Ground |
| P16 | CSI1_RX3+ | | | | | Not used |
| P17 | CSI1_RX3- | | | | | Not used |
| P18 | GND | | | | P | Ground |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| P19 | GbE0_MDI3- | | | | AIO | Qualcomm AR8035 Differential Transmit/Receive Negative Channel 3 |
| P20 | GbE0_MDI3+ | | | | AIO | Qualcomm AR8035 Differential Transmit/Receive Positive Channel 3 |
| P21 | GbE0_LINK100# | | | | O OD | Link Speed Indication LED for 100Mbps Could be able to sink 24mA or more Carrier LED current |
| P22 | GbE0_LINK1000# | | | | O OD | Link Speed Indication LED for 1000Mbps Could be able to sink 24mA or more Carrier LED current |
| P23 | GbE0_MDI2- | | | | AIO | Qualcomm AR8035 Differential Transmit/Receive Negative Channel 2 |
| P24 | GbE0_MDI2+ | | | | AIO | Qualcomm AR8035 Differential Transmit/Receive Positive Channel 2 |
| P25 | GbE0_LINK_ACT# | | | | O OD | Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity Could be able to sink 24mA or more Carrier LED current |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| P26 | GbE0_MDI1- | | | | AIO | Qualcomm AR8035 Differential Transmit/Receive Negative Channel 1 |
| P27 | GbE0_MDI1+ | | | | AIO | Qualcomm AR8035 Differential Transmit/Receive Positive Channel 1 |
| P28 | GbE0_CTREF | | | | O | Qualcomm AR8035 Center tap reference voltage for GBE Carrier board Ethernet magnetic |
| P29 | GbE0_MDI0- | | | | AIO | Qualcomm AR8035 Differential Transmit/Receive Negative Channel 0 |
| P30 | GbE0_MDI0+ | | | | AIO | Qualcomm AR8035: Differential Transmit/Receive Positive Channel 0 |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| P31 | SPI0_CS1# | L3 | ALT3 | UART1_RXD__ ECSPI1_SS1 | O | SPI0 Master Chip Select 1 output. |
| P32 | GND | | | | P | Ground |
| P33 | SDIO_WP | C4 | ALT0 | SD1_WP__ SD1_WP | I | Write Protect |
| P34 | SDIO_CMD | C5 | ALT0 | SD1_CMD__ SD1_CMD | IO | Command Line |
| P35 | SDIO_CD# | C6 | ALT0 | SD1_CD__ SD1_CD | I | Card Detect |
| P36 | SDIO_CK | B5 | ALT0 | SD1_CLK__ SD1_CLK | O | Clock |
| P37 | SDIO_PWR_EN | B4 | ALT0 | SD1_RESET_B__ SD1_RESET_B | O | SD card power enable |
| P38 | GND | | | | P | Ground |
| P39 | SDIO_D0 | A5 | ALT0 | SD1_DATA0__ SD1_DATA0 | IO | Data path |
| P40 | SDIO_D1 | D6 | ALT0 | SD1_DATA1__ SD1_DATA1 | IO | Data path |
| P41 | SDIO_D2 | A4 | ALT0 | SD1_DATA2__ SD1_DATA2 | IO | Data path |
| P42 | SDIO_D3 | D5 | ALT0 | SD1_DATA3__ SD1_DATA3 | IO | Data path |
| P43 | SPI0_CS0# | H5 | ALT0 | ECSPI1_SS0__ ECSPI1_SS0 | O | SPI0 Master Chip Select 0 output, |
| P44 | SPI0_CK | H3 | ALT0 | ECSPI1_SCLK_ ECSPI1_SCLK | O | SPI0 Master Clock output |
| P45 | SPI0_DIN | H4 | ALT0 | ECSPI1_MISO__ ECSPI1_MISO | I | SPI0 Master Data input (input to CPU, output from SPI device) |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| P46 | SPI0_DO | G5 | ALT0 | ECSPI1_MOSI__ ECSPI1_MOSI | O | SPI0 Master Data output (output from CPU, input to SPI device) |
| P47 | GND | | | | P | Ground |
| P48 | SATA_TX+ | | | | | Not used |
| P49 | SATA_TX- | | | | | Not used |
| P50 | GND | | | | P | Ground |
| P51 | SATA_RX+ | | | | | Not used |
| P52 | SATA_RX- | | | | | Not used |
| P53 | GND | | | | P | Ground |
| P54 | ESPI1_CS0# | E8 | ALT1 | SAI2_TXD__ ECSPI1_SS0 | O | SPI1 Master Chip Select 0 output |
| P55 | ESPI1_CS1# | D3 | ALT3 | SD2_CD_B__ ECSP3_SS2 | O | SPI1 Master Chip Select 1 output |
| P56 | ESPI1_CK | E9 | ALT1 | SAI2_RXD__ ECSPI1_SCLK | O | SPI1 Master Clock output |
| P57 | ESPI1_IO_0 | D9 | ALT1 | SAI2_TXFS__ ECSPI3_MISO | I | SPI1 Master Data input (input to CPU, output from SPI device) |
| P58 | ESPI1_IO_1 | D8 | ALT1 | SAI2_TXC__ ECSPI3_MOSI | O | SPI1 Master Data output (output from CPU, input to SPI device) |
| P59 | GND | | | | P | Ground |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| P60 | USB0+ | B8 | | USB_OTG1_DP | B8 | Differential USB0 data |
| P61 | USB0- | A8 | | USB_OTG1_DN | A8 | Differential USB0 data |
| P62 | USB0_EN_OC# | N6<br>P1 | ALT1<br>ALT1 | GPIO1_IO04__USB_OTG1_OC<br>GPIO1_IO05__USB_OTG1_PWR | N6<br>P1 | Pulled low by Module OD driver to disable USB0 power<br>Pulled low by Carrier OD driver to indicate over-current situation<br>If this signal is used, a pull-up is required on the Carrier |
| P63 | USB0_VBUS_DET | C8 | | Turn on USB_OTG_VBUS | C8 | USB host power detection, when this port is used as a device |
| P64 | USB0_OTG_ID | B7 | | USB_OTG1_ID | B7 | USB OTG ID input, active high |
| P65 | USB1+ | B10 | | USB_OTG2_DP | IO | Differential USB0 data pair |
| P66 | USB1- | A10 | | USB_OTG2_DN | IO | |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| P67 | USB1_EN_OC# | P2<br>P3 | ALT1<br>ALT1 | GPIO1_IO06__USB_OTG2_OC<br>GPIO1_IO07__USB_OTG2_PWR | IO OD | Pulled low by Module OD driver to disable USB0 power<br>Pulled low by Carrier OD driver to indicate over-current situation<br>If this signal is used, a pull-up is required on the Carrier |
| P68 | GND | | | | P | Ground |
| P69 | USB2+ | | | | | Not used |
| P70 | USB2- | | | | | Not used |
| P71 | USB2_EN_OC# | | | | | Not used |
| P72 | RSVD | | | | | Not used |
| P73 | RSVD | | | | | Not used |
| P74 | USB3_EN_OC# | | | | | Not used |
| P75 | PCIE_A_RST# | K24 | ALT5 | EPDC_BDR0__GPIO2_IO28 | O | Reset Signal for external devices. |
| P76 | USB4_EN_OC# | | | | | Not used |
| P77 | RSVD | | | | | Not used |
| P78 | RSVD | | | | | Not used |
| P79 | GND | | | | P | Ground |
| P80 | PCIE_C_REFCK+ | | | | | Not used |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| P81 | PCIE_C_REFCK- | | | | | Not used |
| P82 | GND | | | | P | Ground |
| P83 | PCIE_A_REFCK+ | AC10 | | PCIE_ REFCLKOUT_P | O | Differential PCI Express Reference Clock Signals for Lanes A |
| P84 | PCIE_A_REFCK- | AB10 | | PCIE_ REFCLKOUT_N | O | Differential PCI Express Reference Clock Signals for Lanes A |
| P85 | GND | | | | P | |
| P86 | PCIE_A_RX+ | AD11 | | PCIE_RX_P | I | Differential PCIe Link A receive data pair 0 |
| P87 | PCIE_A_RX- | AE11 | | PCIE_RX_N | I | Differential PCIe Link A receive data pair 0 |
| P88 | GND | | | | P | Ground |
| P89 | PCIE_A_TX+ | AB11 | | PCIE_TX_P | O | Differential PCIe Link A transmit data pair 0 |
| P90 | PCIE_A_TX- | AC11 | | PCIE_TX_N | O | Differential PCIe Link A transmit data pair 0 |
| P91 | GND | | | | P | Ground |
| P92 | HDMI_D2+ / DP1_LANE0+ | | | | | Not used |
| P93 | HDMI_D2- / DP1_LANE0- | | | | | Not used |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| P94 | GND | | | | P | Ground |
| P95 | HDMI_D1+ / DP1_LANE1+ | | | | | Not used |
| P96 | HDMI_D1- / DP1_LANE1- | | | | | Not used |
| P97 | GND | | | | P | Ground |
| P98 | HDMI_D0+ / DP1_LANE2+ | | | | | Not used |
| P99 | HDMI_D0- / DP1_LAN2- | | | | | Not used |
| P100 | GND | | | | P | Ground |
| P101 | HDMI_CK+ / DP1_LANE3+ | | | | | Not used |
| P102 | HDMI_CK- / DP1_LANE3- | | | | | Not used |
| P103 | GND | | | | P | Ground |
| P104 | HDMI_HPD / DP1_HPD | | | | | Not used |
| P105 | HDMI_CTRL_CK / DP1_AUX+ | | | | | Not used |
| P106 | HDMI_CTRL_DAT / DP1_AUX- | | | | | Not used |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| P107 | DP1_AUX_SEL | | | | | Not used |
| P108 | GPIO0 / CAM0_PWR# | P20 | ALT5 | EPDC_DATA00__ GPIO2_IO00 | IO | Camera 0 Power Enable, active low output |
| P109 | GPIO1 / CAM1_PWR# | P21 | ALT5 | EPDC_DATA01__ GPIO2_IO01 | IO | Camera 1 Power Enable, active low output |
| P110 | GPIO2 / CAM0_RST# | N20 | ALT5 | EPDC_DATA02__ GPIO2_IO02 | IO | Camera 0 Reset, active low output |
| P111 | GPIO3 / CAM1_RST# | N21 | ALT5 | EPDC_DATA03__ GPIO2_IO03 | IO | Camera 1 Reset, active low output |
| P112 | GPIO4 / HDA_RST# | N22 | ALT5 | EPDC_DATA04__ GPIO2_IO04 | IO | HD Audio Reset, active low output |
| P113 | GPIO5 / PWM_OUT | N2 | ALT1 | GPIO1_IO01__ PWM1 | IO | PWM output |
| P114 | GPIO6 / TACHIN | M20 | ALT5 | EPDC_DATA05__ GPIO2_IO05 | IO | Tachometer input (used with the GPIO5 PWM) |
| P115 | GPIO7 / PCAM_FLD | M22 | ALT5 | EPDC_DATA07__ GPIO2_IO07 | IO | PCAM_FLD (Field) signal input |
| P116 | GPIO8 / CAN0_ERR# | M21 | ALT5 | EPDC_DATA06__ GPIO2_IO06 | IO | CAN0 Error signal, active low input |
| P117 | GPIO9 / CAN1_ERR# | L4 | ALT5 | UART1_TXD__ GPIO4_IO01 | IO | CAN1 Error signal, active low input |
| P118 | GPIO10 | M5 | ALT5 | UART3_RTS__ GPIO4_IO06 | IO | |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| P119 | GPIO11 | M6 | ALT5 | UART3_CTS__ GPIO4_IO07 | IO | |
| P120 | GND | | | | P | |
| P121 | I2C_PM_CK | J2 | ALT0 | I2C1_SCL__ I2C1_SCL | IO OD | Power management I2C bus clock |
| P122 | I2C_PM_DAT | K1 | ALT0 | I2C1_SDA__ I2C1_SDA | IO OD | Power management I2C bus data |
| P123 | BOOT_SEL0# | | | | I | SYSBOOT and Line De-multiplexer Logic Pulled up on Module. Driven by OD part on Carrier. |
| P124 | BOOT_SEL1# | | | | I | SYSBOOT and Line De-multiplexer Logic Pulled up on Module. Driven by OD part on Carrier. |
| P125 | BOOT_SEL2# | | | | I | SYSBOOT and Line De-multiplexer Logic Pulled up on Module. Driven by OD part on Carrier. |
| P126 | RESET_OUT# | | | | O | General purpose reset output to Carrier board. |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| P127 | RESET_IN# | | | | I | Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise<br>Pulled up on Module.<br>Driven by OD part on Carrier. |
| P128 | POWER_BTN# | AC8 | | ONOFF | I | Power-button input from carrier board. Carrier to float the line in in-active state. Active low, level sensitive. It is de-bounced on the Module<br>Pulled up on Module.<br>Driven by OD part on Carrier. |
| P129 | SER0_TX | L25 | ALT3 | EPDC_DATA09__ UART6_TX_DATA | O | Asynchronous serial port data out |
| P130 | SER0_RX | M23 | ALT3 | EPDC_DATA08__ UART6_RX_DATA | I | Asynchronous serial port data in |
| P131 | SER0_RTS# | L24 | ALT3 | EPDC_DATA10__ UART6_RTS_B | O | Request to Send handshake line for SER0 |
| P132 | SER0_CTS# | L23 | ALT3 | EPDC_DATA11__ UART6_CTS_B | I | Clear to Send handshake line for SER0 |
| P133 | GND | | | | P | Ground |
| P134 | SER1_TX | L6 | ALT0 | UART2_TX_DATA__ UART2_TX_DATA | O | Asynchronous serial port data out |
| P135 | SER1_RX | L5 | ALT0 | UART2_RX_DATA__ UART2_RX_DATA | I | Asynchronous serial port data in |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| P136 | SER2_TX | L21 | ALT3 | EPDC_DATA13__ UART7_TX_DATA | O | Asynchronous serial port data out |
| P137 | SER2_RX | L22 | ALT3 | EPDC_DATA12__ UART7_RX_DATA | I | Asynchronous serial port data in |
| P138 | SER2_RTS# | L20 | ALT3 | EPDC_DATA14__ UART7_RTS_B | O | Request to Send handshake line for SER2 |
| P139 | SER2_CTS# | K25 | ALT3 | EPDC_DATA15__ UART7_CTS_B | I | Clear to Send handshake line for SER2 |
| P140 | SER3_TX | M2 | ALT0 | UART3_TX_DATA__ UART3_TX_DATA | O | Asynchronous serial port data out |
| P141 | SER3_RX | M1 | ALT0 | UART3_RX_DATA__ UART3_RX_DATA | I | Asynchronous serial port data in |
| P142 | GND | | | | P | Ground |
| P143 | CAN0_TX | T3 | ALT3 | GPIO1_IO13__ FLEXCAN1_TX | O | CAN0 Transmit output |
| P144 | CAN0_RX | T2 | ALT3 | GPIO1_IO12__ FLEXCAN1_RX | I | CAN0 Receive input |
| P145 | CAN1_TX | T6 | ALT3 | GPIO1_IO15__ FLEXCAN2_TX | O | CAN1 Transmit output |
| P146 | CAN1_RX | T5 | ALT3 | GPIO2_IO14__ FLEXCAN2_RX | I | CAN1 Receive input |
| P147 | VDD_IN | | | | P | Power in |
| P148 | VDD_IN | | | | P | Power in |
| P149 | VDD_IN | | | | P | Power in |
| P150 | VDD_IN | | | | P | Power in |
| P151 | VDD_IN | | | | P | Power in |
| P152 | VDD_IN | | | | P | Power in |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| P153 | VDD_IN | | | | P | Power in |
| P154 | VDD_IN | | | | P | Power in |
| P155 | VDD_IN | | | | P | Power in |
| P156 | VDD_IN | | | | P | Power in |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| S1 | CS1_TX+ / I2C_CAM1_CK | L1 | ALT0 | I2C4_SCL__ I2C4_SCL | IO OD | Camera I2C bus clock |
| S2 | CS1_TX- / I2C_CAM1_DAT | L2 | ALT0 | I2C4_SDA__ I2C4_SDA | IO OD | Camera I2C bus data |
| S3 | GND | | | | P | Ground |
| S4 | RSVD | | | | | Not used |
| S5 | CSI0_TX- / I2C_CAM0_CK | | | | | Not used |
| S6 | CAM_MCK | N5 | ALT5 | GPIO1_IO03__ CCM_CLKO2 | O | Master clock output for CSI camera support |
| S7 | CSI0_TX+ / I2C_CAM0_DAT | | | | | Not used |
| S8 | CSI0_CK+ | | | | | Not used |
| S9 | CSI0_CK- | | | | | Not used |
| S10 | GND | | | | P | Ground |
| S11 | CSI0_RX0+ | | | | | Not used |
| S12 | CSI0_RX0- | | | | | Not used |
| S13 | GND | | | | P | Ground |
| S14 | CSI0_RX1+ | | | | | Not used |
| S15 | CSI0_RX1- | | | | | Not used |
| S16 | GND | | | | P | Ground |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| S17 | GbE1_MDI0+ | | | | AIO | Qualcomm AR8035 Differential Transmit/Receive Positive Channel 0 |
| S18 | GbE1_MDI0- | | | | AIO | Qualcomm AR8035: Differential Transmit/Receive Negative Channel 0 |
| S19 | GbE1_LINK100# | | | | O OD | Link Speed Indication LED for 100Mbps Could be able to sink 24mA or more Carrier LED current |
| S20 | GbE1_MDI1+ | | | | AIO | Qualcomm AR8035 Differential Transmit/Receive Positive Channel 1 |
| S21 | GbE1_MDI1- | | | | AIO | Qualcomm AR8035 Differential Transmit/Receive Negative Channel 1 |
| S22 | GbE1_LINK1000# | | | | O OD | Link Speed Indication LED for 1000Mbps Could be able to sink 24mA or more Carrier LED current |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| S23 | GbE1_MDI2+ | | | | AIO | Qualcomm AR8035 Differential Transmit/Receive Positive Channel 2 |
| S24 | GbE1_MDI2- | | | | AIO | Qualcomm AR8035 Differential Transmit/Receive Negative Channel 2 |
| S25 | GND | | | | P | Ground |
| S26 | GbE1_MDI3+ | | | | AIO | Qualcomm AR8035 Differential Transmit/Receive Positive Channel 3 |
| S27 | GbE1_MDI3- | | | | AIO | Qualcomm AR8035 Differential Transmit/Receive Negative Channel 3 |
| S28 | GbE1_CTREF | | | | O | Qualcomm AR8035 Center tap reference voltage for GBE Carrier board Ethernet magnetic |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| S29 | PCIE_D_TX+ | | | | | Not used |
| S30 | PCIE_D_TX- | | | | | Not used |
| S31 | GBE1_LINK_ACK# | | | | O<br>OD | Link / Activity Indication LED<br>Driven low on Link (10, 100 or 1000 mbps)<br>Blinks on Activity<br>Could be able to sink 24mA or more<br>Carrier LED current |
| S32 | PCIE_D_RX+ | | | | | Not used |
| S33 | PCIE_D_RX- | | | | | Not used |
| S34 | GND | | | | | Ground |
| S35 | USB4+ | | | | | Not used |
| S36 | USB4- | | | | | Not used |
| S37 | USB3_VBUS_DET | | | | | Not used |
| S38 | AUDIO_MCK | E10 | ALT0 | SAI1_MCLK__<br>SAI1_MCLK | O | Master clock output to Audio codecs |
| S39 | I2S0_LRCK | D11 | ALT0 | SAI1_TXFS__<br>SAI1_TXFS | IO | Left& Right audio synchronization clock |
| S40 | I2S0_SDOUT | E11 | ALT0 | SAI1_TXD__<br>SAI1_TXD | O | Digital audio Output |
| S41 | I2S0_SDIN | E12 | ALT0 | SAI1_RXD__<br>SAI1_RXD | I | Digital audio Input |
| S42 | I2S0_CK | C11 | ALT0 | SAI1_TXC__<br>SAI1_TXC | IO | Digital audio clock |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| S43 | ESPI_ALERT0# | | | | | Not used |
| S44 | ESPI_ALERT1# | | | | | Not used |
| S45 | RSVD | | | | | Not used |
| S46 | RSVD | | | | | Not used |
| S47 | GND | | | | G | Ground |
| S48 | I2C_GP_CK | K2 | ALT0 | I2C2_SCL__ I2C2_SCL | IO OD | General purpose I2C bus clock |
| S49 | I2C_GP_DAT | K3 | ALT0 | I2C2_SDA__ I2C2_SDA | IO OD | General purpose I2C bus clock |
| S50 | HDA_SYNC / I2S2_LRCK | | | | | Not used |
| S51 | HDA_SDO / I2S2_SDOUT | | | | | Not used |
| S52 | HDA_SDI / I2S2_SDIN | | | | | Not used |
| S53 | HDA_CK / I2S2_CK | | | | | Not used |
| S54 | SATA_ACT# | | | | | Not used |
| S55 | USB5_EN_OC# | | | | | Not used |
| S56 | ESPI_IO_2 | | | | | Not used |
| S57 | ESPI_IO_3 | | | | | Not used |
| S58 | ESPI_RESET# | | | | | Not used |
| S59 | USB5+ | | | | | Not used |
| S60 | USB5- | | | | | Not used |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| S61 | GND | | | | P | Ground |
| S62 | USB3_SSTX+ | | | | | Not used |
| S63 | USB3_SSTX- | | | | | Not used |
| S64 | GND | | | | | Ground |
| S65 | USB3_SSRX+ | | | | | Not used |
| S66 | USB3_SSRX- | | | | | Not used |
| S67 | GND | | | | P | Ground |
| S68 | USB3+ | | | | | Not used |
| S69 | USB3- | | | | | Not used |
| S70 | GND | | | | P | Ground |
| S71 | USB2_SSTX+ | | | | | Not used |
| S72 | USB2_SSTX-- | | | | | Not used |
| S73 | GND | | | | P | Ground |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| S74 | USB2_SSRX+ | | | | | Not used |
| S75 | USB2_SSRX- | | | | | Not used |
| S76 | PCIE_B_RST# | | | | | Not used |
| S77 | PCIE_C_RST# | | | | | Not used |
| S78 | PCIE_C_RX+ | | | | | Not used |
| S79 | PCIE_C_RX- | | | | | Not used |
| S80 | GND | | | | P | Ground |
| S81 | PCIE_C_TX+ | | | | | Not used |
| S82 | PCIE_C_TX- | | | | | Not used |
| S83 | GND | | | | P | Ground |
| S84 | PCIE_B_REFCK+ | | | | | Not used |
| S85 | PCIE_B_REFCK- | | | | | Not used |
| S86 | GND | | | | P | Ground |
| S87 | PCIE_B_RX+ | | | | | Not used |
| S88 | PCIE_B_RX- | | | | | Not used |
| S89 | GND | | | | P | Ground |
| S90 | PCIE_B_TX+ | | | | | Not used |
| S91 | PCIE_B_TX- | | | | | Not used |
| S92 | GND | | | | P | Ground |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| S93 | DP0_LAN0+ | | | | | Not used |
| S94 | DP0_LAN0- | | | | | Not used |
| S95 | DP0_AUX_SEL | | | | | Not used |
| S96 | DP0_LANE1+ | | | | | Not used |
| S97 | DP0_LANE1- | | | | | Not used |
| S98 | DP0_HDP | | | | | Not used |
| S99 | DP0_LANE2+ | | | | | Not used |
| S100 | DP0_LAN2- | | | | | Not used |
| S101 | GND | | | | P | Ground |
| S102 | DP0_LANE3+ | | | | | Not used |
| S103 | DP0_LANE3- | | | | | Not used |
| S104 | USB3_OTG_ ID | | | | | Not used |
| S105 | DP0_AUX+ | | | | | Not used |
| S106 | DP0_AUX- | | | | | Not used |
| S107 | LCD1_BKLT_ EN | | | | | Not used |
| S108 | LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+ | | | LVDS1_CK+ | O | LVDS1 LCD differential clock pairs |
| S109 | LVDS1_CK- / eDP1_AUX- / DSI1_CLK- | | | LVDS1_CK- | O | LVDS1 LCD differential clock pairs |
| S110 | GND | | | | P | Ground |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| S111 | LVDS1_0+ / eDP1_TX0+ / DSI1_D0+ | | | | AIO | LVDS1 LCD data channel differential pairs 1 |
| S112 | LVDS1_0- / eDP1_TX0- / DSI1_D0- | | | | AIO | LVDS1 LCD data channel differential pairs 1 |
| S113 | eDP1_HPD | | | | | Not used |
| S114 | LVDS1_1+ / eDP1_TX1+ / DSI1_D1+ | | | | AIO | LVDS1 LCD data channel differential pairs 2 |
| S115 | LVDS1_1- / eDP1_TX1- / DSI1_D1- | | | | AIO | LVDS1 LCD data channel differential pairs 2 |
| S116 | LCD1_VDD_EN | | | | | Not used |
| S117 | LVDS1_2+ / eDP1_TX2+ / DSI1_D2+ | | | | AIO | LVDS1 LCD data channel differential pairs 3 |
| S118 | LVDS1_2- / eDP1_TX2- / DSI1_D2- | | | | AIO | LVDS1 LCD data channel differential pairs 3 |
| S119 | GND | | | | P | Ground |
| S120 | LVDS1_3+ / eDP1_TX3+ / DSI1_D3+ | | | | AIO | LVDS1 LCD data channel differential pairs 4 |
| S121 | LVDS1_3- / eDP1_TX3- / DSI1_D3- | | | | AIO | LVDS1 LCD data channel differential pairs 4 |
| S122 | LCD1_BKLT_PWM | | | | | Not used |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| S123 | RSVD | | | | | Not used |
| S124 | GND | | | | P | Ground |
| S125 | LVDS0_0+ / eDP0_TX0+ / DSI0_D0+ | | | | AIO | LVDS0 LCD data channel differential pairs 1 |
| S126 | LVDS0_0- / eDP0_TX0- / DSI0_D0- | | | | AIO | LVDS0 LCD data channel differential pairs 1 |
| S127 | LCD_BKLT_EN | D12 | ALT0 | SAI1_RX_BCLK__ GPIO6_IO17 | O | High enables panel backlight |
| S128 | LVDS0_1+ / eDP0_TX1+ / DSI0_D1+ | | | | AIO | LVDS0 LCD data channel differential pairs 2 |
| S129 | LVDS0_1- / eDP0_TX1- / DSI0_D1- | | | | AIO | LVDS0 LCD data channel differential pairs 2 |
| S130 | GND | | | | P | Ground |
| S131 | LVDS0_2+ / eDP0_TX2+ / DSI0_D2+ | | | | AIO | LVDS0 LCD data channel differential pairs 3 |
| S132 | LVDS0_2- / eDP0_TX2- / DSI0_D2- | | | | AIO | LVDS0 LCD data channel differential pairs 3 |
| S133 | LCD_VDD_EN | C21 | ALT5 | LCD1_RESET__ GOIO3_IO04 | O | High enables panel VDD |
| S134 | LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+ | | | | O | LVDS0 LCD differential clock pairs |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| S135 | LVDS0_CK- / eDP0_AUX- / DSI0_CLK- | | | | O | LVDS0 LCD differential clock pairs |
| S136 | GND | | | | P | Ground |
| S137 | LVDS0_3+ / eDP0_TX3+ / DSI0_D3+ | | | | AIO | LVDS0 LCD data channel differential pairs 4 |
| S138 | LVDS0_3- / eDP0_TX3- / DSI0_D3- | | | | AIO | LVDS0 LCD data channel differential pairs 4 |
| S139 | I2C_LCD_CK | K5 | ALT0 | I2C3_SCL | IO OD | LCD display I2C bus clock |
| S140 | I2C_LCD_DAT | K6 | ALT0 | I2C3_SDA | IO OD | LCD display I2C bus clock |
| S141 | LCD_BKLT_PWM | N3 | ALT1 | GPIO1_IO02__ PWM2_OUT | O | Display backlight PWM control |
| S142 | RSVD | | | | | Not used |
| S143 | GND | | | | P | Ground |
| S144 | eDP0_HPD | | | | | Not used |
| S145 | WDT_TIME_OUT# | E19 | ALT1 | ENET1_CRS__ WDOG2_RST_B_DEB | O | Watchdog-Timer Output |
| S146 | PCIE_WAKE# | K20 | ALT5 | EPDC_PWRSTAT__ GPIO2_IO31 | I | PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup. |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| S147 | VDD_RTC | | | | P | Low current RTC circuit backup power - 3.0V nominal<br>It is sourced from a Carrier based Lithium cell or Super Cap |
| S148 | LID# | C3 | ALT5 | SD2_WP__ GPIO5_IO10 | I | Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state).<br>Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module<br>Pulled up on Module.<br>Driven by OD part on Carrier. |
| S149 | SLEEP# | E4 | ALT5 | SD2_DATA00__ GPIO5_IO14 | I | Sleep indicator from Carrier board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module.<br>Pulled up on Module.<br>Driven by OD part on Carrier. |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| S150 | VIN_PWR_BAD# | | | | I | Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) shall not be enabled while this signal is held low by the Carrier. Pulled up on Module. Driven by OD part on Carrier. |
| S151 | CHARGING# | R1 | ALT0 | GPIO1_IO08__ GPIO1_IO08 | I | Held low by Carrier if DC input for battery charger is present. Pulled up on Module. Driven by OD part on Carrier. |
| S152 | CHARGER_PRSNT# | R2 | ALT0 | GPIO1_IO09__ GPIO1_IO09 | I | |
| S153 | CARRIER_STBY# | C12 | ALT5 | SAI1_RXFS__ GPIO6_IO16 | O | The Module shall drive this signal low when the system is in a standby power state |

| SMARC Edge Finger | | NXP i.MX7 CPU | | | Type | Description |
|---|---|---|---|---|---|---|
| Pin# | Pin Name | Ball | Mode | Signal Name | | |
| S154 | CARRIER_PWR_ON | | | | | Carrier board circuits (apart from power management and power path circuits) should not be powered up until the Module asserts the CARRIER_PWR_ ON signal. |
| S155 | FORCE_RECOV# | | | | I | Pulled up on Module. Driven by OD part on Carrier. |
| S156 | BATLOW# | G3 | ALT5 | SD2_RESET__ GPIO5_IO011 | I | Battery low indication to Module. Carrier to float the line in in-active state. Pulled up on Module. Driven by OD part on Carrier. |
| S157 | TEST# | P6 | | TESTMODE | I | Held low by Carrier to invoke Module SD Boot UP. Pulled up on Module. Driven by OD part on Carrier. |
| S158 | GND | | | | P | Ground |


# Power Control Signals between SMARC Module and Carrier

This Chapter points out the handshaking rule between *SMARC* module and carrier.
Section include：

- *SMARC-FiMX7* Module Power
- Power Signals
- Power Flow and Control Signals Block Diagram
- Power States
- Power Sequences
- Terminations
- Boot Select

# Chapter 4 Power Control Signals between SMARC-FiMX7 Module and Carrier

*SMARC* modules are designed to be driven with a single +3V to +5.25V input power rail. A +5V is recommended for non-battery operated systems. Unlike Q7 module, there is no separate voltage rail for standby power, other than the very low current *RTC* voltage rail. All module operating and standby power comes from the single set of *VDD_IN* pins. This suits battery power sources well, and is also easy to use with non-battery sources.

*SMARC* module has specific handshaking rules to the carrier by *SMARC* hardware specification. To design the carrier board, users need to follow these rules or it might not boot up. Some pull-up and pull-down also need to be cared to make all functions work.

## 4.1 SMARC-FiMX7 Module Power

### 4.1.1. Input Voltage / Main Power Rail

The allowable Module DC input voltage range for *SMARC-FiMX7* is from 3.0V to 5.25V. This voltage is brought in on the *VDD_IN* pins and returned through the numerous *GND* pins on the connector. A single 5V DC input is recommended if device is not operated by battery.

Ten pins are allocated to *VDD_IN*. The connector pin current rating is 0.5A per pin. This works out to 5A total for the 10 pins. At the lowest allowed Module input voltage, this would allow up to 16.75W of electrical power to be brought in (with no de-rating on the connector current capability). With a 40% connector current de-rating, up to 10W may be brought in at 3V.
*SMARC-FiMX7* typically consumes 1.5~4W depending on solo or quad cores and is pretty safe in using the connector.

### 4.1.2. No Separate Standby Voltage

There is no separate voltage rail for standby power, other than the very low

current RTC voltage rail. *SMARC-FiMX7* operating and standby power comes from the single set of *VDD_IN* pins. This suits battery power sources well, and is also easy to use with non-battery sources.

### 4.1.3. RTC/Backup Voltage

RTC backup power is brought in on the *VDD_RTC* rail. The RTC consumption is typically 15 microA or less. The allowable *VDD_RTC* voltage range shall be 2.0V to 3.25V. The *VDD_RTC* rail is sourced from a Carrier based Lithium cell, or it may be left open if the RTC backup functions are not required. *SMARC-FiMX7* module is able to boot without a *VDD_RTC* voltage source.

Lithium cells, if used on Carrier, shall be protected against charging by a Carrier Schottky diode. The diode is placed in series with the positive battery terminal. The diode anode is on the battery side, and the cathode on the Module *VDD_RTC* side.

Note that if a Super cap is used, current may flow out of the Module *VDD_RTC* rail to charge the Super Cap.

### 4.1.4. Power Sequencing

The Module signal *CARRIER_PWR_ON* exists to ensure that the Module is powered before the main body of Carrier circuits (those outside the power and power control path on the Carrier). The main body of Carrier board circuits should not be powered until the Module asserts the *CARRIER_PWR_ON* signal as a high. Module hardware will assert *CARRIER_PWR_ON* when all Module supplies necessary for Module booting are up.

The IO power of carrier board will be turn on at the stage of power on sequence. If the IO power of carrier board been turn on earlier than the *SMARC* module, the power on carrier board might feedback to *SMARC* module through IO lines and disturbs the *SMARC* module power on sequence. More seriously, it might cause to the CPU won't boot up. It is always recommended that the power on module has to be earlier than that on carrier board.

The boot up of module depends on when you release the reset signal of your carrier board. The module will boot up when the reset signal on your carrier board is released. Before that, the module will not boot up. That's

why designer needs to put the *RESET_IN#* in the last stage of power to serve as the "*power good*" signal of the carrier board.

The module will not boot up till the module power is ready because the carrier board hasn't released the reset signal yet.

The sequence is as follows:

Module Power Ready --> *CARRIER_POWER_ON* -->*RESET_IN#* -->Boot Up

### 4.1.5. RESET_IN#

The *SMARC* module does not know the IO power status from the carrier board, and put *RESET_IN#* in the last stage of power can serve as the "*power good*" signal of carrier board. This also assures that the power of carrier board is good when *SMARC* module booting up.

### 4.1.6. VDD_IO

*SMARC* 1.0 specification defines the I/O voltage to be 1.8V or 3.3V or both. The 3.3V *VDD_IO* is depreciated from *SMARC* 1.1 and *SMARC* 2.0 specification.

*SMARC-FiMX7* supports 1.8V *VDD_IO* only.

### 4.1.7. Power Bad Indication (VIN_PWR_BAD#)

Power bad indication is from carrier board and is an input signal for Module. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) will not be enabled while this signal is held low by the Carrier.
This signal has a 100K pull-up on module and is driven by OD part on Carrier.

### 4.1.8. System Power Domains

It is useful to describe an *SMARC* system as being divided into a hierarchy of three power domains:
1) Battery Charger power domain (can be neglected if the system is not

battery powered only)
2) *SMARC* Module power domain
3) Carrier Circuits power domain
The Battery Charger domain includes circuits that are active whenever either charger input power and / or battery power are available. These circuits may include power supply supervisor(s), battery chargers, fuel gauges and, depending on the battery configuration, switching power section(s) to step down a high incoming battery voltage.
The *SMARC* Module domain includes the *SMARC* module.
The Carrier Circuits domain includes “everything else” (and does not include items from the Battery Charger and Module domain, even though they may be mounted on the Carrier).
This is illustrated in the figure below.

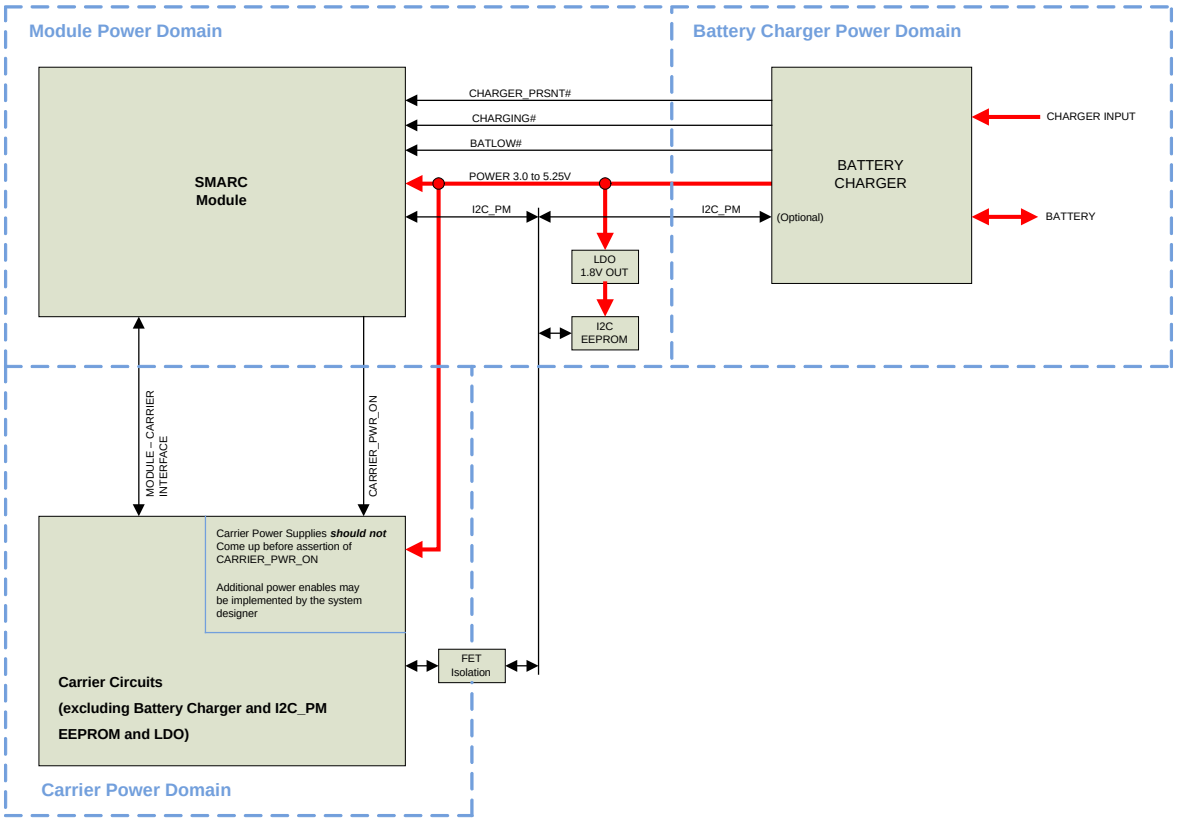



***Figure 24 System Power Domains***

## 4.2 Power Signals

### 4.2.1. Power Supply Signals

| SMARC Edge Finger | | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| Pin# | Pin Name | | | | |
| P147, P148, P149, P150, P151,P152, P153, P154, P155, P156 | VDD_IN | I | PWR | 3.0V~5.25V[1] | Main power supply input for the module |
| P2, S3, P9, S10, P12, S13, P15, S16, P18, S25, P32, S34, P38, S47, P47, P50, P53, P59, S61, S64, S67, P68, S70, S73, P79, S80, P82, S83, P85, S86,P88, S89, P91, S92, P94, P97, P100, S101, P103, S110, S119, P120, S124, S130, P133, S136, P142, S143 | GND | I | PWR | | Common signal and power ground |
| S147 | VDD_RTC | I | PWR | 3.3V | RTC supply, can be left unconnected if internal RTC is not used |

**Note:** 5V is recommended for non-battery operated system.

### 4.2.2. Power Control Signals

The input pins listed in the following table are all active low and are meant to be driven by OD (open drain) devices on the Carrier. The Carrier either floats the line or drives it to *GND*. No Carrier pull-ups are needed. The pull-up functions are performed on the Module. The voltage rail that these lines are pulled to on the Module varies, depending on the design, and may be 3.3V or *VDD_IN*.

| SMARC Edge Finger | | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| Pin# | Pin Name | | | | |
| S150 | VIN_PWR_BAD# | I | CMOS | VDD_IN | Power bad indication from Carrier board |
| S154 | CARRIER_PWR_ON | O | CMOS | 1.8V | Signal to inform Carrier board circuits being powered up |
| P126 | RESET_OUT# | O | CMOS | 1.8V | General purpose reset output to Carrier board. |
| P127 | RESET_IN# | I | CMOS | 1.8V | Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise.<br><br>Pulled up on Module.<br><br>Driven by OD part on Carrier. |
| P128 | POWER_BTN# | I | CMOS | 1.8V | Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. It is de-bounced on the Module<br><br>Pulled up on Module.<br><br>Driven by OD part on Carrier. |

### 4.2.3. Power Management Signals

The pins listed in the following table are related to power management. They will be used in a battery-operated system.

| SMARC Edge Finger | | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| Pin# | Pin Name | | | | |
| S156 | BATLOW# | I | CMOS | 1.8V | Battery low indication to Module. Carrier to float the line in in-active state.<br><br>Pulled up on Module.<br><br>Driven by OD part on Carrier. |
| S154 | CARRIER_PWR_ON | O | CMOS | 1.8V | Signal to inform Carrier board circuits being powered up |
| S153 | CARRIER_STBY# | O | CMOS | 1.8V | Module will drive this signal low when the system is in a standby power state |
| S152 | CHARGER_PRSNT# | I | CMOS | 1.8V | Held low by Carrier if DC input for battery charger is present.<br><br>Pulled up on Module.<br><br>Driven by OD part on Carrier. |
| S151 | CHARGING# | I | Strap | 1.8V | Held low by Carrier during battery charging. Carrier to float the line when charge is complete.<br><br>Pulled up on Module.<br><br>Driven by OD part on Carrier. |

| SMARC Edge Finger | | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| Pin# | Pin Name | | | | |
| S149 | SLEEP# | I | CMOS | 1.8V | Sleep indicator from Carrier board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state.<br><br>Active low, level sensitive. Should be de-bounced on the Module.<br><br>Pulled up on Module.<br><br>Driven by OD part on Carrier. |
| S148 | LID# | I | CMOS | 1.8V | Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module<br><br>Pulled up on Module.<br><br>Driven by OD part on Carrier. |

### 4.2.4. Special Control Signals (TEST#)

*SMARC-FiMX7* module boots up from an onboard *NOR* Flash first. The firmware in the *SPI NOR* flash will read the *BOOT_SEL* configuration and decides where to load the u-boot.
In some situations like the firmware in *NOR* flash needed to be upgrade or at factory default where the firmware in *NOR* flash is empty or at development stage that the firmware in NOR needs to be modified, users will need an alternative way to boot up from SD card first. The *TEST#* pin serves as this purpose. The *TEST#* pin is pulled high on module. If carrier board leaves this pin floating or pulls high, the module will boot up from *SPI NOR*. If carrier board pulls this pin to *GND*, the module will boot up from *SD* card. The first stage bootloader in *i.MX7* CPU ROM codes will load the 2nd stage bootloader based on the setting of this *#TEST* pin (*S157*).

## 4.3 Power Flow and Control Signals Block Diagram

Following figures shows the power flow and control signals block diagram.

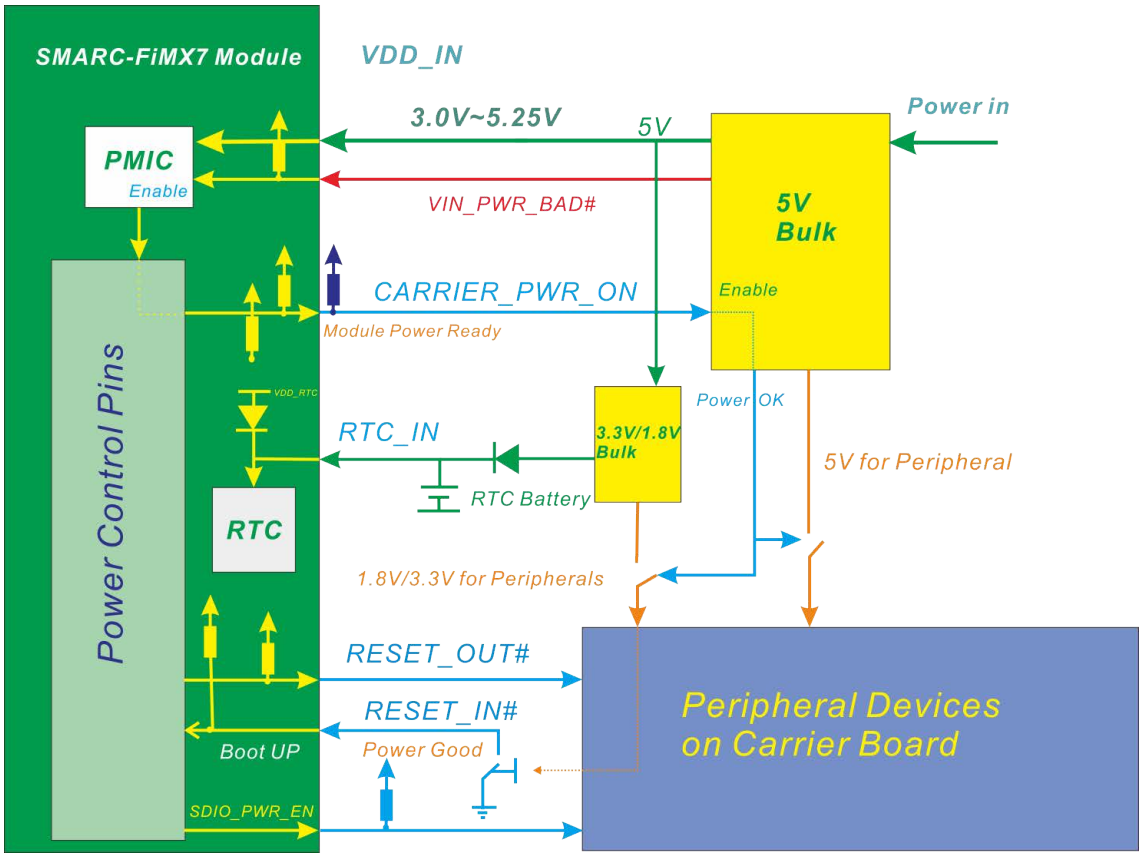



*Figure 25: Power Block Diagram*

When main power is supplied from the carrier, a voltage detector will assert *VIN_PWR_BAD#* signal to tell the module and carrier that the power is good. This signal will turn on the PMIC on module to power on the module.

Carrier power circuits in the carrier Power domain should not power up unless the module asserts *CARRIER_PWR_ON*. The module signal *CARRIER_PWR_ON* exists to ensure that the module is powered before the main body of carrier circuits (those outside the power and power control path on the carrier).

The main body of carrier board circuits will not be powered until the module asserts the *CARRIER_PWR_ON* signal being correct. Module hardware will assert *CARRIER_PWR_ON* when all power supplies necessary for module booting are ready. The module will continue to assert signal *RESET_OUT#* after the release of *CARRIER_PWR_ON*, for a period sufficient to allow carrier power circuits to come up. When Carrier power is ready, it will assert *RESET_IN#* to inform module booting up.

If users would like to have SD boot up, *SDIO_PWR_EN* signal have to be pull up to 3.3V on carrier.

Module and carrier power supplies will not be enabled if the *VIN_PWR_BAD#* is held low by carrier. It is a power bad indication signal from carrier and is 100k pull up to *VDD_IN* on module.

## 4.4 Power States

The *SMARC-FiMX7* module supports different power states. The table below describes the behavior in the different states and which power rails and peripherals are active. Additional power states can be implemented if required using available GPIOs to control additional power domains and peripherals.

| Abbr. | Name | Description | Module | Carrier Board |
|---|---|---|---|---|
| UPG | Unplugged | No power is applied to the system, except the RTC battery might be available | No main VDD_IN applied from fixed DC supply, VDD_IN available if backup battery is implemented | No power supply input, RTC battery maybe inserted |
| OFF | off | System is off, but the carrier board input supply is available | The main VDD_IN is available, but the CPU and peripherals are not running. Only the PMIC is running | Carrier board provides power for module, the peripheral supplies are not available |
| SUS | Suspend | System is suspended and waits for wakeup sources to trigger | CPU is suspended, wakeup capable peripherals are running while others might be switched off | Power rails are available on carrier board, peripherals might be stopped by software |
| RUN | Running | System is running | All power rails are available, CPU and peripherals are running | All power rails are available, peripherals are running |
| RST | Reset | System is put in reset state by holding RESET_IN# is low | All power rails are available, CPU and peripherals are in reset state | All power rails are available, peripherals are in reset state |

The figure below shows a sequence diagram for the different power states. The module automatically enters into the running mode when the main power rail is applied to the module. In the running mode, the system can be set to suspend by software. There might be different wake up sources available. Consult the datasheet for *SMARC-FiMX7* module for more information about the available wakeup events.

In the running state, a shutdown request can be triggered by software. This turns off all power rails on the module and requests the carrier board to switch of the power rails for the peripherals. The module can be brought back to the

running mode in two ways. The module main voltage rail (*VDD_IN*) can be removed and applied again. If needed, this could also be done with a button and a small circuit. *SMARC-FiMX7* module supports being power cycled by asserting the *RESET_IN#* signal (e.g. by pressing the reset button or shunt and relief the reset jumper), please consult the associated module datasheet for more information about the support power cycle methods.

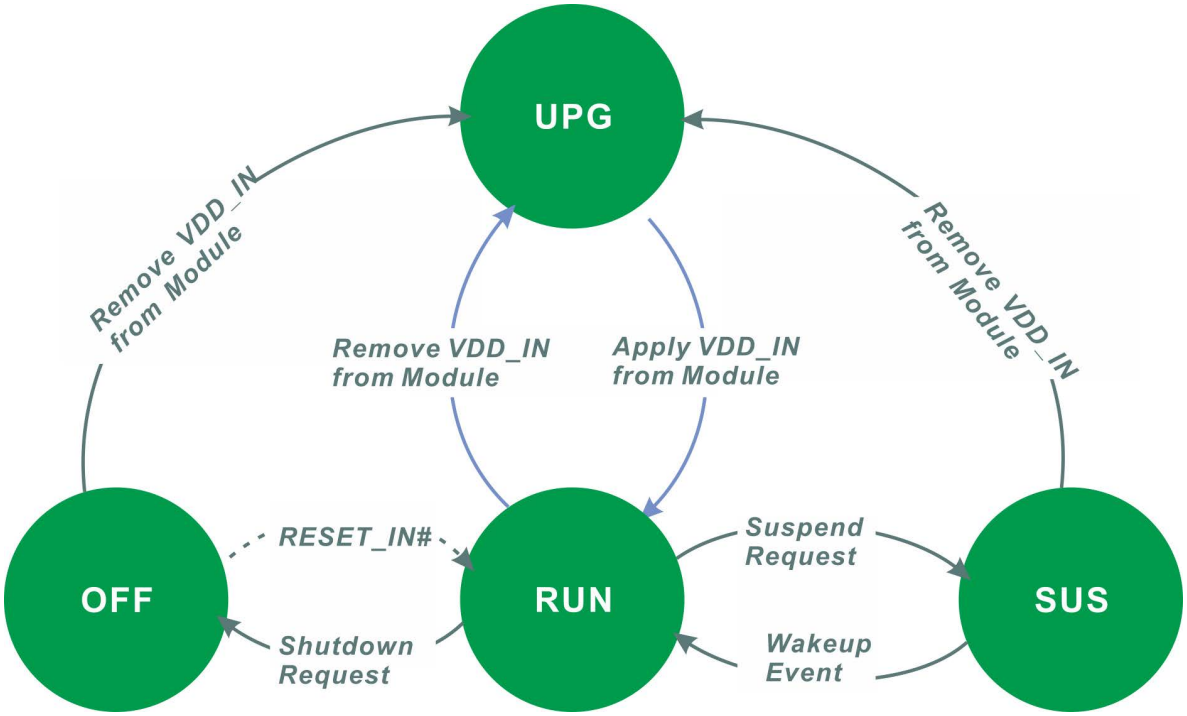



*Figure 26: Power States and Transitions*

## 4.5 Power Sequences

When main power is supplied from the carrier, a voltage detector will assert *VIN_PWR_BAD#* signal to tell the module and carrier that the power is good. This signal will enable the PMIC on module to power on the module. The module will not power up if the module receives a low-active *VIN_PWR_BAD#* signal.

The *SMARC-FiMX7* module starts asserting *CARRIER_PWR_ON* as soon as the main voltage supply is applied to the module and all module supplies necessary for module booting are up. This is to ensure that the module is powered before the main body of carrier circuits (those outside the power and power control path on the carrier). The module will continue to assert signal

*RESET_OUT#* after the release of *CARRIER_PWR_ON*, for a period sufficient time (at least 10ms) to allow carrier power circuits that the peripheral supplies need to ramp up.

The peripheral power rails on the carrier board need to ramp up in a correct sequence. The sequence starts normally with the highest voltage (e.g. 5V) followed by the lower voltages (e.g. 3.3V then 1.8V and so on). Peripherals normally require that a lower voltage rails is never present if a higher rail is missing. Check the datasheet of all peripheral components on the carrier board for a proper sequencing. The *SMARC-FiMX7* modules guarantees to apply the reset output *RESET_OUT#* not earlier than 100ms after the *CARRIER_PWR_ON* goes high. This gives the carrier board a sufficient time for ramping up all power rails. *SDIO_PWR_EN* signal have to be pull up to 3.3V on carrier if users would like to have SD boot up functionality.

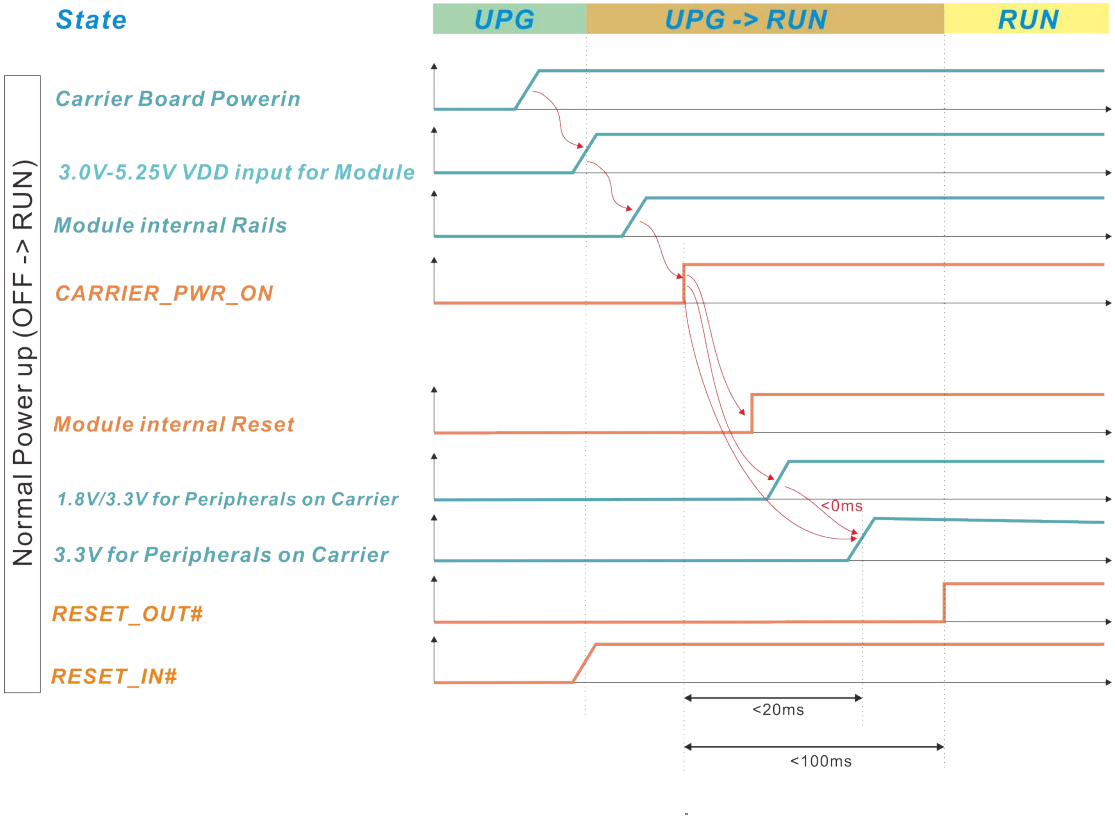



**Figure 27: Power-Up Sequence**

If the operating system supports it, a shutdown sequence can be initiated. Some systems may benefit from shutting down instead of just removing the main power supply as this allows the operating system to take care of any housekeeping (e.g. bringing mass storage devices to a controlled halt). Some operating system may not provide the shutdown function.

As it is not permitted that a lower voltage rail is present when a higher voltage rail has been switched off, the sequence of shutting down the peripheral voltages needs to be considered. The lower voltages (e.g. peripheral 3.3V) need to ramp down before the higher ones do (e.g. peripheral 5V).

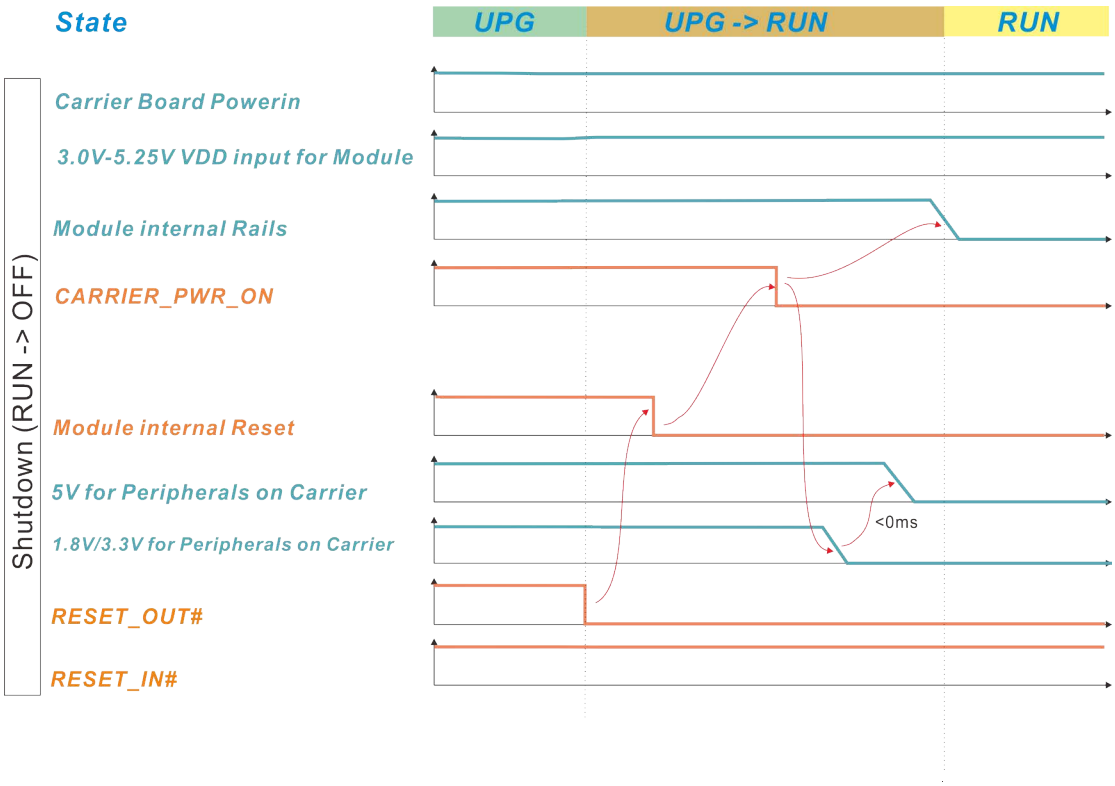



*Figure 28: Shutdown Sequence*

When the *RESET_IN#* is asserted, a reset cycle is initiated. The module internal reset and the external reset output *RESET_OUT#* are asserted as long as *RESET_IN#* is asserted. If the reset input *RESET_IN#* is de-asserted, the internal reset and the *RESET_OUT#* will remain low for at least 1ms until they are also de-asserted and the module starts booting again. This guarantees a minimum reset time of 1ms even if the reset input *RESET_IN#* is triggered for a short time.

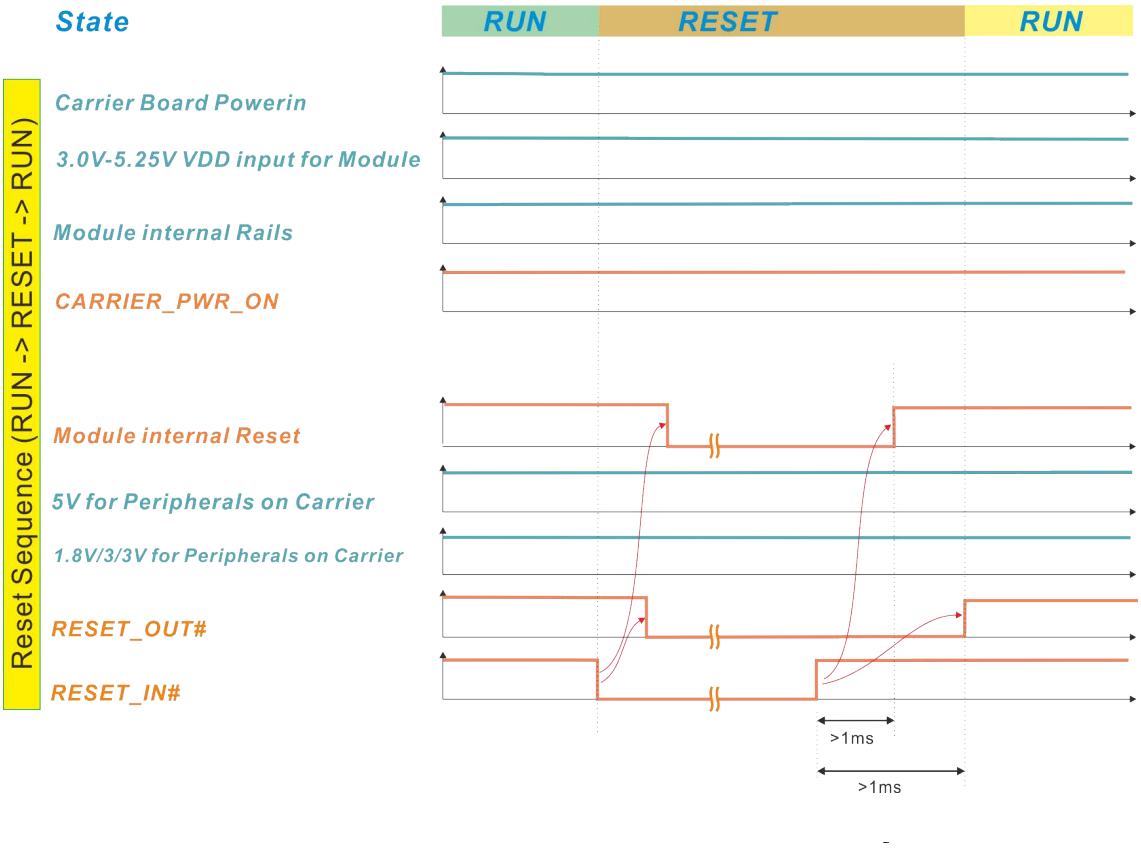



*Figure 29: Reset Sequence*

## 4.6 Terminations

### 4.6.1. Module Terminations

The Module signals listed below will be terminated on the Module. The terminations follow the guidance given in the table below.

| Signal Name | Series Termination | Parallel Termination | Notes |
|---|---|---|---|
| I2C_PM_DAT | | 2.2K pull-up to 1.8V | |
| I2C_PM_CK | | 2.2K pull-up to 1.8V | |
| I2C_LCD_DAT | | 2.2K pull-up to 1.8V | |
| I2C_LCD_CK | | 2.2K pull-up to 1.8V | |
| I2C_GP_DAT | | 2.2K pull-up to 1.8V | |
| I2C_GP_CK | | 2.2K pull-up to 1.8V | |
| I2C_CAM_DAT | | 2.2K pull-up to 1.8V | |
| I2C_CAM_CK | | 2.2K pull-up to 1.8V | |
| | | | |
| PCIE_A_TX+ | 0.1 uF 0402 capacitor | | |
| PCIE_A_TX- | 0.1 uF 0402 capacitor | | |
| | | | |
| SDIO_CD# | | 10k pull-up to 3.3V | |
| SDIO_WP | | 10k pull-up to 3.3V | |
| | | | |
| VIN_PWR_BAD# | | 200k pull-up to VIN | |
| | | | |

| Signal Name | Series Termination | Parallel Termination | Notes |
|---|---|---|---|
| USB[0:1]_EN_OC# | | 10K pull-up to 3.3V or a switched 3.3V on the Module | Switched 3.3V: if a USB channel is not used, then the USBx_EN_OC# pull-up rail may be held at GND to prevent leakage currents. |
| | | | |

### 4.6.2. Carrier/Off-Module Terminations

The following Carrier terminations are required, if the relevant interface is used. If unused, the *SMARC* Module pins may be left un-connected.

| Module Signal Group Name | Carrier Series Termination | Carrier Parallel Termination | Notes |
|---|---|---|---|
| **GBE[0:1]_MDI[0:3]** | *Magnetics module appropriate for 10/100/1000 GBE transceivers* | *Secondary side center tap terminations appropriate for Gigabit Ethernet implementations* | |
| **GBE[0:1]_LINK**<br><br>**(GBE status LED sinks)** | | *If used, current limiting resistors and diodes to pulled to a positive supply rail* | *The open drain GBE status signals, GBE_LINK100#, GBE_LINK1000# and GBE_LINK_ACT#, if used, need Carrier based current limiting resistors and LEDs. The LED may be integrated into a Carrier RJ45 jack. A resistor of 68 ohms, and a LED with the anode tied to Carrier 3.3V, is typical.* |
| **LVDS LCD** | | *100 ohm resistive termination across the differential pairs at the endpoint of the signal path, usually on the display assembly* | |
| **PCIE_A_RX** | *Series coupling caps near the TX pins of the Carrier board PCIe device* | | |

## 4.7 Boot Device Selection

*SMARC* hardware specification defines three pins (*BOOT_SEL[0:2]*) that allow the Carrier board user to select from eight possible boot devices. The first stage of bootloader on *SMARC-FiMX7* will boot up to *SPI NOR* flash first. The firmware on *NOR* flash will read the boot device configuration and load the second stage bootloader from selected boot devices. The *BOOT_SELx#* pins are weakly pulled up on the Module and the pin states decoded by module logic. The Carrier shall either leave the Module pin Not Connected ("Float" in the table below) or shall pull the pin to *GND*, per the table below.

| | Carrier Connection | | | Boot Source |
|---|---|---|---|---|
| | BOOT_SEL2# | BOOT_SEL1# | BOOT_SEL0# | |
| 0 | GND | GND | GND | Carrier SATA |
| 1 | GND | GND | Float | Carrier SD Card |
| 2 | GND | Float | GND | Carrier eMMC Flash |
| 3 | GND | Float | Float | Carrier SPI |
| 4 | Float | GND | GND | Module Device(USB) |
| 5 | Float | GND | Float | Remote Boot (GBE) |
| 6 | Float | Float | GND | Module eMMC Flash |
| 7 | Float | Float | Float | Module SPI |