

# LAN8720A RMII PHY Customer Evaluation Board

Assy 6584

PCB Revision C

Schematic Revision 1.3

## Design Details

Board:

Assy 6584

Chip:

SMSC LAN8720A

Board Form Factor:

MII Add-On Card

Assembly:

24 Lead QFN w/ Exposed GND Pad

Circuit Diagrams utilizing SMSC Products Are Included As A Means Of Illustrating Typical Semiconductor Applications: Consequently Complete Information Sufficient For Construction Purposes Is Not Necessarily Given. The Information Has Been Carefully Checked And Is Believed To Be Entirely Reliable. However, No Responsibility Is Assumed For Inaccuracies. Furthermore, Such Information Does Not Convey To The Purchaser Of The Semiconductor Devices Described Any License Under The Patent Rights Of SMSC Or Others. SMSC Reserves The Right To Make Changes At Any Time In Order To Improve Design And Supply The Best Product Possible.

### Revision History

#### Rev 1.0:

Initial release, Rev C

#### Rev 1.1:

U3 (page 2) - Changed from 74LVC1G07 to 74LVC1G17 in rework prior to release of all Revision C boards.

"Configuration Resistor Settings" (Pg. 03): Created new table.

Configuration Resistor Settings" table, (Pg. 03): Correction to signal name within table from "nINT/TXEN/TXD4" to "nINT/REFCLKO Signal".

Added text to signal "nINT" pull-up jumper.

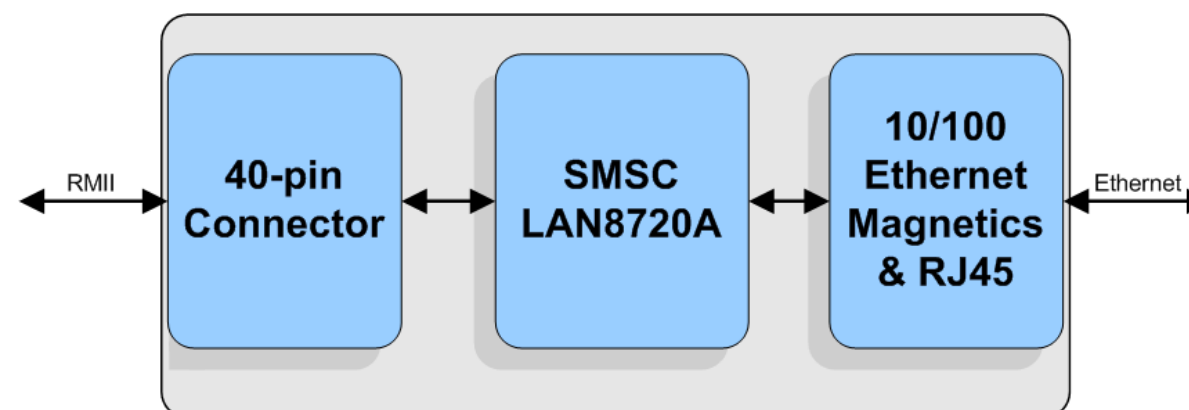
#### Rev 1.2:

All Pages - Changed from LAN8720 to LAN8720A

#### Rev 1.3:

C19 changed from 0.1uF to 470pF.

### BLOCK DIAGRAM

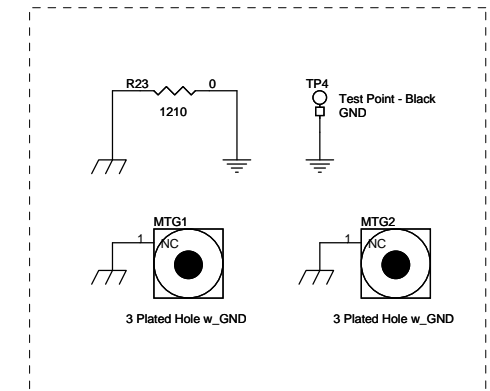
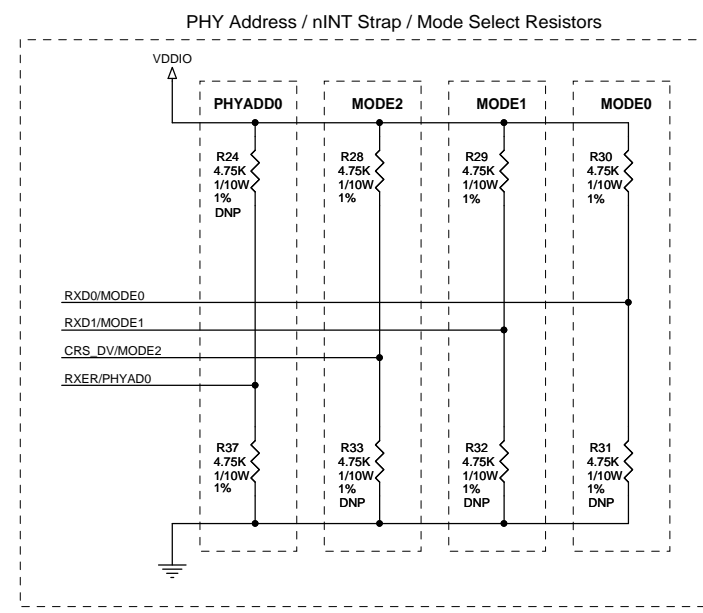
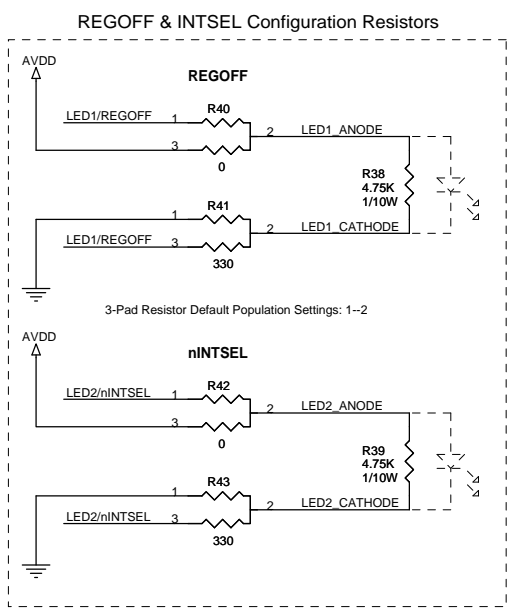
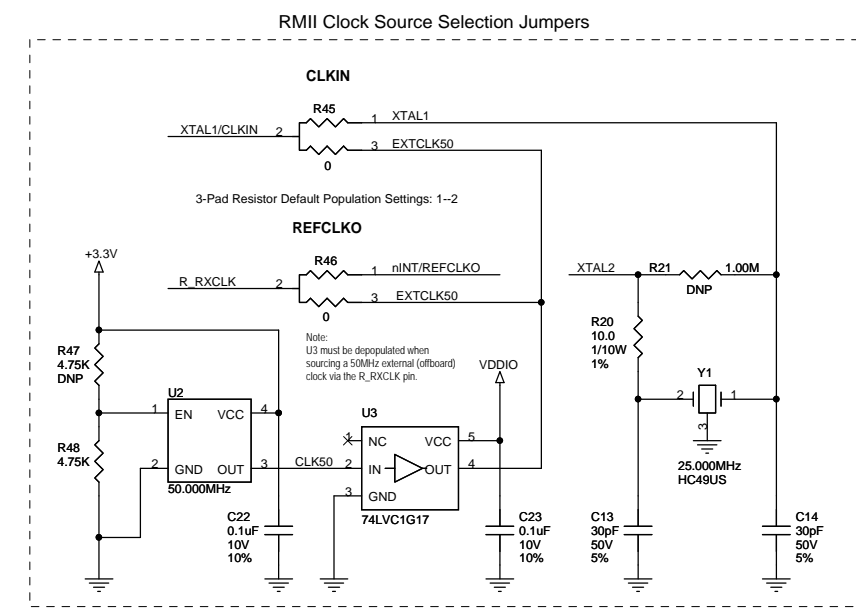
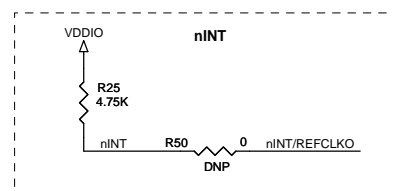
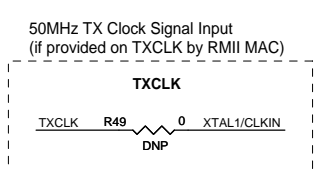
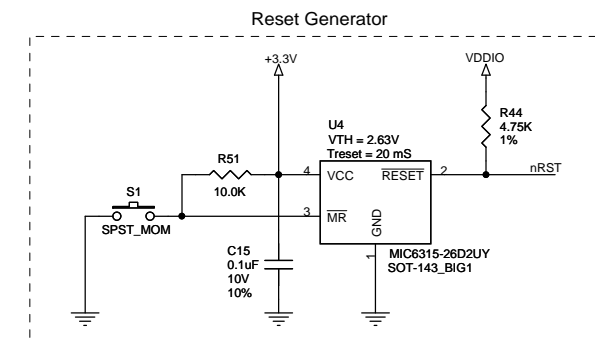
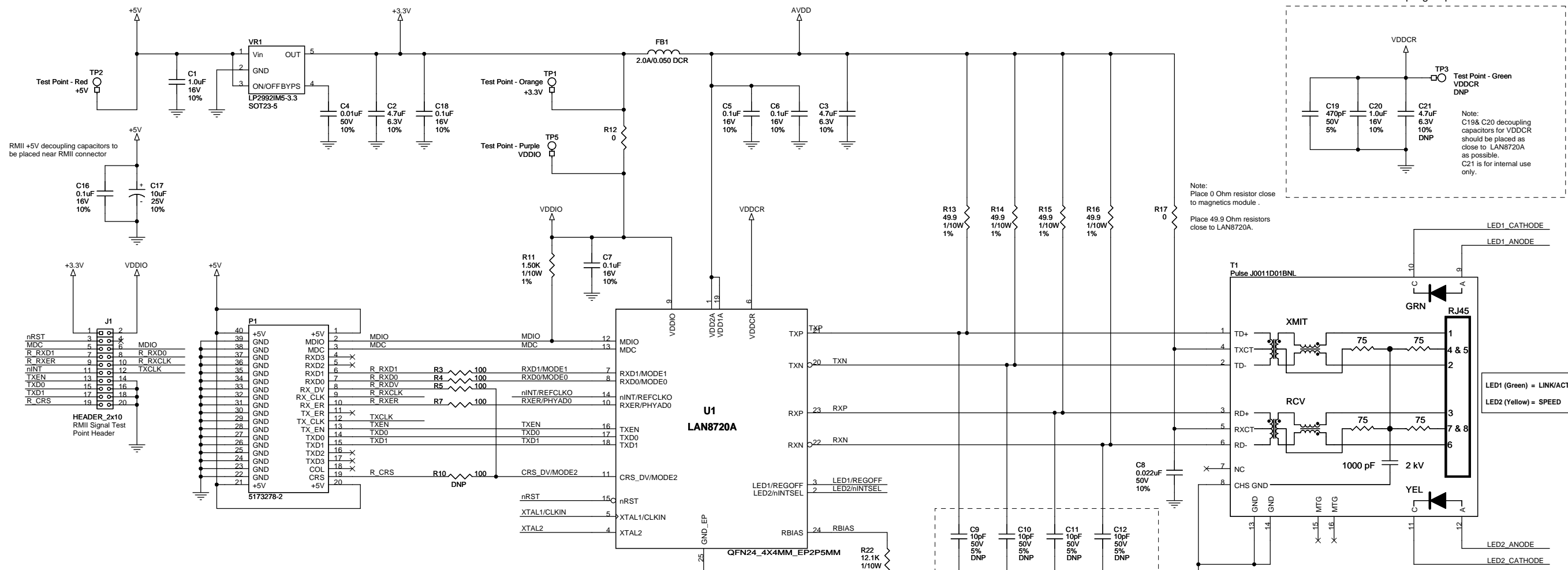


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Title				
LAN8720A RMII PHY Customer Evaluation Board				
Size	Engineer	Assembly No.	PCB Rev	Schematic Rev
	R. W.	6584	C	1.3
Date:	Tuesday, May 18, 2010		Sheet	1 of 3

# LAN8720A / Magnetics / RMII Connector



**SMSC**  
SUCCESS BY DESIGN

Title: LAN8720A / Magnetics / (R)MII Connector

Size	Engineer	Assembly No.	PCB Rev	Schematic Rev
	R. W.	6584	C	1.3

Date: Thursday, January 06, 2011 Sheet 2 of 3

# Configuration Settings

## Configuration Settings

SIGNAL	POPULATE	DEPOPULATE	Default	COMMENTS
PHYAD[0] = 0	R37	R24	Default	
PHYAD[0] = 1	R24	R37		
MODE[0] = 0 MODE[1] = 0 MODE[2] = 0	R31 R32 R33	R30 R29 R28		
MODE[0] = 1 MODE[1] = 1 MODE[2] = 1	R30 R29 R28	R31 R32 R33	Default Default Default	
Internal 1.2V Reg. Enabled Internal 1.2V Reg. Disabled	R40 & R41: 1-2 R40 & R41: 2-3	R40 & R41: 2-3 R40 & R41: 1-2	Default	
Interrupt Function Enabled on nINT/TXER/TXD4 Signal Interrupt Function Disabled on nINT/TXER/TXD4 Signal	R50, R42 & R43: 2-3  R42 & R43: 1-2	R42 & R43: 1-2  R50, R42 & R43: 2-3	Default	
25.000MHz Crystal Clock Source Enabled	R20, R48, R45 & R46: 1-2	R47, R49 R45 & R46: 2-3	Default	Interrupt Function must be disabled in this configuration.
25MHz Crystal Clock Source Disabled, with Offboard 50MHz Clock Source Provided on TXCLK	R48, R49	R20, R47, R45 & R46: 1-2 R45 & R46: 2-3		Interrupt Function must be enabled in this configuration.
25MHz Crystal Clock Source Disabled, with Offboard 50MHz Clock Source Provided on RXCLK	R48, R45 & R46: 2-3	U3, R20, R47, R49 R45 & R46: 1-2		Interrupt Function must be enabled in this configuration.
25MHz Crystal Clock Source Disabled, with Onboard 50MHz Clock Source Provided on RXCLK	U3, R47, R45 & R46: 2-3	R20, R48, R49 R45 & R46: 1-2		Interrupt Function must be enabled in this configuration.
25MHz Crystal Clock Source Disabled, with Onboard 50MHz Clock Source Provided on RXCLK via REFCLK0	U3, R47, R45: 2-3 R46: 1-2	R20, R48, R49 R45: 1-2 R46: 2-3		Interrupt Function must be disabled in this configuration.