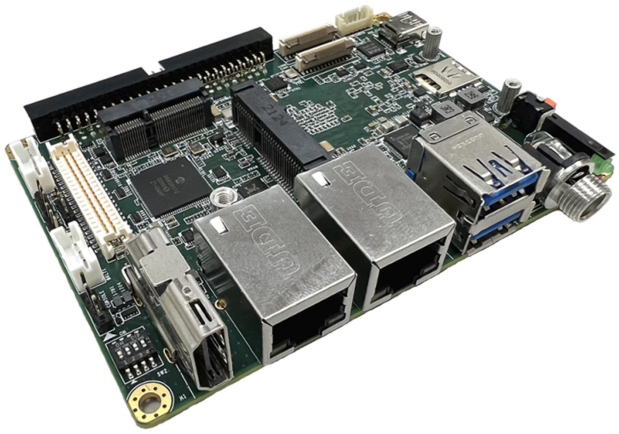
USER GUIDE



pITX-MX8M-PLUS

User Guide Rev. 1.0

Doc ID: 1822-7820

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pITX-MX8M-PLUS USER GUIDE

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⚠ CAUTION	Handling and operation of the product is permitted only for trained personnel within a work place that is access controlled. Please follow the “General Safety Instructions” supplied with the system.
NOTICE	You find the most recent version of the “General Safety Instructions“ online in the download area of this product.

Revision History

Revision	Brief Description of Changes	Date of Issue	Author
1.0	Initial Issue	2022-July-01	ykl

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Symbols

The following symbols may be used in this manual

DANGER

DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.

WARNING

WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.

NOTICE

NOTICE indicates a property damage message.

CAUTION

CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.

Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

ESD Sensitive Device!

This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.

HOT Surface!

Do NOT touch! Allow to cool before servicing.

This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.

For Your Safety

Your new Embedian product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Embedian product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠ CAUTION

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

⚠ CAUTION

Electric Shock!

Before installing a non hot-swappable Embedian product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

⚠ CAUTION

Danger of explosion if the battery is replaced incorrectly.

- Replace only with same or equivalent battery type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer's instructions.

General Instructions on Usage

In order to maintain Embedian's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Embedian and described in this user guide or received from Embedian Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Quality and Environmental Management

Embedian aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements.

Disposal and Recycling

Embedian's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

Environmental protection is a high priority with Embedian.

Embedian follows the WEEE directive

You are encouraged to return our products for proper disposal.

Packing List

Your product package should include the items listed below.

If any of the items below is missing, contact the seller from whom you have purchased the product.

Packing List
1 x pITX-MX8M-Plus SBC

NOTICE

All most update user's manual and software source codes can be downloaded from Embedian's website. No printed or digital CD will be included.

Ordering Information

Part Number	Description
pITX-MX8M-Plus-2G	Pico-ITX SBC with NXP i.MX8M Plus Quad Core, 2 GByte LPDDR4, 0~60° C
pITX-MX8M-Plus-2G-I	Pico-ITX SBC with NXP i.MX8M Plus Quad Core, 2 GByte LPDDR4, -40°C~85° C
pITX-MX8M-Plus-4G	Pico-ITX SBC with NXP i.MX8M Plus Quad Core, 4 GByte LPDDR4, 0~60° C
pITX-MX8M-Plus-4G-I	Pico-ITX SBC with NXP i.MX8M Plus Quad Core, 4 GByte LPDDR4, -40°C~85° C

Optional Accessories

Part Number	Description
125021500AUD-00	Audio HP Out, Mic In and Line In Cable
VTT-HS-9A981-A1	Heat Sink for pITX-MX8M-PLUS
125040700LCD-00	7-inch LVDS Display G070VW01 V0
125023000LVD-00	LVDS Cable for 7-inch G070VW01 V0
125022000BKT-00	LVDS Backlight Cable for 7-inch G070VW01 V0
12605M200ABG-00	M.2 WiFi Module (IEEE 802.11a/b/g/n/ac Wireless LAN 2T2R and Bluetooth 5.3 Combo Module with 88W8997 chipset)
pITX-IOB-2201	50-pin IO Extension Board with 2 x CAN, 4 x RS232, 1 x RS484 (Terminal Blocks), 1 x USB 2.0 Type-A, 1 x USB 2.0+3.0 Type-A, SPI, I2C
126010101245-00	Dipole Ant. D.B 2.4/5G WIFI 3dBi SMA/M BLK
12506100003HF4-00	Antenna Cable SMA (F) to MHF4 (F), 100mm

Table of Contents

General Information

The information provided in this chapter includes:

- Introduction
- Features and Functionality
- Product View
- Product Variants
- Block Diagram
- Mechanical Drawing
- Software Installation and Support

Chapter 1 General Information

1.1 Introduction

This manual describes the pico-ITX board from NXP i.MX8M Plus processor, which is the first Cortex®-A53 based SoC integrated with NPU (Neural Processing Unit). This board will also be denoted pITX-MX8M-Plus within this Users Guide.

pITX-MX8M-Plus is capable of providing outstanding Edge AI inference at 2.3 TOPS to perform well on Object Detection as well as Image Segmentation. The use of this Users Guide implies a basic knowledge of PC hardware. This manual is focused on describing the pITX-MX8M-Plus board's special features and is not intended to be a standard PC textbook.

New users are recommended to study the short installation procedure stated in the last chapter before switching-on the power. Latest revision of this manual, datasheet, BSPs (Board Support Packages) can be downloaded from Embedian Web Page. All IO mappings to i.MX8M Plus that are especially usefully for software engineers are also described in this manual.

Upon the standard I/Os on the coastline, pITX-MX8M-Plus also offers the possibility of I/O Extension on the rear side by a 50-pin 2.00mm box header (EIO50) to provide flexible I/Os like more USB, I2C, RS232/285, SPI and CAN for your specific vertical requirements. Users can download the reference design of EIO50 expansion board from Embedian's website.

1.2 Features and Functionality

The board is based on the NXP´s quad core ARM Cortex-A53 i.MX8M Plus processor. It is mechanically compliant to the Pico-ITX (pITX) specification. Board key features are:

- Form Factor: pico-ITX and passive cooling solution
- Processor: NXP i.MX8M Plus Quad ARM Core Cortex-A53 (Up to 1.8GHz)
- Memory:
    - Capacity and Technology: 2GB or 4GB LPDDR4 4000MT/s (6GB optional)
    - Flash: 16GB eMMC
    - EEPROM: 4M (to store board part number, revision number, serial number and MAC address)
- NPU: 2.3 TOPS Neural Network performance
- Display:
    - HDMI: 1 x HDMI 2.0a, up to 3840 x 2160 at 30Hz
    - LVDS: 1 x Single Channel or 1 x Dual Channel 24 bit Bit LVDS, Backlight Power 5V or 12V, Max. 1.5A
    - MIPI-DSI: 1 4-Lane MIPI-DSI (shared with second channel LVDS interface)
- Graphic Engine
    - GC7000UL with 2D/3D Graphic Acceleration supporting 1G Pixel/s
    - OpenVG 1.1, OpenGL ES3.1, Vulkan, and OpenCL 1.2 FP
- H/W Video Codec:
    - Decoder: 1080p60 HEVC/H.265 Main, VP9 Profile 0/2, VP8, AVC/H.264 Baseline/Main/High
    - Encoder: 1080p60 AVC/H.264, HEVC/H.265
- 2 x Ethernet (RJ-45):
    - Chipset: NXP i.MX8M Plus integrated RGMII
    - One supports QoS with TSN
    - Speed: 10/100/1000 Mbps
    - PHY: Realtek RTL8211FD(I)-CG
- Watchdog Timer:
    - Chipset: TI TPS3828-33DBVR
    - 200ms timeout timer

(Continued)

- TPM: TPM2.0 (ST33HTPH2X32AHE1)
- Audio:
  - Audio Codec WM8960
  - Headphone Out
  - Microphone In
- RTC: RTC Backup Battery by 2-pin type connector
- Reset: 1 Reset Button
- IO:
  - USB: 2 x USB 3.1 Gen 1 Host (Type A), 1x USB client (Mini Type B)
  - UART: 1 x UART as debug console by pin header
  - Camera Input: 2 x 4-Lane MIPI-CSI2
- Rear IO:
  - EIO50 50-pin 2.00mm Box Header
    - 1 x USB 3.1 Host, 3 x USB 2.0 Host, 2 x CAN-FD, 1 x SPI, 2 x I2C, 4 x UARTs and 6 x GPIOs
- LED:
  - 1 x Green Power LED
  - 1 x Yellow Programmable LED
- Expansion:
  - 1 Mini-PCIe: 1 x Full Size Mini-PCIe Slot (USB 3.1 and USB 2.0 Signals only)
  - 1 M.2 2230 Key E Slot (USB 2.0/I2C/UART/PCIe/UART/SDIO/I2S)
  - EIO50 50-pin 2.00mm Box Header (4 x UARTs, 1 x USB 3.1, 2 x USB 2.0, 2 x I2C, 1 x SPI, 6 GPIOs, 2 x CAN-FD)
  - SD Socket: 1 x Micro SD Socket
  - SIM Slot: 1 x Nano SIM Slot
- Power:
  - Power Supply Voltage: 12V DC-IN by lockable DC Jack (or 2-pin type connector by BOM option)
  - Power Consumption: 7.21 W

(Continued)

- Environment:
  - Operational Temperature: 0^0 ~ 60^0 C (Commercial) / -40^0 ~ 85^0 C (Industrial)
  - Operating Humidity: 5% ~ 95% Relatively Humidity, non-condensing
- Mechanical:
  - Dimensions: 100 x 72 x 19 mm
  - Weight: 0.05Kg (0.25Kg with Heat Sink)
- Operating System: Yocto, Debian and Android
- Certifications: CE/ FCC Class B

1.3 Product View

Figure 1: pITX-MX8M-Plus Product View (Top View)

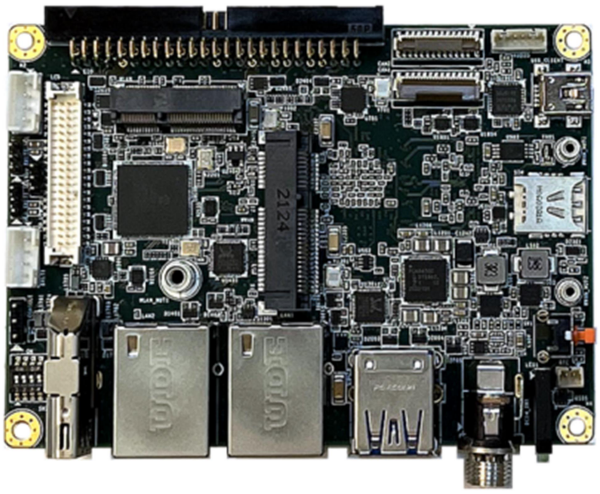


Figure 2: pITX-MX8M-Plus Product View (Front View)

Figure 3: pITX-MX8M-Plus Product View (Rear View)

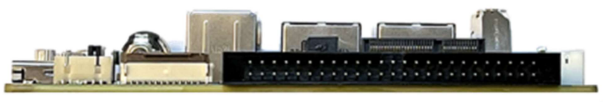
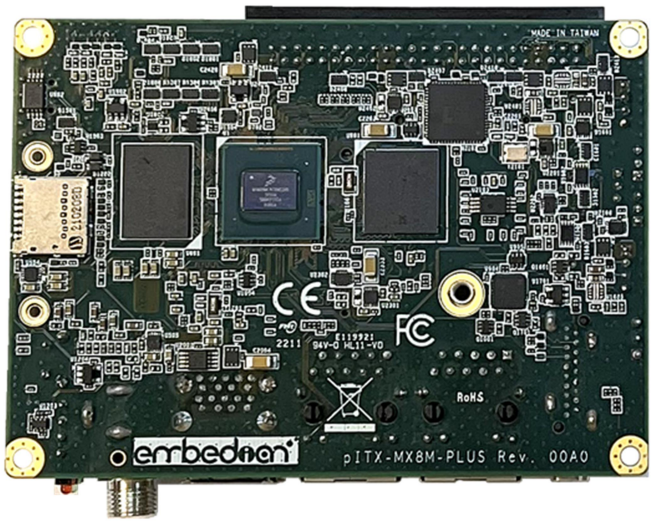


Figure 4: pITX-MX8M-Plus Product View (Bottom View)



1.4 Product Variants

Embedian offers the pITX-MX8M-Plus in five different configurations.

Part Number	Description
pITX-MX8M-Plus-2G	Pico-ITX SBC with NXP i.MX8M Plus Quad Core Cortex®-A53 1.8 GHz with NPU, GPU, and VPU, commercial temperature range, 2 GByte LPDDR4, 16 GByte eMMC
pITX-MX8M-Plus-2G-I	Pico-ITX SBC with NXP i.MX8M Plus Quad Core Cortex®-A53 1.6 GHz with NPU, GPU, and VPU, industrial temperature range, 2 GByte LPDDR4, 16 GByte eMMC
pITX-MX8M-Plus-4G	Pico-ITX SBC with NXP i.MX8M Plus Quad Core Cortex®-A53 1.8 GHz with NPU, GPU, and VPU, commercial temperature range, 4 GByte LPDDR4, 16 GByte eMMC
pITX-MX8M-Plus-4G-I	Pico-ITX SBC with NXP i.MX8M Plus Quad Core Cortex®-A53 1.6 GHz with NPU, GPU, and VPU, industrial temperature range, 4 GByte LPDDR4, 16 GByte eMMC

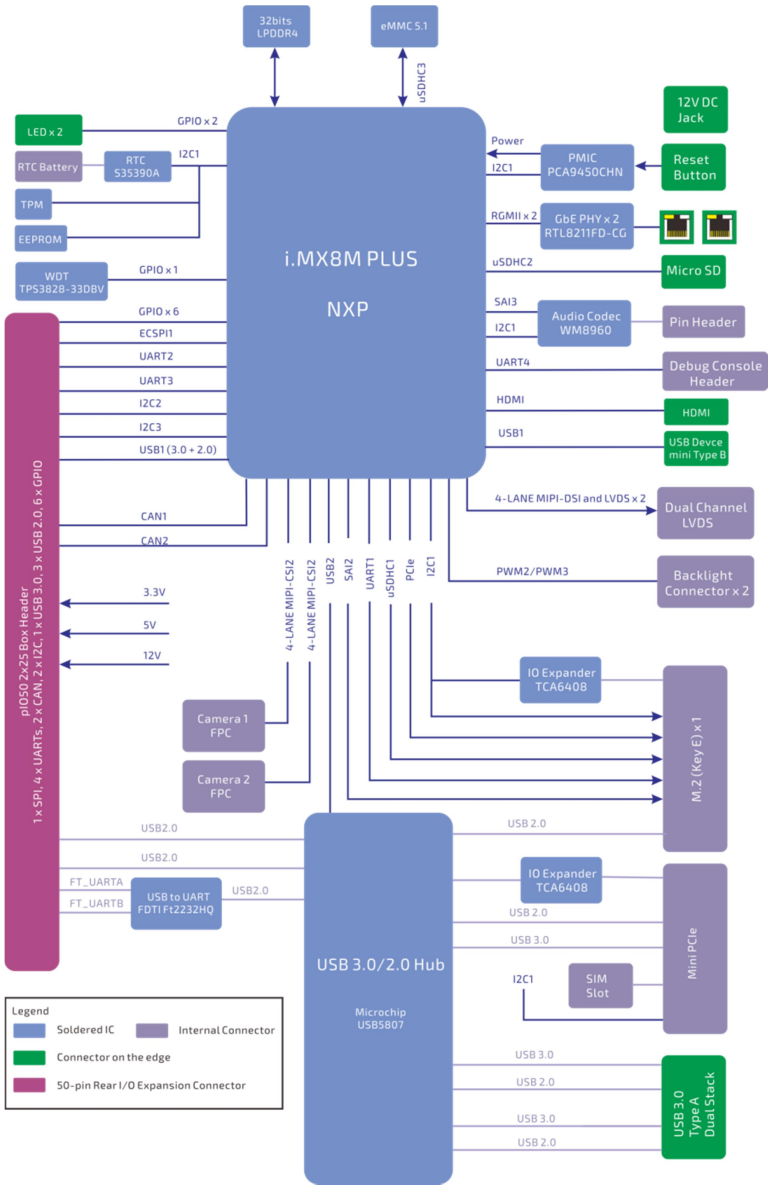
WARNING Please do not operate the pITX-IMX8M without sufficient cooling system.

Please contact Embedian sales person if you need other memory and flash configurations.

1.5 Block Diagram

Overall system block diagram is shown as figure 5.

Figure 5: Block Diagram



1.6 Mechanical Drawing

Overall system mechanical drawings are shown in the following figures.

Figure 6: Mechanical Drawing (Top View)

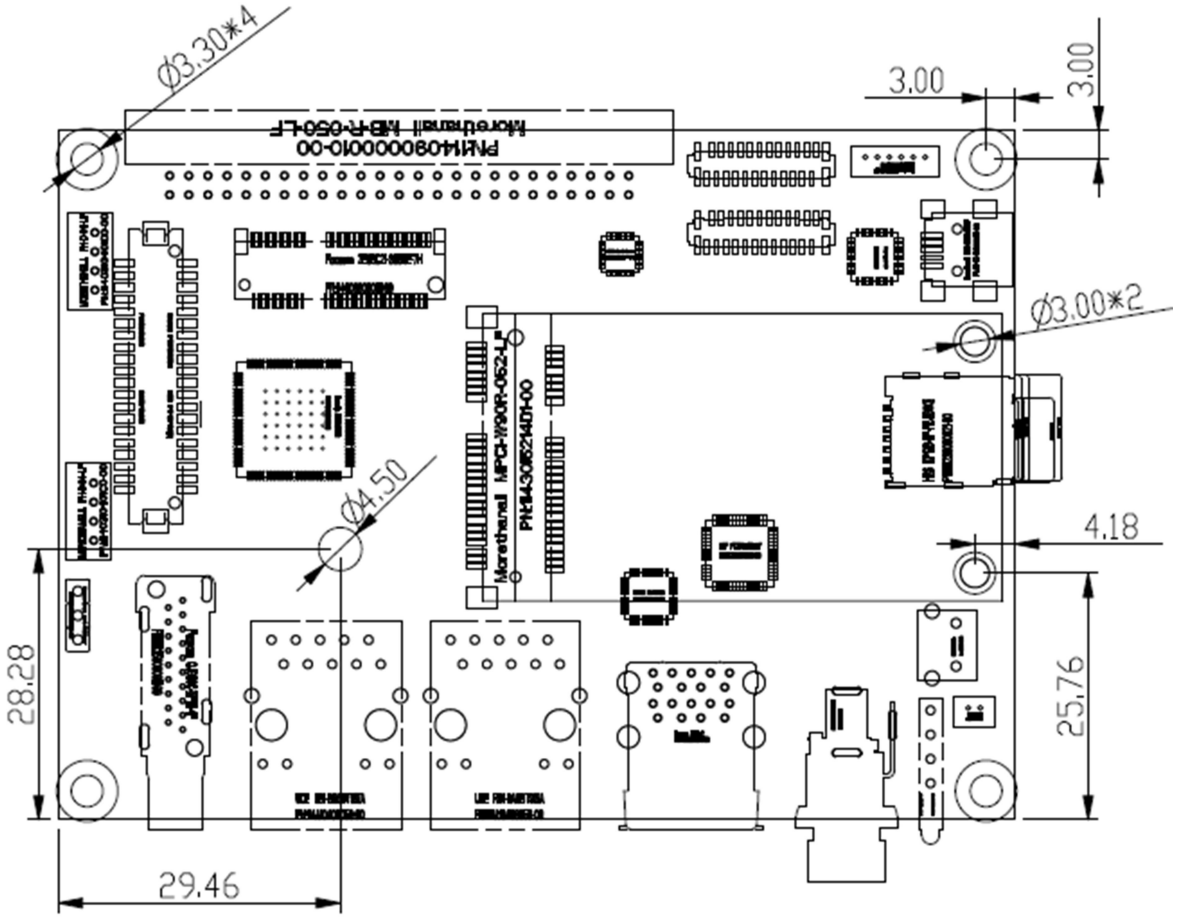


Figure 7: Mechanical Drawing (Bottom View)

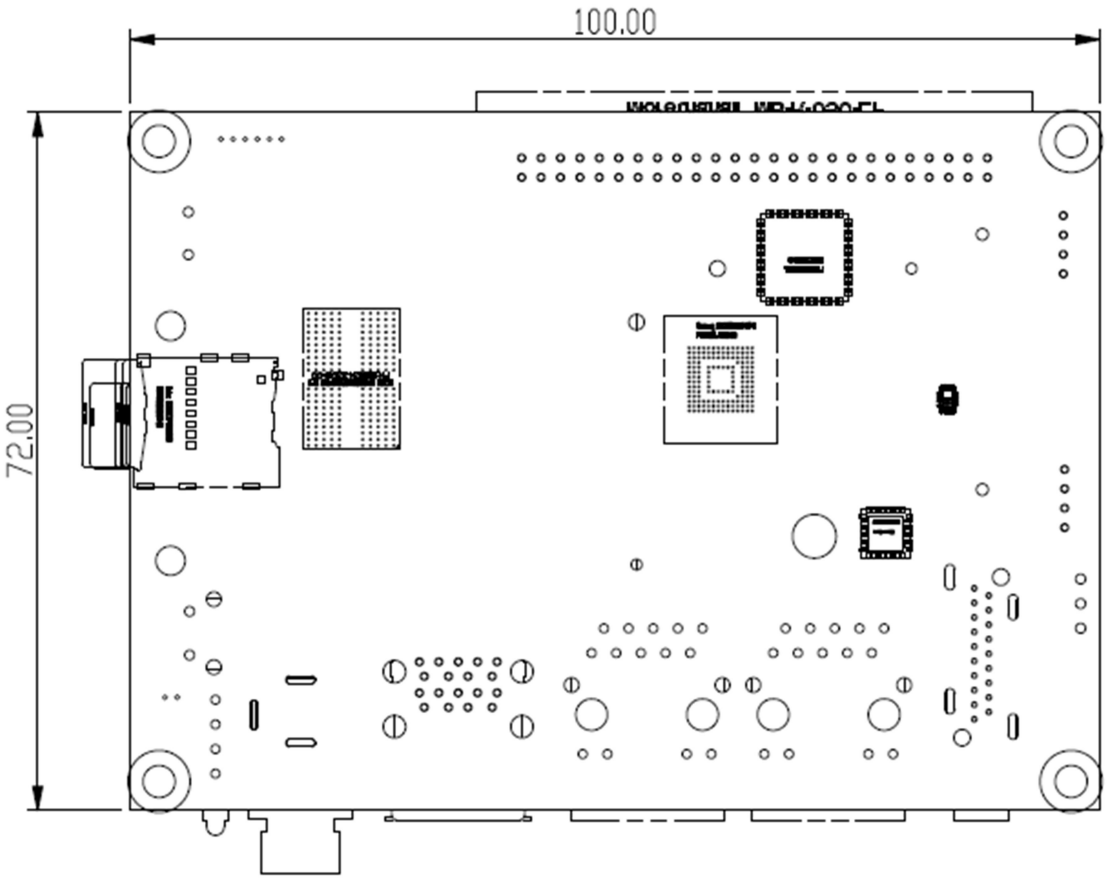
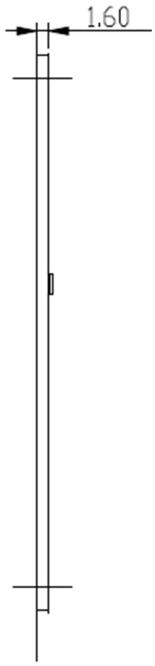
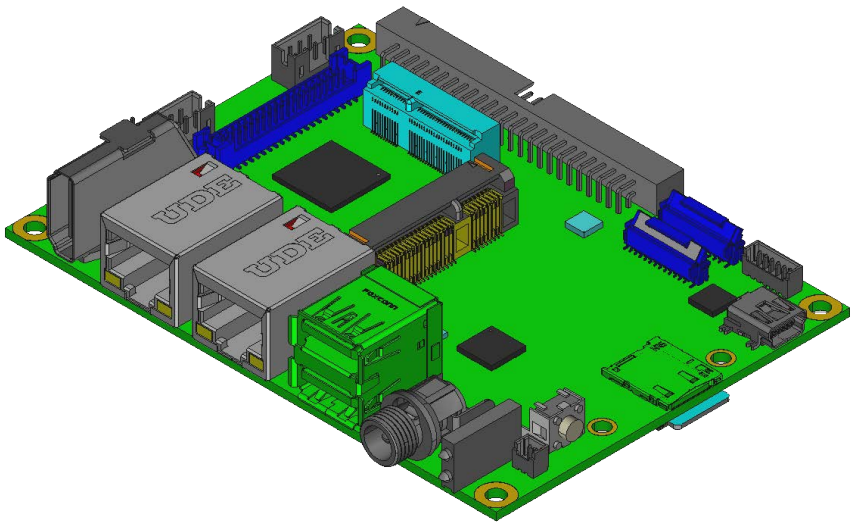


Figure 8: Mechanical Drawing (Side View)



3D .stp or .igs model are available from Embedian's website.



1.7 Software Installation and Support

Embedian supports and keeps updating the most recent BSP from NXP. All most update software source codes, build and installation instructions can be found at the development center on Embedian's website. Please also contact the sales person for the technical support windows.

Hardware Configuration

This section contains general information about:

- Jumpers
- Switches
- LEDs
- EEPROM
- Passive Cooler

Chapter 2 Hardware Configuration

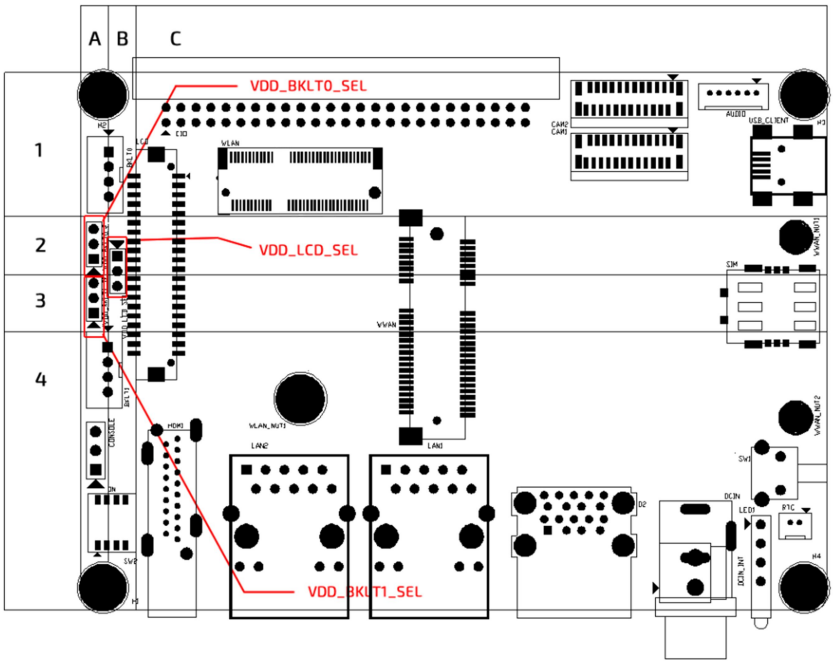
This chapter gives the definitions and shows the positions of jumpers, switched, LED and EEPROM. All of the configuration jumpers on the board are in the proper position.

2.1 Jumpers

The pITX-MX8M-Plus has a number of jumpers that allow you to configure your system to suit your application. All use 2mm shorting blocks (shunts) to select settings. Turn off power to the pITX-MX8M-Plus before changing the position of a shunt.

2.1.1 Jumper Location

Figure 9 Jumper Location



2.1.2. List of Jumpers

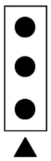
The table below lists the function of various jumpers.

Label	Function
VDD_BKLT0_SEL	5V/12V LVDS LCD Backlight Voltage
VDD_BKLT1_SEL	5V/12V MIPI-DSI LCD Backlight Voltage
VDD_LCD_SEL	3.3V/5V LVDS/MIPI-DSI LCD VDD Voltage

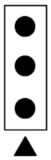
2.1.3. Jumper Settings

The following tables describe how the jumper shunts to various configurations.

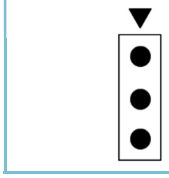
VDD_BKLT0_SEL: Location on Board, A2

VDD_BKLT0_SEL	5V/12V LVDS LCD Backlight Voltage	
	Setting	Function
	VDD_BKLT0_SEL (1-2)	5V
	VDD_BKLT0_SEL (2-3)	12V (Default)

VDD_BKLT1_SEL: Location on Board, A3

VDD_BKLT1_SEL	5V/12V MIPI-DSI LCD Backlight Voltage	
	Setting	Function
	VDD_BKLT1_SEL (1-2)	5V
	VDD_BKLT1_SEL (2-3)	12V

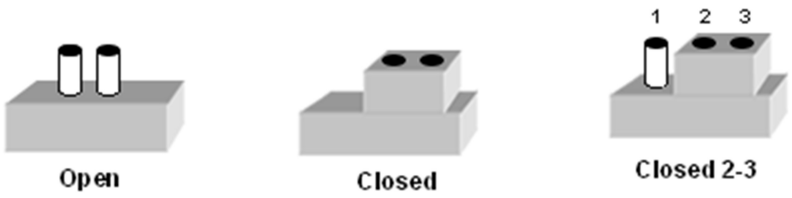
VDD_LCD_SEL: Location on Board, B2, B3

VDD_LCD_SEL	3.3V/5V LVDS/MIPI-DSI LCD VDD Voltage	
	Setting	Function
	VDD_LCD_SEL (1-2)	3.3V (Default)
	VDD_LCD_SEL (2-3)	5V

2.1.4. Setting Jumpers

You configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To "close" a jumper you connect the pins with the clip.

To "open" a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2 or 2 and 3.



The jumper settings are schematically depicted in this manual as follows.

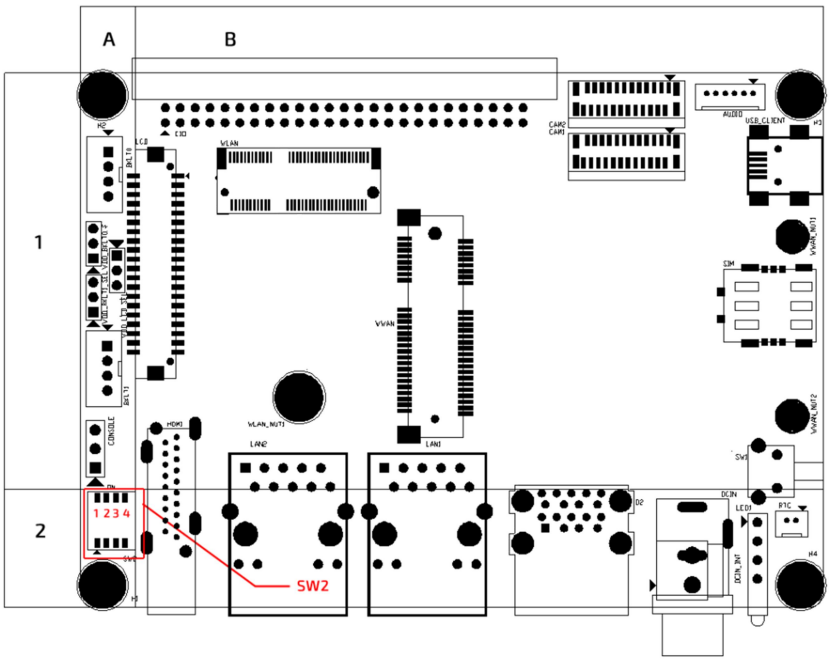
A pair of needle-nose pliers may be helpful when working with jumpers. If you have any doubts about the best hardware configuration for your application, contact your sales representative before you make any change.

2.2 Switches

The pITX-MX8M-Plus has one 4-port switch allow you to select where to boot up the board and configure the USB1_ID to determine USB1 as a USB 3.0 host (to EIO50 expansion connector) or client port (mini type B).

2.2.1 Switch Location

Figure 10 Switch Location



2.2.2. List of Switches

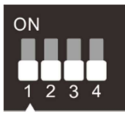
The table below lists the function of various jumpers.

Label	Function
SW2.1-3	Port 1-3: Boot Select
SW2.4	Port4: Pull USB1_ID to High (Switch OFF) or Low (Switch ON) to configure USB1 as a USB 3.0 host (to the EIO50 50-pin expansion connector) or USB Client (mini type B).

2.2.3. Switch Settings

The following tables describe the switch configurations.

SW2: Location on Board, A2

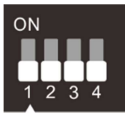
SW2	Setting			Function
Port 1-3	1	2	3	Boot Select
	ON	ON	ON	Boot from Micro SD card
	OFF	ON	OFF	Boot from eMMC flash

NOTICE

The first stage bootloader in the CPU ROM will read port 1 and port 2 configurations and decide where to load the second stage booloader (u-boot). If (port 1, port 2) is set (ON, ON), it will load from micro SD card. If (port 1, port 2) is set (OFF ON), it will load from eMMC flash.

Once the second stage booloader (u-boot) is loaded, it will read port 3 configuration and decide where to load the Linux kernel. If port 3 is set high, the u-boot will load Linux kernel from micro SD card. Otherwise, it will load Linux kernel from eMMC flash.

SW2: Location on Board, A2

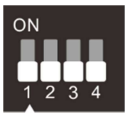
SW2	Setting	Function
Port 4	4	USB_ID
	ON	USB1_ID is low. USB1 signals from i.MX8M Plus will go to EIO50 connector and serve as a USB host.
	OFF	USB1_ID is high. USB1 signals from iMX8M Plus will go to mini type B connector and serve as a client port.

NOTICE

There are two USB 3.0/2.0 (USB1 and USB2) in i.MX8M Plus processor. USB2 connects to Microchip USB 5807C USB3.0/2.0 hub as shown in the block diagram. USB1 goes either to EIO50 connector or USB client connector.

2.2.4. Setting Switches

You configure your board to match the needs of your application by setting switches.



The diagram in the left shows switches off.

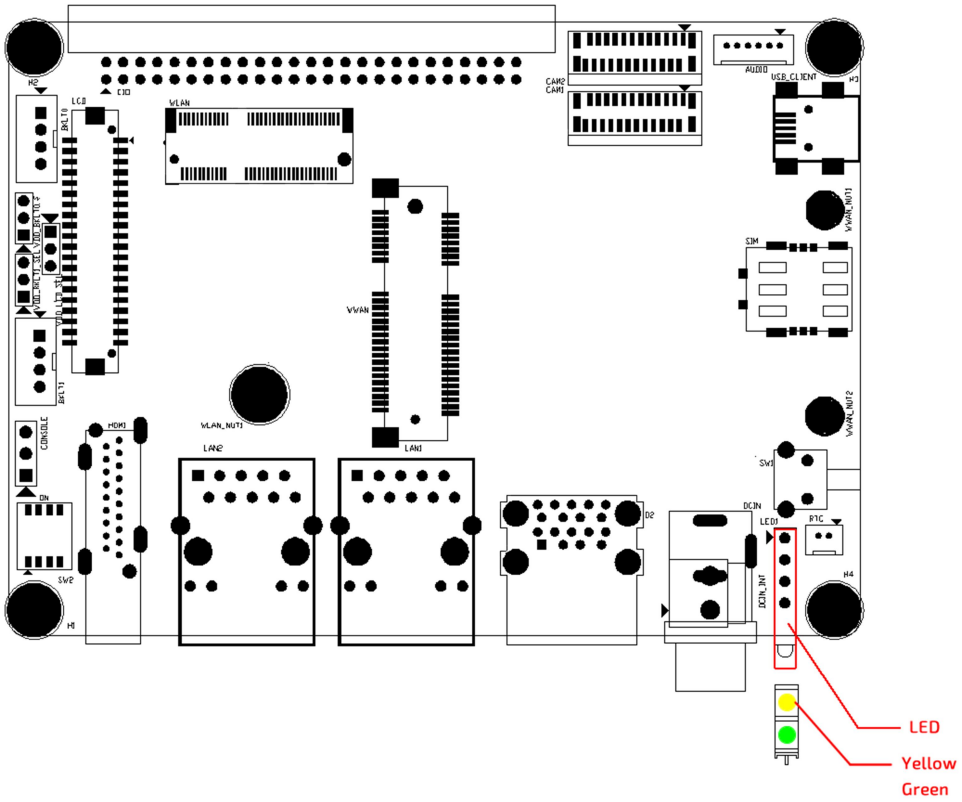
The diagram in the left shows switches on.

2.3 LED

The pITX-MX8M-Plus implements a 2mm bi-level yellow/green LEDs. One (green) indicates the power status and the other (yellow) is free for use by user defined.

2.3.1 LED Location

Figure 11 LED Location



2.3.2. LED Settings

The following tables describe the LED configurations.

LED				Description
Green				Show power status
Yellow	NXP i.MX8M Plus Processor			User Programmable
	Ball	Mode	Pin Name	
	AD8	ALT5	I2C4_SDA__GPIO5_IO21	

2.4 EEPROM

The pITX-MX8M-Plus SBC includes an I2C serial EEPROM available on the I2C1 bus. An On Semiconductor 24C32 or equivalent EEPROM is used. The device operates at 1.8V. The serial EEPROM is placed at I2C slave addresses address 50 hex.

The serial EEPROM is intended to retain board parameter information, including part number, hardware revision number, serial number, and Ethernet MAC addresses. The module serial EEPROM data structure conforms to the PICMG® EEEP Embedded EEPROM Specification.

Note:

The EEPROM ID memory layout is now follow the mainline and as follows.

Name	Size (Bytes)	Contents
Header	4	MSB 0xEE3355AA LSB
Board Name	8	Name for Board in ASCII “PITX8MP4” = pITX-MX8M-Plus Commercial Temperature with 4GB LPDDR4 Configuration “PTXI8MP4” = pITX-MX8M-Plus Industrial Temperature with 4GB LPDDR4 Configuration
Hardware Revision	4	Hardware version code for version in ASCII “00A0” = rev. A0
Serial Number	12	Serial number of the board. This is a 12 character string which is: WWYYAABBnnnn Where: WW = 2 digit week of the year of production YY = 2 digit year of production AABB= “PITX” is commercial temp. and “PTXI” is industrial temp. nnnn = incrementing board number
MAC1 Address	6	Ethernet MAC 1 Address
MAC2 Address	6	Ethernet MAC 2 Address

NOTICE The u-boot and Linux kernel will read the Ethernet MAC address in EEPROM.

2.5 Passive Cooler (VTT-HS-9A981-A1)

⚠ CAUTION

pITX-MX8M-Plus should only operate with a suitable heat sink. Allow to cool down after operation.

Figure 12 Passive Cooler

Coastline I/O Connectors

This Chapter gives coastline I/O connectors detail information. Section includes:

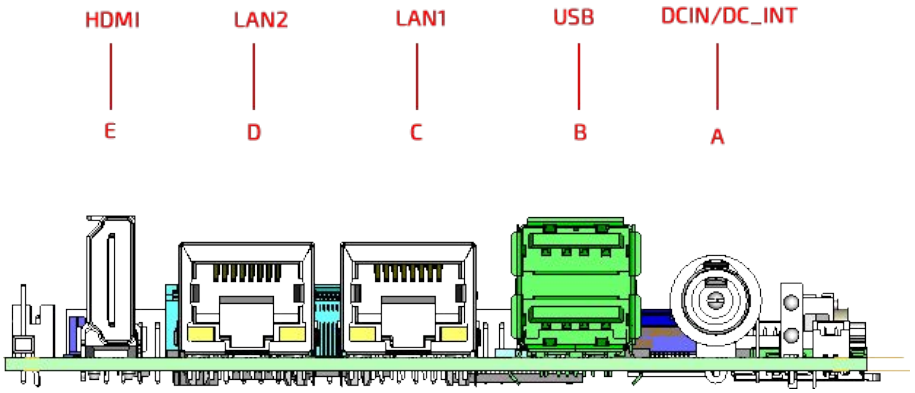
- Connector Locations
- List of Connectors
- Connector Pin Assignments

Chapter 3 Coastline I/O Connectors

Coast line panel I/O connectors of pITX-MX8M-Plus are described in this section.

3.1 Connector Locations

Figure 13 Connector Locations



3.2 List of Connectors

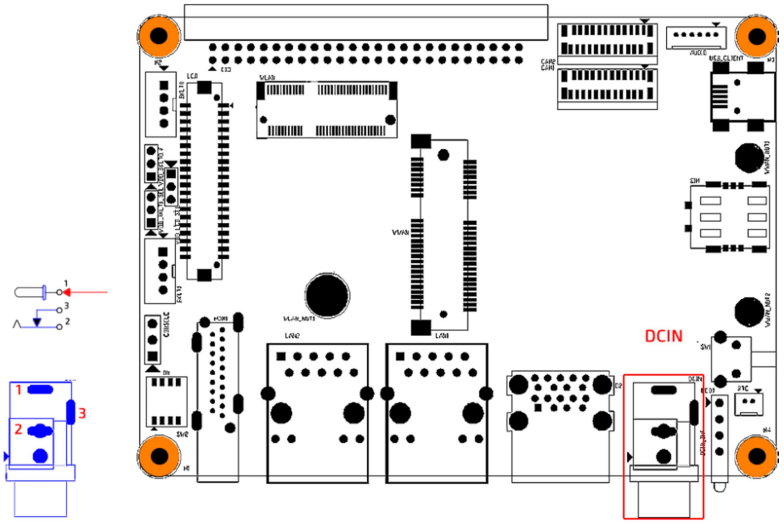
The table below lists the function of various connectors.

Reference	Location	Description
DCIN/DC_INT	A	12V DC Power Input by lockable 2.50mm DC Jack (default) /by 3.96mm 2-pin pin Header
USB	B	USB 3.0 Type A Connector Dual Stack
LAN1	C	10/100/1000Mbps Ethernet 1 RJ45 Connector (eth0)
LAN2	D	10/100/1000Mbps Ethernet 2 RJ45 Connector (eth1)
HDMI	E	HDMI Connector

3.3 Connector Pin Assignments

3.3.1 DCIN/DC_INT (12V DC Power Supply by DC Jack/ 3.96mm 2-pin Header)

Figure 14 DCIN/DC_INT Connector Locations



The pITX-iMX8M-Plus operates with a 12 V DC +/- 10% power supply. We design DC Jack and 2 Pos 3.96mm Pin Header co-layout, default uses lockable 2.5mm DC Jack.

DCIN: Lockable Power Jack Connector

pin	Assignment	Signal	Description
1	+V12_IN	+12V Power Input	PWR
2	GND	Power Ground	PWR
3	GND	Power Ground	PWR

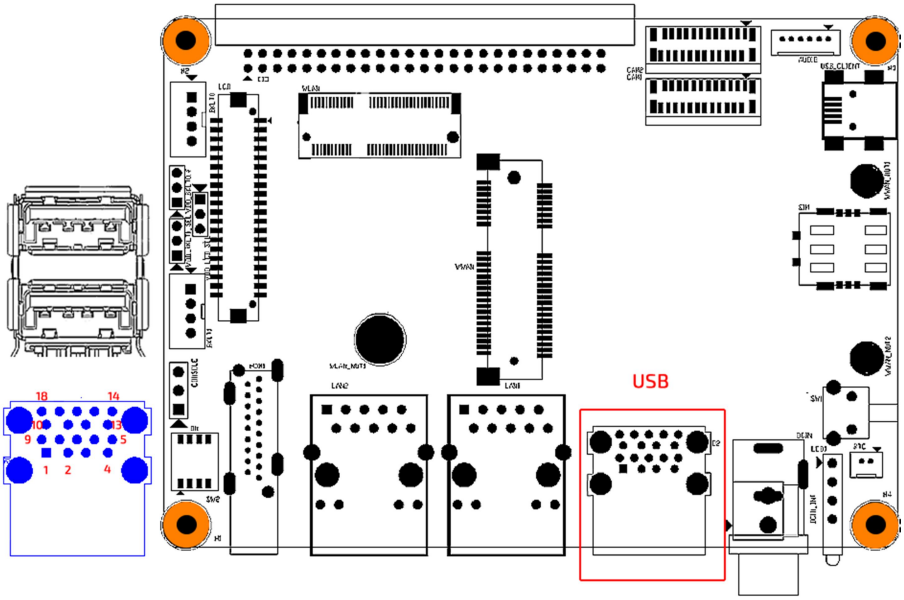
DC_INT: Internal 2 Pos 3.96mm Power Header Connector

pin	Assignment	Signal	Description
1	+V12_IN	+12V Power Input	PWR
2	GND	Power Ground	PWR

3.3.2 USB

pITX-iMX8MP-Plus board supports a dual-stacked USB3.0 interface. Both ports can reach 5 Gbps speed (Super Speed).

Figure 15 Dual-Stacked USB 3.0 Connector



pin	Assignment	Signal	Description
1	+VBUS_USB5_TOP	PWR	USB 5V Power Distribution to downstream device.
2	USB_TOP_D-	BIDIR	USB3 HUB P1 differential USB 2.0 data-.
3	USB_TOP_D+	BIDIR	USB3 HUB P1 differential USB 2.0 data+.
4	GND_TOP	PWR	Ground
5	USB_TOP_SSRX-	INPUT	USB3 HUB P1 differential USB 3.0 receive data-.
6	USB_TOP_SSRX+	INPUT	USB3 HUB P1 differential USB 3.0 receive data+.
7	GND_DRAIN_TOP	PWR	Ground
8	USB_TOP_SSTX-	OUTPUT	USB3 HUB P1 differential USB 3.0 transmit data -.
9	USB_TOP_SSTX+	OUTPUT	USB3 HUB P1 differential USB 3.0 transmit data +.
10	+VBUS_USB5_BOT	PWR	USB 5V Power Distribution to downstream device.
11	USB_BOT_D-	BIDIR	USB3 HUB P2 differential USB 2.0 data-.
12	USB_BOT_D+	BIDIR	USB3 HUB P2 differential USB 2.0 data+.
13	GND_BOT	PWR	Ground
14	USB_BOT_SSRX-	INPUT	USB3 HUB P2 differential USB 3.0 receive data-.
15	USB_BOT_SSRX+	INPUT	USB3 HUB P2 differential USB 3.0 receive data+.
16	GND_DRAIN_BOT	PWR	Ground
17	USB_BOT_SSTX-	OUTPUT	USB3 HUB P2 differential USB 3.0 transmit data -.
18	USB_BOT_SSTX+	OUTPUT	USB3 HUB P2 differential USB 3.0 transmit data +.

NOTICE

There are two USB 3.0 compliant instances (USB1 and USB2) in i.MX8M Plus processor.

The USB1 from i.MX8M Plus operates in following modes and goes to either EIO50 expansion connector or mini type B connector. It can be configured as one of the following modes.

- Host Mode: SS/HS/FS/LS
- Device Mode: SS/HS/FS
- OTG: HS/FS/LS

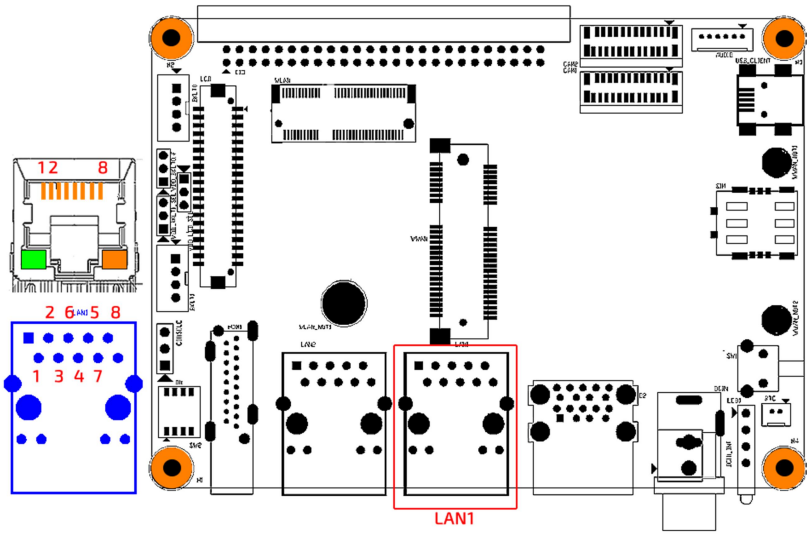
USB2 from i.MX8M Plus connects to Microchip USB 5807C 7-port USB3.0/2.0 hub and operates as USB 3.0 host only.

The signals in this dual-stacked USB3.0 connector are from port 1 (top) and port 2 (bottom) of the USB5807C hub.

3.3.3 LAN1 (Ethernet eth0)

LAN1 supports 10/100/1000 Mbit/s.

Figure 16 Ethernet Connector RJ-45 Jack with Integrated Magnetic



pin	Assignment	Description
1	LAN1_MDI0+	Differential Transmit/Receive Positive Channel 0
2	LAN1_MDI0-	Differential Transmit/Receive Negative Channel 0
3	LAN1_MDI1+	Differential Transmit/Receive Positive Channel 1
4	LAN1_MDI2+	Differential Transmit/Receive Positive Channel 2
5	LAN1_MDI2-	Differential Transmit/Receive Negative Channel 2
6	LAN1_MDI1-	Differential Transmit/Receive Negative Channel 1
7	LAN1_MDI3+	Differential Transmit/Receive Positive Channel 3
8	LAN1_MDI3-	Differential Transmit/Receive Negative Channel 3

3.3.3.1 LAN1 LEDs

The LAN1 LED signals are described as follows.

	Description
Green	Off = no receive or transmit activities On = receive or transmit activity
Orange	Off = no link, 10/100Base-T Link On = 1000Base-T Link

3.3.3.2 Path of LAN1

The first 10/100/1000Mbps LAN is implemented from RGMII2 interface of i.MX8M Plus processor that connecting to a Realtek RTL8211FD(I)-CG Ethernet PHY. The implementation from i.MX8M Plus to RTL8211FD(I)-CG is show in the following table.

NXP i.MX8M Plus Processor RGMII2			Realtek RTL8211FD(I)-CG		Description
Ball	Mode	Pin Name	Pin #	Pin Name	
AJ8	ALT4	SAI1_RXD3__ ENET1_MDIO	14	MDIO	Serial Management Interface data input/output
AH9	ALT4	SAI1_RXD2__ ENET1_MDC	13	MDC	Serial Management Interface clock
AD10	ALT4	SAI1_RXD4__ ENET1_RGMII_RD0	25	RXD0	Bit 0 of the 4 data bits that are sent by the transceiver on the receive path.
AE10	ALT4	SAI1_RXD5__ ENET1_RGMII_RD1	24	RXD1	Bit 1 of the 4 data bits that are sent by the transceiver on the receive path.
AH10	ALT4	SAI1_RXD6__ ENET1_RGMII_RD2	23	RXD2	Bit 2 of the 4 data bits that are sent by the transceiver on the receive path.
AH12	ALT4	SAI1_RXD7__ENET1_RGMII_RD3	22	RXD3	Bit 3 of the 4 data bits that are sent by the transceiver on the receive path.
AJ12	ALT4	SAI1_TXC__ ENET1_RGMII_RXC	27	RXC	Reference clock
AF12	ALT4	SAI1_TXFS__ ENET1_RGMII_RX_CTL	26	RXCTL	Indicates both the receive data valid (RXDV) and receive error (RXER) functions per the RGMII specification.
AH14	ALT4	SAI1_TXD4__ ENET1_RGMII_TX_CTL	19	TXCTL	Indicates that valid transmission data is present on TXD[3:0].
AJ11	ALT4	SAI1_TXD0__ ENET1_RGMII_TD0	18	TXD0	The MAC transmits data to the transceiver using this signal.
AJ10	ALT4	SAI1_TXD1__ ENET1_RGMII_TD1	17	TXD1	The MAC transmits data to the transceiver using this signal.
AH11	ALT4	SAI1_TXD2__ ENET1_RGMII_TD2	16	TXD2	The MAC transmits data to the transceiver using this signal.
AD12	ALT4	SAI1_TXD3__ ENET1_RGMII_TD3	15	TXD3	The MAC transmits data to the transceiver using this signal.
AH14	ALT4	SAI1_TXD5__ ENET1_RGMII_TXC	20	TXC	Used to latch data from the MAC into the PHY. 1000BASE-T: 125MHz 100BASE-TX: 25MHz 10BASE-T: 2.5MHz
AF10	ALT5	SAI1_RXD1__ GPIO4_IO03			LAN1 interrupt pin

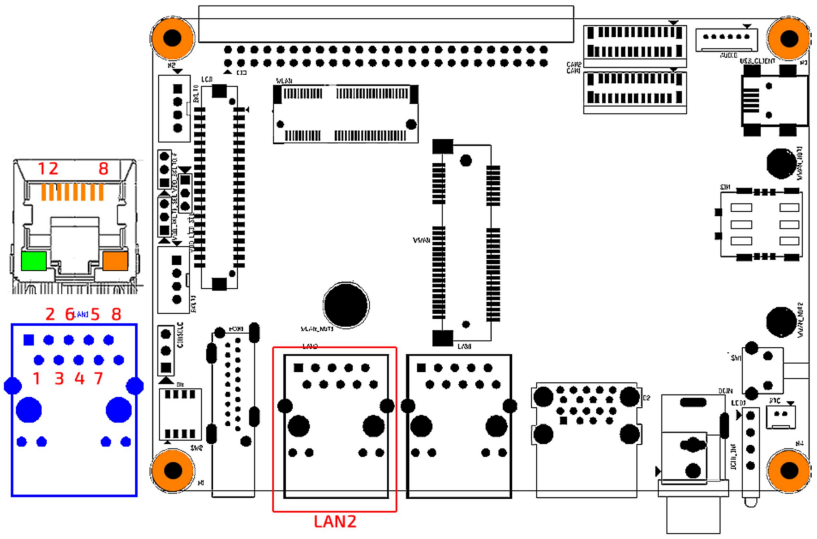
The path from RTL8211FD(I)-CG to the RJ45 connector is show in the following table.

Realtek RTL8211FD(I)-CG		RJ45 Connector	
pin	Pin Name	pin	Assignment
1	MDIP0	1	LAN1_MDI0+
2	MDIN0	2	LAN1_MDI0-
4	MDIP1	3	LAN1_MDI1+
5	MDIN1	6	LAN1_MDI1-
6	MDIP2	4	LAN1_MDI2+
7	MDIN2	5	LAN1_MDI2-
9	MDIP3	7	LAN1_MDI3+
10	MDIN3	8	LAN1_MDI3-

3.3.4 LAN2 (Ethernet eth1)

LAN2 also supports 10/100/1000 Mbit/s. In addition to that, LAN2 also supports QoS with TSN.

Figure 17 Ethernet Connector RJ-45 Jack with Integrated Magnetic



pin	Assignment	Description
1	LAN2_MDI0+	Differential Transmit/Receive Positive Channel 0
2	LAN2_MDI0-	Differential Transmit/Receive Negative Channel 0
3	LAN2_MDI1+	Differential Transmit/Receive Positive Channel 1
4	LAN2_MDI2+	Differential Transmit/Receive Positive Channel 2
5	LAN2_MDI2-	Differential Transmit/Receive Negative Channel 2
6	LAN2_MDI1-	Differential Transmit/Receive Negative Channel 1
7	LAN2_MDI3+	Differential Transmit/Receive Positive Channel 3
8	LAN2_MDI3-	Differential Transmit/Receive Negative Channel 3

3.3.4.1 LAN2 LEDs

The LAN2 LED signals are described as follows.

	Description
Green	Off = no receive or transmit activities On = receive or transmit activity
Orange	Off = no link, 10/100Base-T Link On = 1000Base-T Link

3.3.4.2 Path of LAN2

The second 10/100/1000Mbps LAN is implemented from RGMII1 interface of i.MX8M Plus processor that connecting to a Realtek RTL8211FD(I)-CG Ethernet PHY. The implementation from i.MX8M Plus to RTL8211FD(I)-CG is show in the following table.

NXP i.MX8M Plus Processor RGMII2			Realtek RTL8211FD(I)-CG		Description
Ball	Mode	Pin Name	Pin #	Pin Name	
AH29	ALT0	ENET_MDIO__ENET_QOS_MDIO	14	MDIO	Serial Management Interface data input/output
AH28	ALT0	ENET_MDC__ENET_MDC	13	MDC	Serial Management Interface clock
AG29	ALT0	ENET_RD0__ ENET_QOS_RGMII_RD0	25	RXD0	Bit 0 of the 4 data bits that are sent by the transceiver on the receive path.
AG28	ALT0	ENET_RD1__ ENET_QOS_RGMII_RD1	24	RXD1	Bit 1 of the 4 data bits that are sent by the transceiver on the receive path.
AF29	ALT0	ENET_RD2__ ENET_QOS_RGMII_RXD2	23	RXD2	Bit 2 of the 4 data bits that are sent by the transceiver on the receive path.
AF28	ALT0	ENET_RD3__ ENET_QOS_RGMII_RXD3	22	RXD3	Bit 3 of the 4 data bits that are sent by the transceiver on the receive path.
AE29	ALT0	ENET_RXC__ CCM_ENET_QOS_ CLOCK_GENERATE_RX_CLK	27	RXC	Reference clock
AE28	ALT0	ENET_RX_CTL__ ENET_QOS_RGMII_RX_CTL	26	RXCTL	Indicates both the receive data valid (RXDV) and receive error (RXER) functions per the RGMII specification.
B48	ALT0	ENET_TX_CTL__ ENET_QOS_RGMII_TX_CTL	19	TXCTL	Indicates that valid transmission data is present on TXD[3:0].
AC25	ALT0	ENET_TD0__ ENET_QOS_RGMII_TD0	18	TXD0	The MAC transmits data to the transceiver using this signal.
AE26	ALT0	ENET_TD1__ ENET_QOS_RGMII_TD1	17	TXD1	The MAC transmits data to the transceiver using this signal.
AF26	ALT0	ENET_TD2__ ENET_QOS_RGMII_TD2	16	TXD2	The MAC transmits data to the transceiver using this signal.
AD24	ALT0	ENET_TD3__ ENET_QOS_RGMII_TD3	15	TXD3	The MAC transmits data to the transceiver using this signal.
AE24	ALT0	ENET_RGMII_TXC__ CCM_ENET_QOS_ CLOCK_GENERATE_TX_CLK	20	TXC	Used to latch data from the MAC into the PHY. 1000BASE-T: 125MHz 100BASE-TX: 25MHz 10BASE-T: 2.5MHz
AH17	ALT5	SAI2_RXFS__ GPIO4_IO21			LAN2 interrupt pin

The path from RTL8211FD(I)-CG to the RJ45 connector is show in the following table.

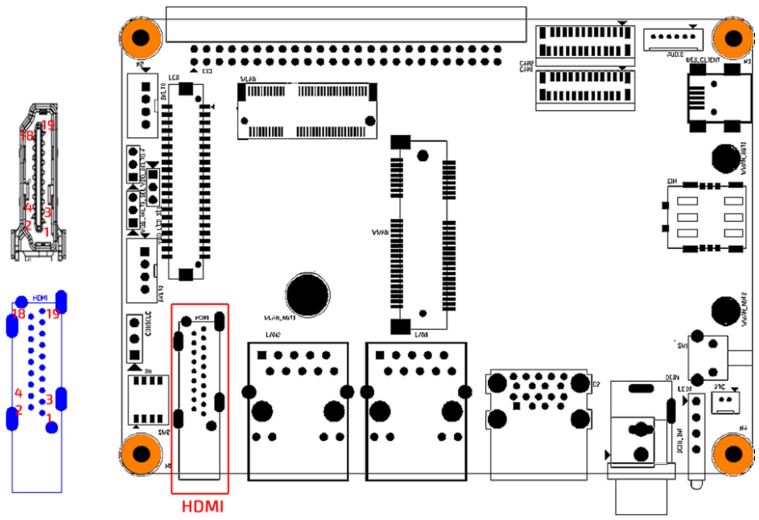
Realtek RTL8211FD(I)-CG		RJ45 Connector	
pin	Pin Name	pin	Assignment
1	MDIP0	1	LAN2_MDI0+
2	MDIN0	2	LAN2_MDI0-
4	MDIP1	3	LAN2_MDI1+
5	MDIN1	6	LAN2_MDI1-
6	MDIP2	4	LAN2_MDI2+
7	MDIN2	5	LAN2_MDI2-
9	MDIP3	7	LAN2_MDI3+
10	MDIN3	8	LAN2_MDI3-

NOTICE LAN2 also supports QoS with TSN. NXP offers sample codes and examples to support this feature.

3.3.5 HDMI

pITX-MX8M-Plus supports one HDMI instance. The HDMI is implemented directly from HDMI interface from NXP i.MX8M Plus processor.

Figure 18 HDMI Connector



HDMI: HDMI Pin Mapping

pin	Function	Direction	Description
1	HDMI_D2+	Out	TMDS Link Channel 2
2	GND	Ground	
3	HDMI_D2-	Out	
4	HDMI_D1+	Out	TMDS Link Channel 1
5	GND	Ground	
6	HDMI_D1-	Out	
7	HDMI_D0+	Out	TMDS Link Channel 0
8	GND	Ground	
9	HDMI_D0-	Out	
10	HDMI_CLK+	Out	TMDS Clock Channel
11	GND	Ground	
12	HDMI_CLK-	Out	
13	HDMI_CEC	In/Out	
14	HDMI_AUX-	In	Optional usage as Audio Return Channel
15	HDMI_DDC_SCL	Out	HDMI DDC Serial Clock
16	HDMI_DDC_SDA	In/Out	HDMI DDC Serial Date
17	GND	Ground	
18	+5V	Power	
19	HDMI_AUX+/HPD	In	Hot plug detect, optional usage as Audio Return Channel

Internal I/O Connectors

This Chapter gives internal I/O connectors detail information. Section includes:

- Connector Locations
- List of Connectors
- Connector Pin Assignments

Chapter 4 Internal I/O Connectors

Internal I/O connectors of pITX-MX8M-Plus are described in this section.

4.1 Connector Locations

Figure 19 Connector Locations (Top View)

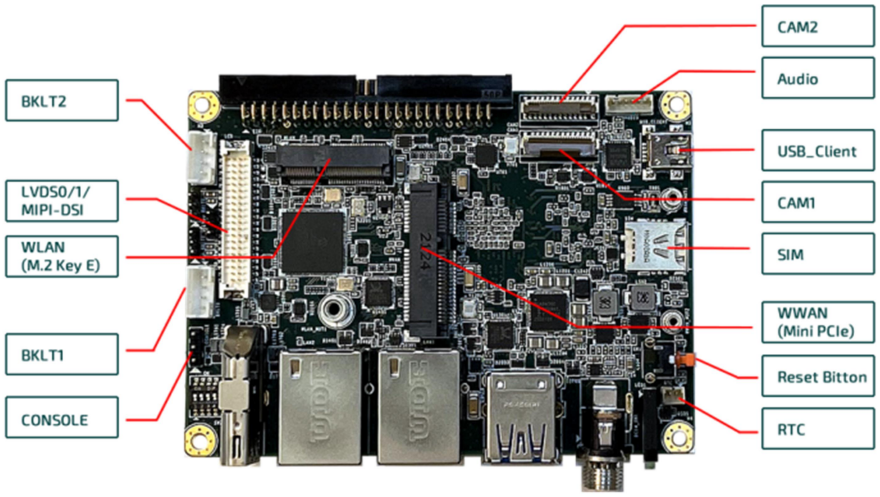
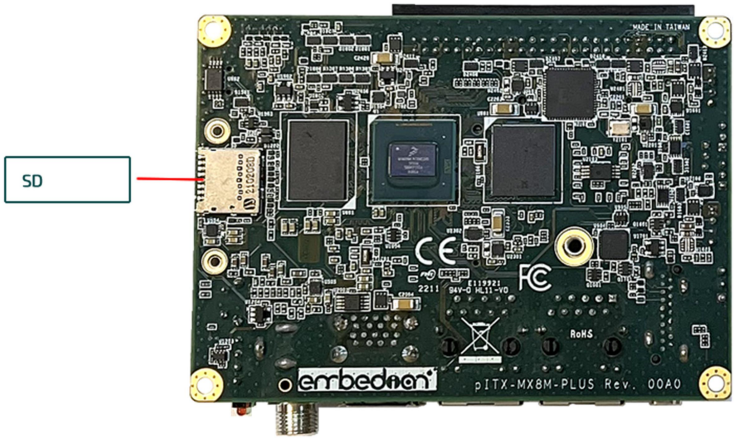


Figure 20 Connector Locations (Bottom View)



4.2 List of Connectors

The table below lists the function of various connectors.

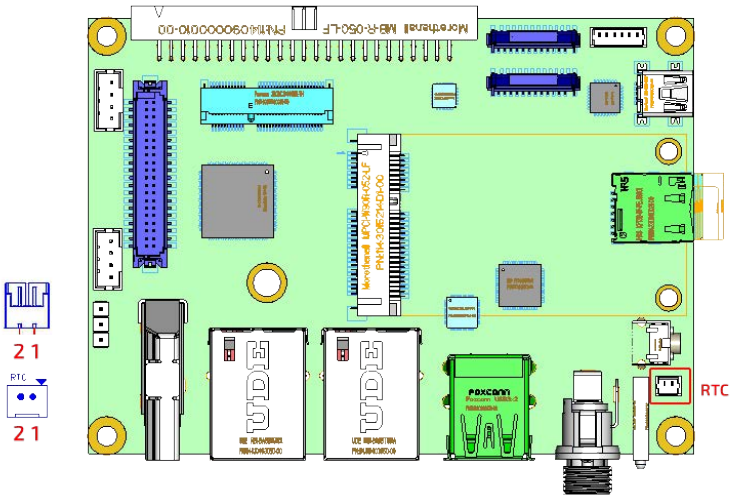
Reference	Description
RTC	RTC Battery Connector
SW1	Reset Button
BKLT0	LVDS Backlight Control Signals
BKLT1	MIPI-DSI Backlight Control Signals
LCD	LVDS, MIPI-DSI Connector
CAM1	MIPI-CSI Camera Input 1 FPC Connector
CAM2	MIPI-CSI Camera Input 2 FPC Connector
AUDIO	Min In and Line Out Connector
USB_CLIENT	USB Client mini Type B Connector
WLAN	M..2 Key E Connector
WWAN	Mini PCIe Connector
SIM	Nano SIM Card Slot
CONSOLE	Debug Uart Console Connector
SD	Micro SD Card Slot

4.3 Connector Pin Assignments

4.3.1 RTC (RTC Battery 2-pin 1.25mm Connector)

The 2-pin connector has a 1.25 mm pitch.

Figure 21 RTC Battery 2-pin Connector Locations

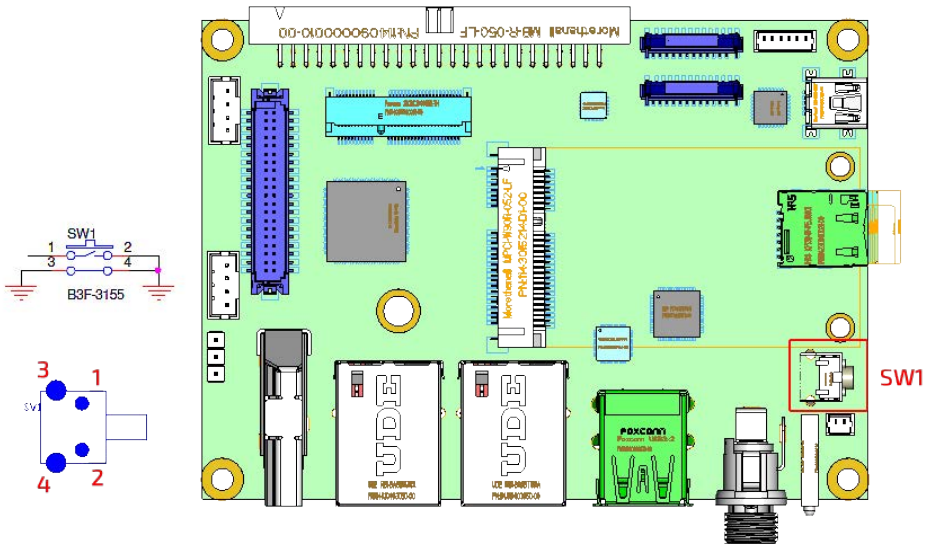


RTC: 2-pin 1.25mm connector (Connector: Molex 0530470210 or compatible. Mating Connector: Molex 0510210200 or compatible)

pin	Signal
1	+COIN_RTC
2	GND

4.3.2 SW1 (Reset Button)

Figure 22 RESET Button Locations

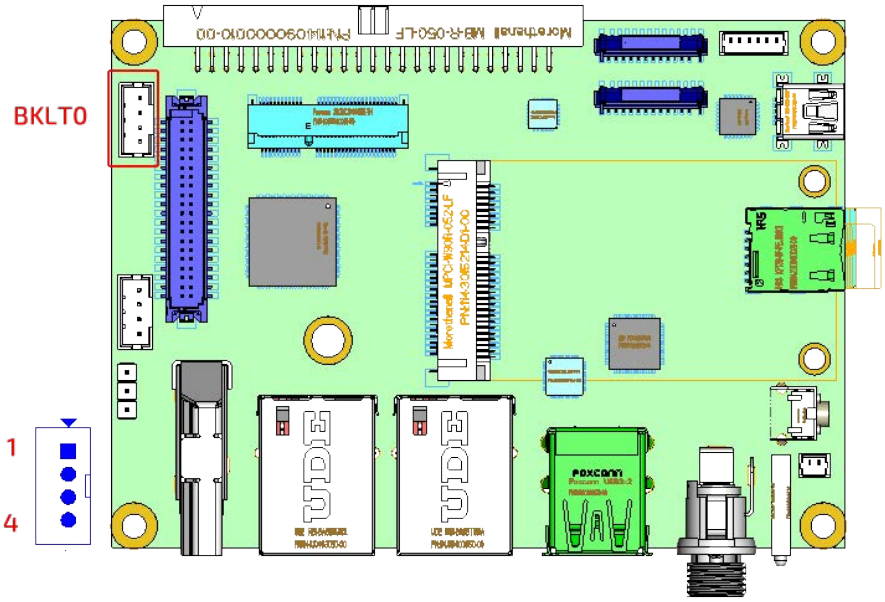


SW1: RESET Button

pin	Signal
1	RESET_IN#
2	GND
3	GND
4	GND

4.3.3 BKLT0 (LVDS Backlight Control Signals)

Figure 23 BKLT0 Locations

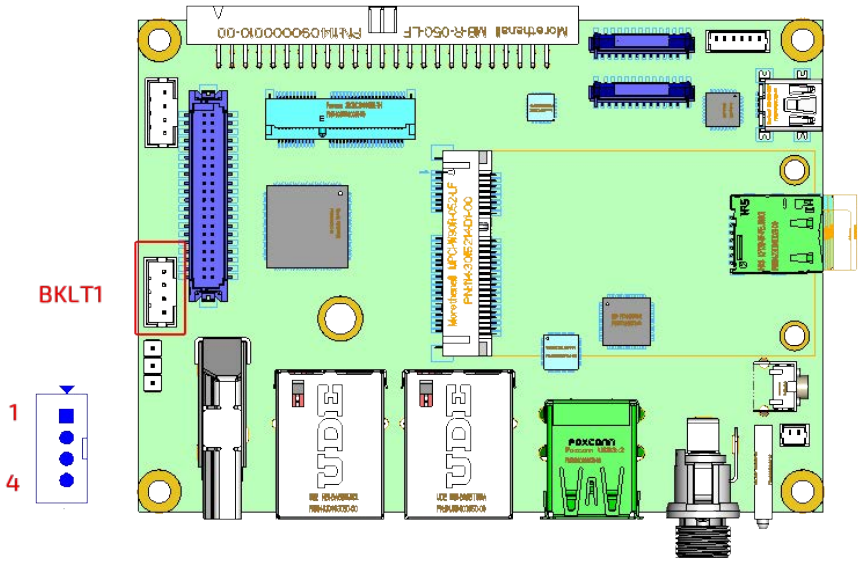


BKLT0: LVDS Backlight Control Signals (Mating Connector: JST PHR-4 or compatible)

pin	Signal	NXP i.MX8M Plus Processor			Description
		Ball	Mode	Pin Name	
1	VDD_BKLT0				Backlight Power
2	LCD0_BKLT_EN	AC12	ALT5	SAI1_TXD6__GPIO4_IO18	High enables panel backlight
3	LCD0_BKLT_PWM	AE16	ALT2	SAI5_RXD0__PWM2_OUT	Display backlight PWM control
4	GND				Ground

4.3.4 BKLT1 (MIPI-DSI Backlight Control Signals)

Figure 24 BKLT1 Locations



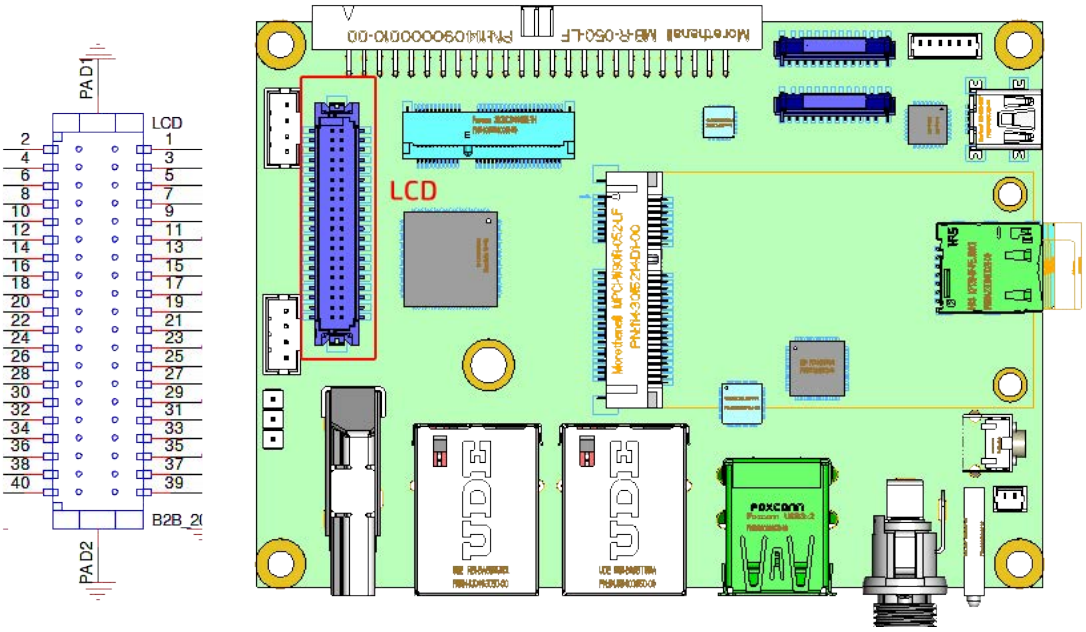
BKLT1: MIPI-DSI Backlight Control Signals (Mating Connector: JST PHR-4 or compatible)

pin	Signal	NXP i.MX8M Plus Processor			Description
		Ball	Mode	Pin Name	
1	VDD_BKLT1				Backlight Power
2	LCD1_BKLT_EN	AE12	ALT5	SAI1_MCLK__GPIO4_IO20	High enables panel backlight
3	LCD1_BKLT_PWM	AE18	ALT1	SPDIF_TX__PWM3_OUT	Display backlight PWM control
4	GND				Ground

4.3.5 LCD (LVDS, MIPI-DSI Connector)

pITX-MX8M-Plus supports one single channel or one Dual Channel 24 bit LVDS LCD display. It also supports one 4-Lane MIPI-DSI interface that shared with LVDS1. All LVDS and MIPI-DSI signals are from i.MX8M Plus processor.

Figure 25 LCD Locations



LCD: LVDS0, LVDS1 and MIPI-DSI Signals (Mating Connector: Hirose DF13-40DS-1.25DSA(55) or compatible)

pin	Signal	NXP i.MX8M Plus Processor			Description
		Ball	Mode	Pin Name	
1	VDD_LCD				LVDS panel VDD
2	VDD_LCD				LVDS panel VDD
3	VDD_LCD				LVDS panel VDD
4	VDD_LCD				LVDS panel VDD
5	GND				Ground
6	GND				Ground
7	LVDS0_D0-	E28			LVDS0 LCD data channel differential pairs 1-
8	LVDS1_D0-/ MIPI_DSI_D0-	B26/ B16			LVDS1/MIPI-DSI LCD data channel differential pairs 1-
9	LVDS0_D0+	D29			LVDS0 LCD data channel differential pairs 1+
10	LVDS1_D0+/ MIPI_DSI_D0+	A26/ A16			LVDS1/MIPI-DSI LCD data channel differential pairs 1+
11	GND				Ground
12	GND				Ground
13	LVDS0_D1-	F28			LVDS0 LCD data channel differential pairs 2-
14	LVDS1_D1-/ MIPI_DSI_D1-	B27/ B17			LVDS1/MIPI-DSI LCD data channel differential pairs 2-
15	LVDS0_D1+	E29			LVDS0 LCD data channel differential pairs 2+
16	LVDS1_D1+/ MIPI_DSI_D1+	A27/ A17			LVDS1/MIPI-DSI LCD data channel differential pairs 2+
17	GND				Ground
18	GND				Ground
19	LVDS0_D2-	H28			LVDS0 LCD data channel differential pairs 3-
20	LVDS1_D2-/ MIPI_DSI_D2-	C28/ B18			LVDS1/ MIPI-DSI LCD data channel differential pairs 3-

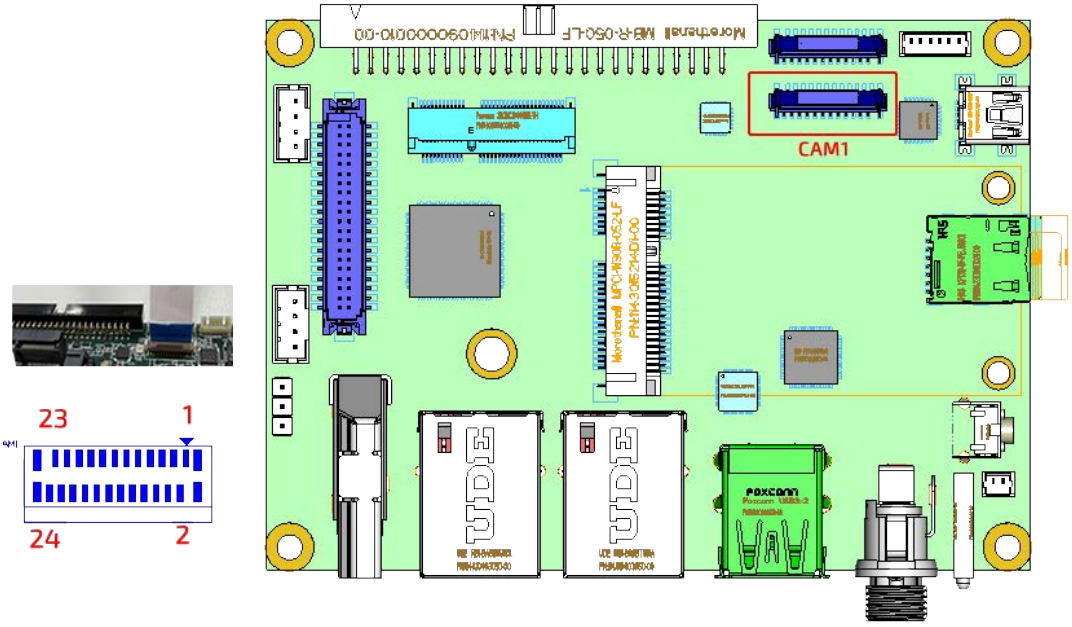
(Continued)

pin	Signal	NXP i.MX8M Plus Processor			Description
		Ball	Mode	Pin Name	
21	LVDS0_D2+	G29			LVDS0 LCD data channel differential pairs 3+
22	LVDS1_D2+/ MIPI_DSI_D2+	B29/ A19			LVDS1/MIPI_DSI LCD data channel differential pairs 3+
23	GND				Ground
24	GND				Ground
25	LVDS0_CK-	G28			LVDS0 LCD differential clock pairs-
26	LVDS1_CK-	B28/ B18			LVDS1/MIPI-DSI LCD differential clock pairs-
27	LVDS0_CK+	F29			LVDS0 LCD differential clock pairs+
28	LVDS1_CK+	A28/ A18			LVDS1/MIPI-DSI LCD differential clock pairs+
29	GND				Ground
30	GND				Ground
31	LVDS0_D3-	J28			LVDS0 LCD data channel differential pairs 4-
32	LVDS1_D3-	D29/ B20			LVDS1/MIPI_DSI LCD data channel differential pairs 4-
33	LVDS0_D3+	H29			LVDS0 LCD data channel differential pairs 4+
34	LVDS1_D3+	C29/ A20			LVDS1/MIPI_DSI LCD data channel differential pairs 4+
35	GND				Ground
36	GND				Ground
37	I2C2_SCL	AH6	ALT0	I2C2_SCL__I2C2_SCL	I2C_LCD bus clock
38	I2C2_SDA	AE8	ALT0	I2C2_SDA__I2C2_SDA	I2C_LCD bus data
39	EDP0_HPD				eDP0 Hot Plug Detect
40	EDP1_HPD				eDP1 Hot Plug Detect

4.3.6 CAM1 (MIPI-CSI Camera Input 1 FPC Connector)

pITX-MX8M-Plus supports two MIPI-CSI2 interfaces. The 24-pin 0.5mm FPC connector default supports Google /Coral 5Mpix CAMERA MODULE, Omnivision OV5645. Users can purchase them from Coral's website at https://coral.ai/products/camera/

Figure 26 CAM1 Locations



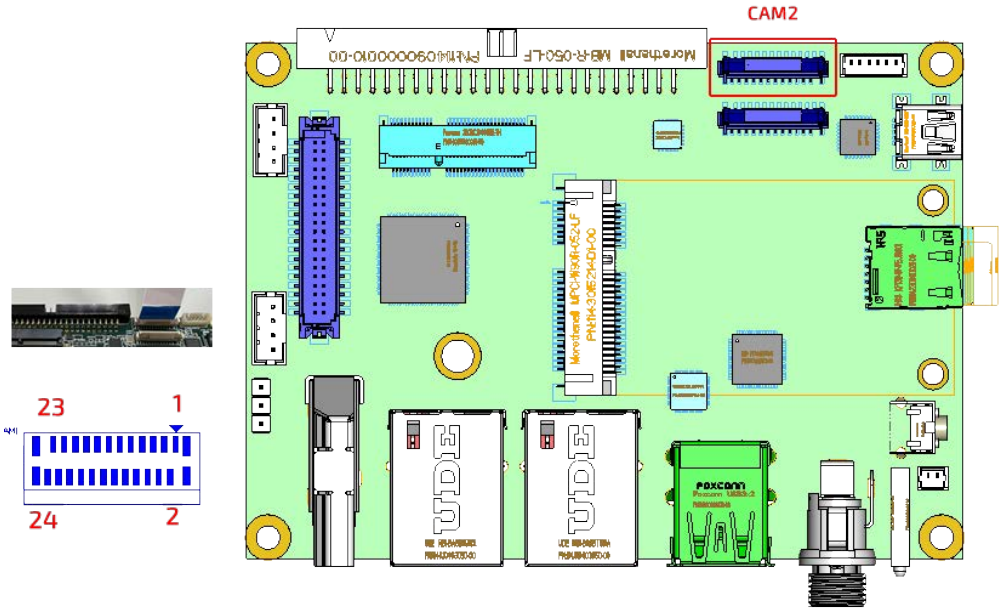
CAM1: MIPI-CSI Camera Input 1 FPC Connector (Connector: Hirose FH12S-50S-0.5SH(55) or compatible)

pin	Signal	NXP i.MX8M Plus Processor			Description
		Ball	Mode	Pin Name	
1	VDD_CAM1				3.3V CAM1 VDD
2	CAM1_RST#	L23	ALT5	NAND_DATA01__GPIO3_IO07	Camera Reset (Active Low)
3	CAM1_VSYNC	AJ18	ALT5	SAI3_RXC__GPIO4_IO29	CAM1 Vsync.
4	CAM1_I2C_SDA	AD14	ALT3	SAI5_RXC__I2C6_SDA	I2C Data
5	CAM1_I2C_SCL	AC14	ALT3	SAI5_RXFS__I2C6_SCL	I2C Clock
6	GND				Ground
7	CAM1_MCK	A4	ALT6	GPIO1_IO14__CCM_CLKO1	CAM1 MCLK
8	CAM1_PWR#	R25	ALT5	NAND_DATA00__GPIO3_IO06	Camera Power Down (Active Low)
9	GND				Ground
10	MIPI_CSI1_D3_P	D26			Differential Data3 P
11	MIPI_CSI1_D3_N	E26			Differential Data3 N
12	GND				Ground
13	MIPI_CSI1_D2_P	D24			Differential Data2 P
14	MIPI_CSI1_D2_N	E24			Differential Data2 N
15	GND				Ground
16	MIPI_CSI1_D1_P	D20			Differential Data1 P
17	MIPI_CSI1_D1_N	E20			Differential Data1 N
18	GND				Ground
19	MIPI_CSI1_CLK_P	D22			Differential Clock P
20	MIPI_CSI1_CLK_N	E22			Differential Clock N
21	GND				Ground
22	MIPI_CSI1_D0_P	D18			Differential Data0 P
23	MIPI_CSI1_D0_N	E18			Differential Data0 N
24	GND				Ground

4.3.7 CAM2 (MIPI-CSI Camera Input 2 FPC Connector)

The second MIPI-CSI2 interface also uses 24-pin 0.5mm FPC connector and default supports Google /Coral 5Mpix CAMERA MODULE, Omnivision OV5645.

Figure 27 CAM2 Locations



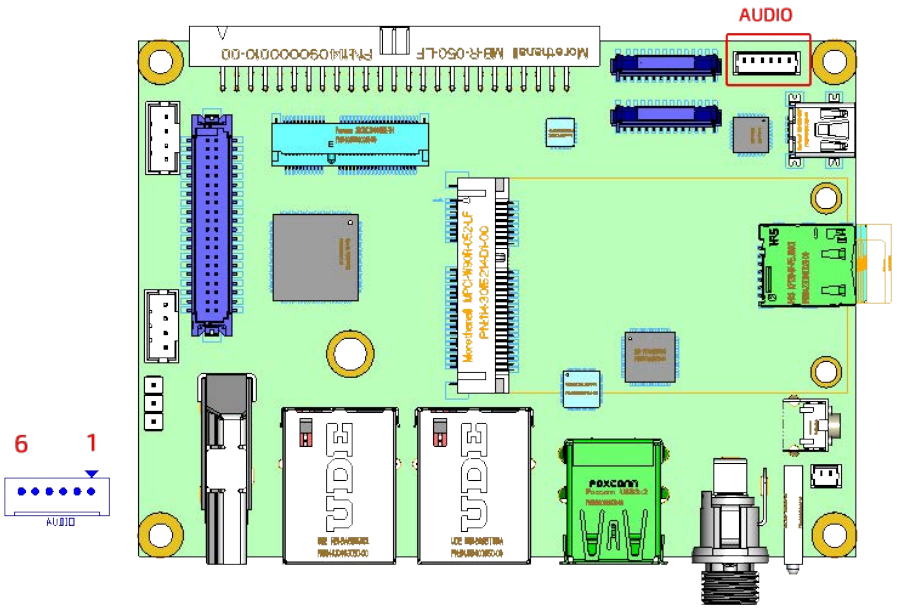
CAM2: MIPI-CSI Camera Input 2 FPC Connector (Connector: Hirose FH12S-50S-0.5SH(55) or compatible)

pin	Signal	NXP i.MX8M Plus Processor			Description
		Ball	Mode	Pin Name	
1	VDD_CAM1				3.3V CAM2 VDD
2	CAM2_RST#	N24	ALT5	NAND_DATA03__GPIO3_IO09	Camera Reset (Active Low)
3	CAM2_VSYNC	AJ9	ALT5	SAI1_RXFS__GPIO4_IO00	CAM2 Vsync.
4	CAM2_I2C_SDA	AJ22	ALT2	ECSPI2_SS0__I2C4_SDA	I2C Data
5	CAM2_I2C_SCL	AH20	ALT2	ECSPI2_MISO__I2C4_SCL	I2C Clock
6	GND				Ground
7	CAM2_MCK	A4	ALT6	GPIO1_IO14__CCM_CLKO1	CAM2 MCLK
8	CAM2_PWR#	L24	ALT5	NAND_DATA02__GPIO3_IO08	Camera Power Down (Active Low)
9	GND				Ground
10	MIPI_CSI2_D3_P	B21			Differential Data3 P
11	MIPI_CSI2_D3_N	A21			Differential Data3 N
12	GND				Ground
13	MIPI_CSI2_D2_P	B22			Differential Data2 P
14	MIPI_CSI2_D2_N	A22			Differential Data2 N
15	GND				Ground
16	MIPI_CSI2_D1_P	B24			Differential Data1 P
17	MIPI_CSI2_D1_N	A24			Differential Data1 N
18	GND				Ground
19	MIPI_CSI2_CLK_P	A23			Differential Clock P
20	MIPI_CSI2_CLK_N	B23			Differential Clock N
21	GND				Ground
22	MIPI_CSI2_D0_P	B25			Differential Data0 P
23	MIPI_CSI2_D0_N	A25			Differential Data0 N
24	GND				Ground

4.3.8 Audio

The audio interface is implemented from SAI3 of i.MX8M Plus and connecting to Cirrus WM8960 Audio Codec.

Figure 28 Audio Connector Locations



Audio: 6-pin 1.25mm Audio Connector (Connector: Molex 0530470610 or compatible. Mating Connector: Molex 0510210600 0r compatible)

pin	Assignment	Description
1	HP_R	Headphone Right Channel
2	GND	Ground
3	HP_L	Headphone Left Channel
4	LINEIN_R	Line-In Right Channel
5	MIC_IN	Microphone Input
6	LINEIN_L	Line-In Left Channel

4.3.8.1 Path of Audio

The Audio interface is implemented from SAI3 interface of i.MX8M Plus processor that connecting to a Cirrus WM8960 Audio Codec. The implementation from i.MX8M Plus to WM8960 is show in the following table.

NXP i.MX8M Plus Processor SAI3			Cirrus WM8960		Description
Ball	Mode	Pin Name	Pin#	Pin Name	
AJ20	ALT0	SAI3_MCLK__ AUDIOMIX_SAI3_MCLK	11	MCLK	Master clock output to Audio codecs
N25	ALT2	NAND_ALE__ AUDIOMIX_SAI3_TX_BCLK	12	BCLK	Digital audio clock
AC16	ALT0	SAI3_TXFS__ AUDIOMIX_SAI3_TX_SYNC	13	DACLRC	Left& Right audio synchronization clock
L26	ALT2	NAND_CE0_B__ AUDIOMIX_SAI3_TX_DATA00	14	DACDAT	Digital audio Output
AJ19	ALT5	SAI3_RXFS__GPIO4_IO28	15	ADCLRC	Interrupt
AF18	ALT0	SAI3_RXD__ AUDIOMIX_SAI3_RX_DATA00	16	ADCDAT	Digital audio Input
AC8	ALT0	I2C1_SCL__I2C1_SCL	17	SCLK	I2C Clock
AH8	ALT0	I2C1_SDA__I2C1_SDA	18	SDIN	I2C Data

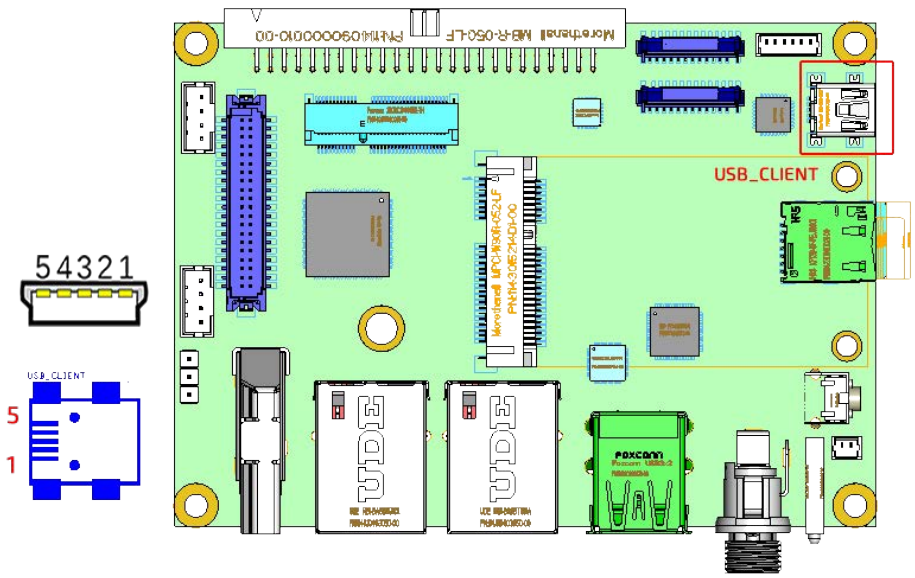
The path from WM8960 to the 6-pin 1.25mm audio connector is show in the following table.

Cirrus WM8960		Audio Connector	
pin	Pin Name	pin	Assignment
31	HP_L	1	HP_R
		2	GND
29	HP_R	3	HP_L
7	RINPUT3	4	LINEIN_R
4,5	LINPUT1, RINPUT1	5	MIC_IN
2	LINPUT3	6	LINEIN_L

4.3.9 USB_Client (USB mini Type B)

pITX-MX8M-Plus offers one USB client port . The USB client is especially useful when the device running Android. The USB client signals are from USB1 interface of i.MX8M Plus processor.

Figure 29 USB Client Connector (mini Type B) Locations



USB_Client: USB mini type B Connector

pin	Assignment	Description
1	USB_VBus	+5V USB VBus
2	USB1_D_D-	USB1 Client Data-
3	USB1_D_D+	USB1 Client Data+
4	NC	Not Connected
5	GND	Ground

NOTICE

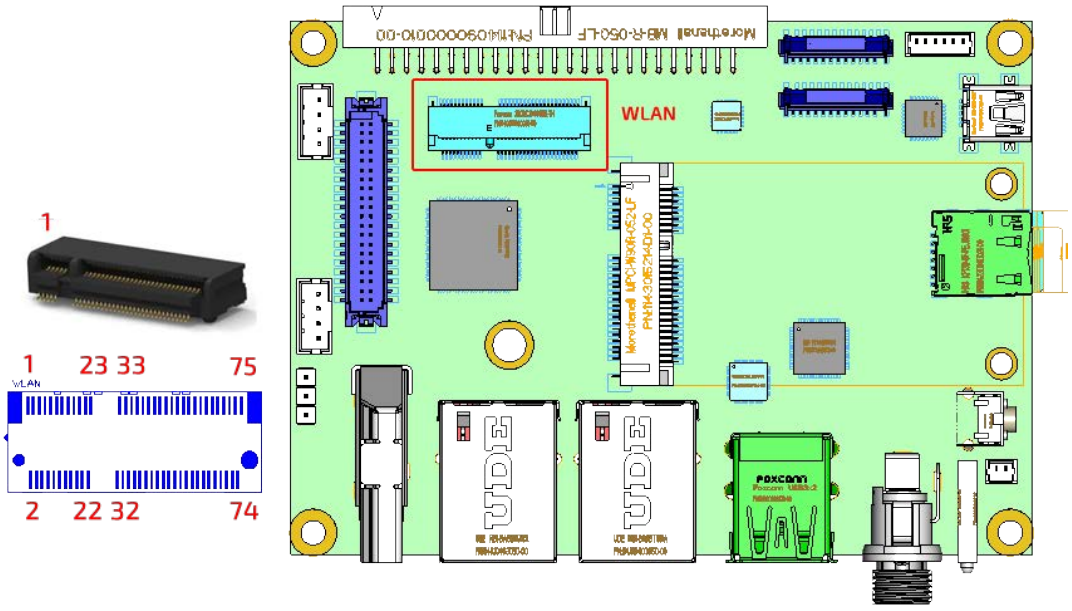
1. To use USB client port, port 4 of SW2 switch has to be switched off and the usb_dwc3_0 dr_mode in Linux kernel device tree has to be set as “peripheral”.

2. When configured as a device port, the pin 33, 35, 39, 41, 45, 47 in EIO50 expansion connector will not be functional.

4.3.10 WLAN (M.2 Key E Connector)

pITX-MX8M-Plus supports 1 M.2 Key E CONN. for extension. The M.2 interfaces include USB, PCIe, SDIO, UART and I2S.

Figure 30 WLAN (M.2 Key E) Connector Locations



WLAN: M.2 Key E Connector

pin	Signal	NXP i.MX8M Plus Processor			Description
		Ball	Mode	Pin Name	
1	GND				Ground
2	+3.3V				M.2 3.3V
3	USB_M2_D+				From USB2DN_DP4 of USB5807C hub
4	+3.3V				M.2 3.3V
5	USB_M2_D-				From USB2DN_DM4 of USB5807C hub
6	NC				Not Connected
7	GND				Ground
8	SAI2_BCLK	AH15	ALT0	SAI2_TXC__ AUDIOMIX_SAI2_TX_BCLK	Digital audio clock
9	SD1_CLK	W28	ALT0	SD1_CLK__USDHC1_CLK	SD Clock
10	SAI2_LRCLK	AJ17	ALT0	SAI2_TXFS__ AUDIOMIX_SAI2_TX_SYNC	Left& Right audio synchronization clock
11	SD1_CMD	W29	ALT0	SD1_CMD__USDHC1_CMD	SD Command
12	SAI2_RXD	AJ14	ALT0	SAI2_RXD0__ AUDIOMIX_SAI2_RX_DATA00	Digital audio Input
13	SD1_DATA0	Y29	ALT0	SD1_DATA0__USDHC1_DATA0	SD receive/transmit data 0
14	SAI2_TXD	AH16	ALT0	SAI2_TXD0__ AUDIOMIX_SAI2_TX_DATA00	Digital audio Output
15	SD1_DATA1	Y28	ALT0	SD1_DATA1__USDHC1_DATA1	SD receive/transmit data 1
16	-				Not Connected
17	SD1_DATA2	V29	ALT0	SD1_DATA2__USDHC1_DATA2	SD receive/transmit data 2
18	GND				Ground
19	SD1_DATA3	V28	ALT0	SD1_DATA3__USDHC1_DATA3	SD receive/transmit data 3
20	UART1_WAKE# _3V3				Port 6 of TCA6408 i2c IO expander (Note)
21	SD1_WAKE#	W26	ALT0	SD1_STROBE__ USDHC1_STROBE	SD Strobe
22	UART1_RXD	AD6	ALT0	UART1_RXD__UART1_DCE_RX	UART Receive Data
23	SD1_RESET#	W25	ALT0	SD1_RESET_B__ USDHC1_RESET_B	Reset SD
Key					

(Continued)

pin	Signal	NXP i.MX8M Plus Processor			Description
		Ball	Mode	Pin Name	
32	UART1_TXD	AJ3	ALT0	UART1_TXD__UART1_DCE_TX	UART Transmit Data
33	GND				Ground
34	UART1_CTS#	AJ4	ALT1	UART3_TXD__ UART1_DCE_RTS	UART Clear to Send
35	PCIE_A_TX+	A15			PCIE Transmitter Lane +
36	UART1_RTS#	AE6	ALT1	UART3_RXD__ UART1_DCE_CTS	UART Ready to Send
37	PCIE_A_TX-	B15			PCIE Transmitter Lane -
38	-				Not Connected
39	GND				Ground
40	-				Not Connected
41	PCIE_A_RX+	A14			PCIE Receiver Lane +
42	-				Not Connected
43	PCIE_A_RX-	B14			PCIE Receiver Lane -
44	-				Not Connected
45	GND				Ground
46	-				Not Connected
47	PCIE_A_REFCK+				PCIE Reference Clock +, from external clock generator
48	-				Not Connected
49	PCIE_A_REFCK-				PCIE Reference Clock -, from external clock generator
50	WLAN_SUSCLK_3V3				SUSCLK(32kHz) (O)(0/3.3V)
51	GND				Ground
52	M2_RESET#_ 3V3				Port 3 of TCA6408 i2c IO expander (Note)
53	PCIE_A_ CKREQ#_3V3				Port 4 of TCA6408 i2c IO expander (Note)
54	M2_W_ DISABLE2#_ 3V3				Port 2 of TCA6408 i2c IO expander (Note)
55	PCIE_A_WAKE#_ +3.3V				Port 5 of TCA6408 i2c IO expander (Note)

(Continued)

pin	Signal	NXP i.MX8M Plus Processor			Description
		Ball	Mode	Pin Name	
56	M2_W_ DISABLE1#_ 3V3				Port 1 of TCA6408 i2c IO expander (Note)
57	GND				Ground
58	I2C1_SDA	AH7	ALT0	I2C1_SDA__I2C1_SDA	I2C1 Data
59	-				Not Connected
60	I2C1_SCL	AC8	ALT0	I2C1_SCL__I2C1_SCL	I2C1 Clock
61	-				Not Connected
62	M2_IRQ#	AC26	ALT5	SD2_WP__GPIO2_IO20	M.2 Interrupt
63	GND				Ground
64	-				Not Connected
65	-				Not Connected
66	-				Not Connected
67	-				Not Connected
68	-				Not Connected
69	GND				Ground
70	-				Not Connected
71	-				Not Connected
72	+3.3V				M.2 3.3V
73	-				Not Connected
74	+3.3V				M.2 3.3V
75	GND				Ground

NOTICE

1.Due to the insufficient free IOs, an 8-port I2C IO expander TCA6408 at i2c slave address 0x20 from I2C1 of i.MX8M Plus is used. Below is the summary of port mapping.

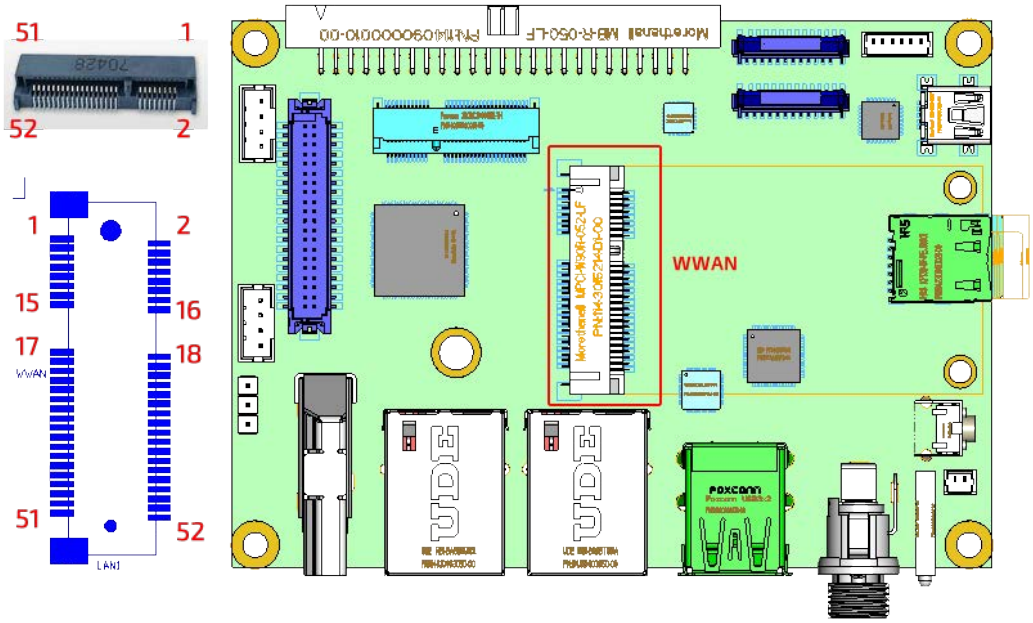
TCA6408		WLAN M.2 Connector	Description
Port	Signals	Pin#	
P0	WLAN_PWR_EN		Enable M.2 +3.3V
P1	M2_W_DISABLE1#_3V3	56	Disable radio operation
P2	M2_W_DISABLE2#_3V3	54	Disable radio operation
P3	M2_RESET#_3V3	52	Reset all services
P4	PCIE_A_CKREQ#_3V3	53	Request PCIe running clock
P5	PCIE_A_WAKE#_3V3	55	PCIe Link Reactivation
P6	UART_WAKE#_3V3	20	Radio to wake up the MPU/MCU.
P7	-		Not Connected

2. The Linux device descriptor for UART1 is /dev/ttymxc0.

4.3.11 WWAN (Mini-PCIe Connector)

pITX-MX8M-Plus supports 1 Full size Mini-PCIe CONN. for extension. The Mini PCIe interfaces include USB2.0 and USB 3.0.

Figure 31 WWAN (Mini-PCIe) Connector Locations



WWAN: Mini-PCIe Connector (0.80mm Pitch, 5.20mm Height, PCI Express* Mini Card, 52 Circuit, Right Angle, Surface Mount, 0.25μm Gold (Au) Plating)

Top Side			Bottom Side		
Pin	Signal	Function	Pin	Signal	Function
1	WWAN_ WAKE#_3V3	P3 of TCA6408 i2c IO expander (Note)	2	+3.3V	+3.3V Power
3	-	Not Connected	4	GND	Ground
5	-	Not Connected	6	-	Not Connected
7	-	Not Connected	8	UIM_PWR	Sim card VDC power supply
9	GND	Ground	10	UIM_DATA	Sim card serial data
11	-	Not Connected	12	UIM_CLK	Sim card clock signal
13	-	Not Connected	14	UIM_RESET	Sim card reset signal
15	GND	Ground	16	UIM_VPP	Programing voltage input
Key					
17	-	Not Connected	18	GND	Ground
19	-	Not Connected	20	WWAN_W_ DISABLE1#_3V3	P1 of TCA6408 i2c IO expander (Note)
21	GND	Ground	22	WWAN_ PERST#_3V3	P3 of TCA6408 i2c IO expander (Note)
23	USB_WWAN_ SSRX-	USB3DN_RXDM5 of USB5807C Hub	24	+3.3V	+3.3V Power
25	USB_WWAN_ SSRX+	USB3DN_RXDP5 of USB5807C Hub	26	GND	Ground
27	GND	Ground	28	-	Not Connected
29	GND	Ground	30	I2C1_SCL	I2C Clock
31	USB_WWAN_ SSTX-	USB3DN_TXDM5 of USB5807C Hub	32	I2C1_SDA	I2C Data
33	USB_WWAN_ SSTX+	USB3DN_TXDP5 of USB5807C Hub	34	GND	Ground
35	GND	Ground	36	USB_WWAN_D-	USB2DN_DM5 of USB5807C Hub

(Continued)

Top Side			Bottom Side		
Pin	Signal	Function	Pin	Signal	Function
37	GND	Ground	38	USB_WWAN_D+	USB2DN_DP5 of USB5807C Hub
39	+3.3V	+3.3V Power	40	GND	Ground
41	+3.3V	+3.3V Power	42	-	Not Connected
43	GND	Ground	44	-	Not Connected
45	-	Not Connected	46	-	Not Connected
47	-	Not Connected	48	-	Not Connected
49	-	Not Connected	50	GND	Ground
51	WWAN_W_ DISABLE2#_3V3	P2 of TCA6408 i2c IO expander (Note)	52	+3.3V	+3.3V Power

NOTICE

1. USB 2.0 and USB 3.0 signals in mini PCIe connectors are from port 5 of USB5807C USB Hub.

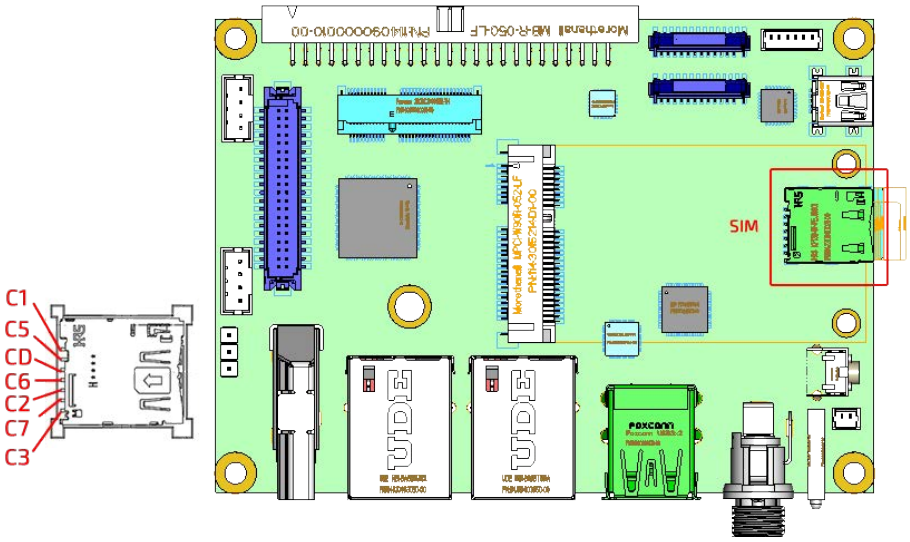
2. Due to the insufficient free IOs, an 8-port I2C IO expander TCA6408 at i2c slave address 0x21 from I2C1 of i.MX8M Plus is used. Below is the summary of port mapping.

TCA6408		WLAN M.2 Connector	Description
Port	Signals	Pin#	
P0	WWAN_PWR_EN		Enable Mini PCIe +3.3V
P1	WWAN_W_DISABLE1#_3V3	20	Disable radio operation
P2	WWAN_W_DISABLE2#_3V3	51	Disable radio operation
P3	WWAN_PERST#_3V3	22	Reset all services
P4	-		Not Connected
P5	WWAN_WAKE#_3V3	1	Mini PCIe Link Reactivation
P6	UIM_CD_3V3 (to SIM Card)		SIM Card Detect
P7	-		Not Connected

4.3.12 SIM (Nano SIM Card Slot)

pITX-MX8M-Plus supports one nano SIM card slot in case that a 3G/4G/5G module inserting to the mini PCIe connector inserting.

Figure 32 SIM (Nano SIM Card Slot)



SIM: SIM card Connector (Hirose KP13B-SF-PEJ(800), Push-Push Type)

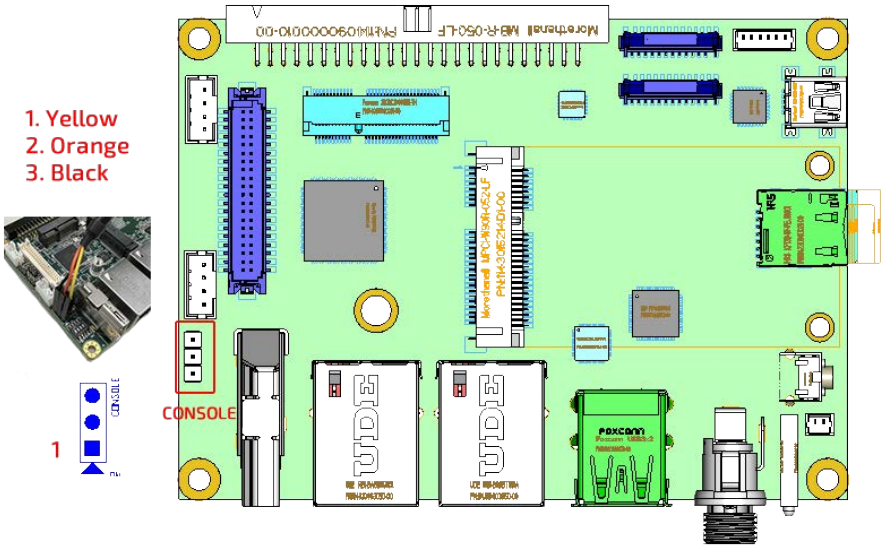
pin	Assignment	Description
C1	UIM_PWR	Power Supply Input
C2	UIM_RESET	Reset signal, used to reset the card's communications.
C3	UIM_CLK	Provides the card with a clock signal, from which data communications timing is derived
C4	-	Not Connected
C5	GND	Ground
C6	UIM_VPP	Programing voltage input
C7	UIM_DATA	Serial Data
CD	UIM_CD#_3V3	SIM Card Detect, from P7 of TCA6408

4.3.13 CONSOLE (Debug UART Console Connector)

pITX-MX8M-Plus uses 3-pin 2.54mm header as a debug port This is the same Raspberry Pi. User can get the debug cable (P/N: TTL-232R-RPi) from Digikey or Mouser.

Figure 33 Debug Cable

Figure 34 CONSOL HEADER



CONSOLE: Debug UART Console Connector (3-pin 2.54mm Header)

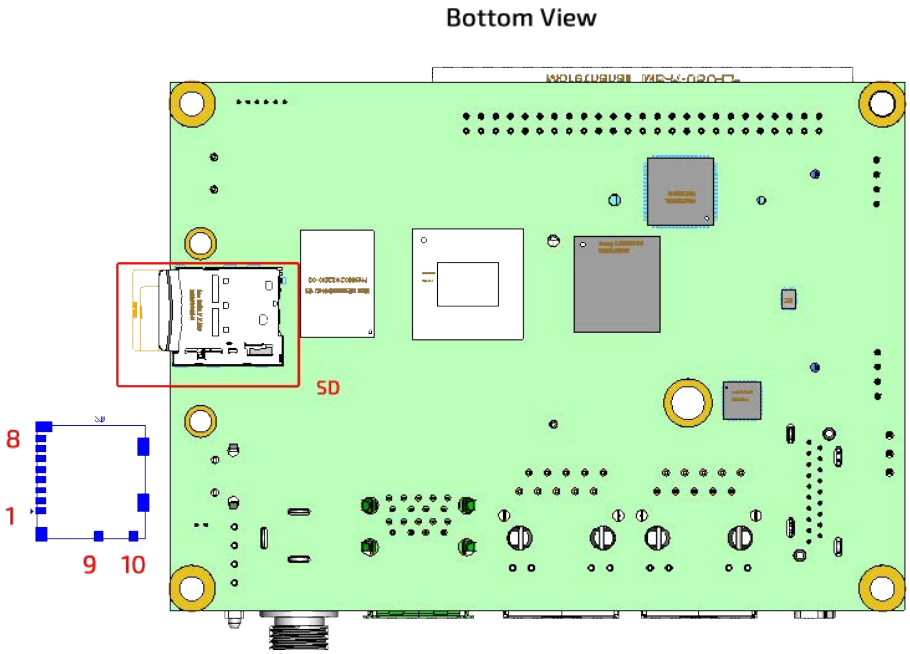
pin	Signal	NXP i.MX8M Plus Processor			Description
		Ball	Mode	Pin Name	
1	UART4_TXD	AH5	ALT0	UART4_TXD__UART4_DCE_TX	UART Transmit Data
2	UART4_RXD	AJ5	ATL0	UART4_RXD__UART4_DCE_RX	UART Receive Data
3	GND				Ground

NOTICE The mapping between the console header and console cable is as follows.

1. Yellow
2. Orange
3. Black

4.3.14 SD (Micro SD card slot)

Figure 35 Micro SD Card Slot (Bottom Side)



SD: Micro SD Card Slot (Connector: Hirose DM3NW-SF-PEJ(800), Push-Push Type)

pin	Signal	NXP i.MX8M Plus Processor			Description
		Ball	Mode	Pin Name	
1	SD2_DATA2	AA26	ALT0	SD2_DATA2__USDHC2_DATA2	SD receive/transmit data2
2	SD2_DATA3	AA25	ALT0	SD2_DATA3__USDHC2_DATA3	SD receive/transmit data3
3	SD2_CMD	AB28	ALT0	SD2_CMD__USDHC2_CMD	SD receive response/ transmit command
4	V3.3_SDIO				+3.3V
5	SD2_CLK	AB29	ALT0	SD2_CLK__USDHC2_CLK	SD Clock
6	GND				Ground
7	SD2_DATA0	AC28	ALT0	SD2_DATA0__USDHC2_DATA0	SD receive/transmit data0
8	SD2_DATA1	AC29	ALT0	SD2_DATA1__USDHC2_DATA1	SD receive/transmit data1
9	SD2_CD#	AD29	ALT5	SD2_CD_B__GPIO2_IO12	SD Card Insert Detect
10	GND				Ground

4.3.15 Watchdog Timer

An external GPIO based watchdog timer by TI TPS3828-33DBVR is implemented in pITX-MX8M-Plus. The Linux kernel will toggle the SAI1_RXD0__GPIO4_IO02 pin within 200ms. If timeout, the board will reset.

Watchdog: GPIO based external watchdog

pin	Signal	NXP i.MX8M Plus Processor			Description
		Ball	Mode	Pin Name	
1	WDT_EN	AJ15	ALT5	SAI2_MCLK__GPIO4_IO27	Enable Watchdog
2	WDT_TIME_OUT#	AC10	ALT5	SAI1_RXD0__GPIO4_IO02	Toggle Watchdog

Rear EIO50 Connector

This Chapter gives rear EIO50 connector detail information. Section includes:

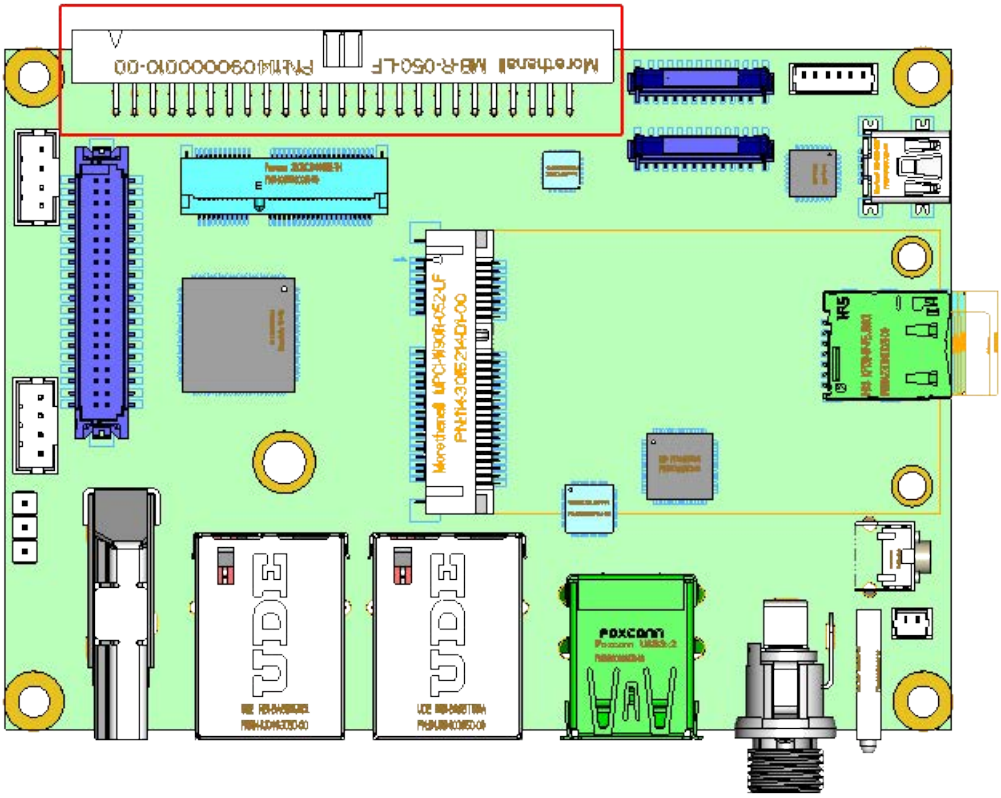
- Connector Locations
- Connector Pin Assignments

Chapter 5 Rear EIO50 Connector

A 50-pin 90-degree 2.00mm box header EIO50 expansion connector is implemented in pITX-MX8M-Plus. It is used to extend more IO functions like RS232, RS 485, CAN, USB, GPIOs, capacitive touch and SPI devices. A reference design can be downloaded from Embedian's website.

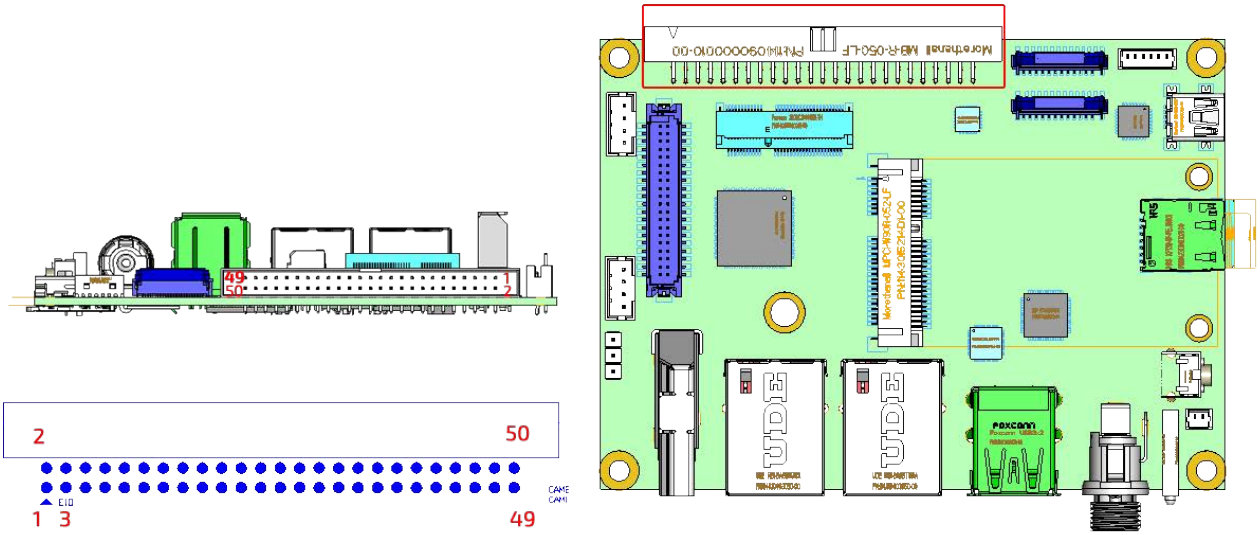
5.1 Connector Locations

Figure 36 Connector Locations



5.2 Connector Pin Assignments

Figure 37 Connector Pin Assignments



EIO50: EIO50 expansion Connector (Connector: 2 row 2.00mm 2x25 box header)

pin	Signal	NXP i.MX8M Plus Processor			Description
		Ball	Mode	Pin Name	
1	CAN1_TXD	AD16	ALT6	SAI5_RXD1__CAN1_TX	CAN1 Transmit Output
2	GND				Ground
3	CAN1_RXD	AF16	ALT6	SAI5_RXD2__CAN1_RX	CAN1 Receive input
4	UART1_TXD	AH4	ALT0	UART2_TXD__UART2_DCE_TX	From i.MX8MP UART2, Transmit Data Output
5	CAN2_TXD	AE14	ALT6	SAI5_RXD3__CAN2_TX	CAN2 Transmit Output
6	UART1_RXD	AF6	ALT0	UART2_RXD__UART2_DCE_RX	From i.MX8MP UART2, Receive Data Input
7	CAN2_RXD	AF14	ALT6	SAI5_MCLK__CAN2_RX	CAN2 Receive input
8	+12V				+12V Power Supply
9	+3.3V				+3.3V Power Supply
10	UART1_RTS#	AA29	ALT4	SD1_DATA5__UART2_DCE_CTS	From i.MX8MP UART2, Request to Send handshake line
11	SPI_MOSI	AC20	ALT0	ECSPI1_MOSI__ECSPI1_MOSI	SPI Master Data output (output from CPU, input to SPI device)
12	UART1_CTS#	U26	ALT4	SD1_DATA4__UART2_DCE_RTS	From i.MX8MP UART2, Clear to Send handshake line
13	SPI_MISO	AD20	ALT0	ECSPI1_MISO__ECSPI1_MISO	SPI Master Data input (input to CPU, output from SPI device)
14	TS_RST#	D8	ALT0	GPIO1_IO11__GPIO1_IO11	Capacitive Touch Reset Pin
15	SPI_SCLK	AF20	ALT0	ECSPI1_SCLK__ECSPI1_SCLK	SPI Master Clock output
16	UART2_TXD	AA28	ALT4	SD1_DATA6__UART3_DCE_TX	From i.MX8MP UART3, Transmit Data Output
17	SPI_SS0#	AE20	ALT5	ECSPI1_SS0__GPIO5_IO09	SPI Master Chip Select 0 output
18	UART2_RXD	U25	ALT4	SD1_DATA7__UART3_DCE_RX	From i.MX8MP UART3, Receive Data Input
19	OUT1	A7	ALT0	GPIO1_IO00__GPIO1_IO00	GPO1
20	TS_INT#	B5	ALT0	GPIO1_IO15__GPIO1_IO15	Capacitive Touch Interrupt Pin

(Continued)

pin	Signal	NXP i.MX8M Plus Processor			Description
		Ball	Mode	Pin Name	
21	USB1_D+				From USB5807C HUB P7, differential USB 2.0 data+
22	UART3_TXD				From FT2232HQ PortA, UART Transmit Data Output(Note1)
23	USB1_D-				From USB5807C HUB P7, differential USB 2.0 data-
24	UART3_RXD				From FT2232HQ PortA, UART Receive Data Input(Note1)
25	GND				Ground
26	GND				
27	USB2_D+				From USB5807C HUB P6, differential USB 2.0 data+
28	UART4_TXD				From FT2232HQ PortB, UART Transmit Data Output(Note1)
29	USB2_D-				From USB5807C HUB P6, differential USB 2.0 data-
30	UART4_RXD				From FT2232HQ PortB, UART Receive Data Input(Note1)
31	+5V_USB12				USB 5V Power Distribution to downstream device for USB1/USB2
32	+5V				+5V Power Supply

(Continued)

pin	Signal	NXP i.MX8M Plus Processor			Description
		Ball	Mode	Pin Name	
33	USB3_D+	D10			USB2.0 differential data+ from i.MX8M Plus USB1(Note3)
34	I2C1_SCL	AJ7	ALT0	I2C3_SCL__I2C3_SCL	I2C1 Clock, from i.MX8MP I2C3
35	USB3_D-	E10			USB2.0 differential data- from i.MX8M Plus USB1(Note3)
36	I2C1_SDA	AJ6	ALT0	I2C3_SDA__I2C3_SDA	I2C1 Data, from i.MX8MP I2C3
37	OUT2	E8	ALT0	GPIO1_IO01__GPIO1_IO01	GPO2
38	I2C2_SCL	AH20	ALT2	ECSPI2_MISO__I2C4_SCL	I2C2 Clock, from i.MX8MP I2C4
39	USB3_SS_TX+	A10			USB3.0 differential transmit data+ from i.MX8M Plus USB1(Note2).
40	I2C2_SDA	AJ22	ALT2	ECSPI2_SS0__I2C4_SDA	I2C2 Data, from i.MX8MP I2C4
41	USB3_SS_TX-	B10			USB3.0 differential transmit data- from i.MX8M Plus USB1(Note2).
42	GND				Ground
43	GND				Ground
44	OUT3	A3	ALT0	GPIO1_IO06__GPIO1_IO06	GPO3
45	USB3_SS_RX+	A9			USB3.0 differential receive data+ from i.MX8M Plus USB1(Note2).
46	IN1	F6	ALT0	GPIO1_IO07__GPIO1_IO07	GPI1
47	USB3_SS_RX-	B9			USB3.0 differential receive data- from i.MX8M Plus USB1(Note2).
48	IN2	A8	ALT0	GPIO1_IO08__GPIO1_IO08	GPI2
49	+V5_USB3				USB3 5V Power Distribution to downstream device for USB3
50	IN3	B8	ALT0	GPIO1_IO09__GPIO1_IO09	GPI3

NOTICE

1. An USB 2.0 to dual UARTs bridge FT2232HQ is implemented from P3 of USB5807C hub to expand two additional UARTs to the EIO connector (Pin 22, 24, 28 and 30)
2. The USB 3.0 signals (Pin 39, 41, 45, 47) in EIO connector from i.MX8M Plus will only work when SW2 P4 set to ON and Linux device tree set this port to "Host".
3. The USB 2.0 signal from i.MX8M Plus in EIO connector (Pin 33 and 35) will only work when SW2 P4 set to ON and Linux device tree set this port to "Host" or "OTG".
4. Only industrial temp. variants support CAN-FD. The commercial temp. variants support CAN 2.0b. They are TTL level signals and CAN transceivers need to be implemented on expansion board.
5. The Linux device descriptor for UART1 is /dev/ttymxc1, for UART2 is /dev/ttymxc2, for UART3 is /dev/ttyUSB0 and for UART4 is /dev/ttyUSB1.
6. The I2C buses are 2.2k pull up to 1.8V on pITX-MX8M-Plus.
7. IN2 (Pin 48, ALT2) and OUT2 (Pin 37, ALT1) can also be configured as PWM1.
8. There is one GPIO to turn on/off the +3.3V, +5V and +12V power in EIO connector. The default is ON.

Signal	NXP i.MX8M Plus Processor			Description
	Ball	Mode	Pin Name	
EIO_PWR_EN	AC18	ALT5	SPDIF_EXT_CLK__GPIO5_IO05	Enable +3.3V, +5V and +12V in EIO connector

9. Detail reference schematic for EIO expansion board is available on Embedian's website.